



Video Multiplexer Example

Summary

This application note describes the VideoMultiplexer demonstration project, which can be found in the \Examples\Reference Designs folder of the installation.

Application Note

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In this example project the user can select as video output (on J2) any one of four video inputs or any two, in which case the second video input appears picture-in-picture.

The design features the following inputs, outputs and controls:

- A 5VDC power pack socket (J6) compatible with the NanoBoard power pack.
- A power on/off switch with red "power" LED (S1 and LED5).
- Four composite video input RCA connectors (J1, J3, J4 & J5).
- One composite video output RCA connector (J2).
- Four channel-select pushbuttons (SW1, SW2, SW3 & SW4).
- Four channel status LEDs (LED1, LED2, LED3 & LED4).

Operation

- Connect a 5VDC power pack to J6.
- Connect one to four composite video sources to the input RCA connectors.
- Connect a television or studio monitor to the RCA output connector.
- Switch the device on at switch S1.

At this point the left-most input (J5) will be selected for output. LED4, next to the left-most pushbutton, is illuminated to indicate this.

- To select a new channel for output, press the corresponding button.
- To select two channels, depress the key for the main channel to display and, while this key is still being depressed, press a second key to select the picture-in-picture input. You can change you picture-in-picture selection at will until you release the main channel key. Two LEDs are now illuminated to indicate the two video sources that are being displayed.
- When finished with the unit, switch off the power at switch S1.

FPGA Design Description

This document describes the circuitry synthesized on the FPGA.

External I/O

The circuit connects via the PCB to the following peripherals:

- A 128kbyte SRAM compatible with those used on the NanoBoard.
- A Philips SAA7121 or SAA7127 video encoder (the software is configured at compile time to support whichever device is used).
- Two Philips SAA7111A video decoders.
- Four status LEDs.
- Four pushbutton inputs.
- A power on reset chip with power-good indication and watchdog input.

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The video decoders each provide an ITU recommendation BT656, 8 bit video data stream and a line-locked clock. The A clock is used as the main clock for the FPGA and the B clock is only used to clock circuits that are "upstream" of the Synchronizer. Each decoder has a four-way analogue multiplexer on its input and so can be configured to decode any of the four inputs.

Output to the video encoder is another BT656 data stream and an output clock that is derived from the decoder A clock.

The decoders and encoder, additionally, share an I2C interface that is used to configure them from the software.

Vmux_Top

The top-level schematic shows the I/O ports to the FPGA and the two main functional blocks of the design: the processor (Vmux_CPU) and the video datapath (Vmux_DataPath). It also includes the circuits required to handle external tristate devices, specifically, the I2C interface and the SRAM data I/O bus. Cross-coupled NAND gates are used to ensure that the FPGA output drivers and the SRAM outputs are never both enabled at the same time.

A low speed clock is generated to stimulate the watchdog input of the power-on-reset chip but on the current PCB, the watchdog input has been disabled.

Vmux_CPU

The processor used is the TSK51. Vertical blanking signals (50Hz) from the two video decoders drive the INT0 and INT1 inputs so the software can update the DMA and picture-in-picture (PIP) registers at the appropriate times. Odd and even field signals for each decoder are available to the software through Port 2 as are the I2C signals.

An 8-bit address latch and a write-enable decoder are wired to appear at SFR addresses 0xFE and 0xFF so that the software can communicate with the PIP and DMA control registers in the video datapath.

Vmux_DataPath

Under normal operation, with only one video input selected for display, BT656 data from decoder A (VINA[7..0]) is transferred directly to the encoder via an 8-bit multiplexer.

When picture-in-picture is selected, a number of registers are set up by the software in the PipControl block and the two DMA controllers. The PipControl block uses horizontal and vertical sync information that is extracted from the datastream by the BT656Decoder and internal counters to detect when the output pixel coordinates fall within the bounding box described by the register settings. Whenever the output falls within the bounding box, ALT_IMAGE is asserted to select an alternate BT656 datastream to be output to the encoder.

The alternate image stream is sourced from a field buffer in the external SRAM. A DMA controller copies the contents of the field buffer to the data multiplexer via a FIFO that is large enough to hold more than one scan line of the picture-in-picture image. This allows the DMA controller to operate at half the memory bandwidth (see PHIA/PHIB).

There are actually four field buffers in the external SRAM. The DMA controllers sequence through these under software control to ensure that only complete, stable images are output. The contents of the field buffers are generated from the B video decoder data stream via a synchronizer, horizontal decimator and vertical decimator.

The synchronizer receives the B video data (VINB[7..0]) on the rising edges of CLKB and writes it to a FIFO. Because there may be +/-6% frequency difference between the two, line-locked, decoder clocks, 128 bytes of data are allowed to prefill the FIFO before the CLKB side is enabled to start reading. The V, and F bits that have been extracted from the B datastream under CLKB and the adjusted H signal are "synchronized" through 4 flipflops each to minimised the probability of a metastable state persisting long enough to be a problem.

The horizontal decimator (XDecimator.VHD) takes groups of eight pixels and sums them pixel-by-pixel to produce 2 output pixels. This divides the B image by 4 in the X direction.

The vertical decimator (YDecimator.VDH) then takes the new, 180-pixel-per-line data and adds together 4 lines at a time pixel-by-pixel, outputting the results rounded to 8 bits. This divides the image by 4 in the vertical direction. This final 180 pixel by 144 line field is what is DMAed to one of the four SRAM-resident field buffers.

Software

The software (VideoMuxSrc.PrjEmb) starts by initialising the I2C interface and uses this to configure the video decoders and encoder.

Its foreground task is then to implement a state machine that handles user interactions on the keypad and LEDs.

At the interrupt level, it debounces key presses (see KeyScan) and updates the PipControl and DMA registers at a time when it is known to be safe to do so, just after the vertical blanking interval.

PCB Design Description

The following describes the circuit, sheet by sheet.

PCB_Power

Regulated power is derived from the 5V input by fast, low dropout regulators. Pi-network filters with ferrite beads provide high frequency isolation between the two supplies, the 5V input and each other. (The regulated, analogue and digital supplies to each of the other circuit blocks have similar pi-networks for the same reason.)

Clip-on heatsinks are used to lower the temperature rise of the regulators from 72 degrees celcius per watt to 23 degrees per watt. A TPS3306 supply monitor chip provides power on reset, power good, and a watchdog input. (The default load option disables the watchdog input.)

PCB_Encoder

The encoder sheet shows the SAA7127 with its analogue and digital supplies and a 5MHz low pass filter on the composite video output. Provision is made for S-Video or RGB output through an 8-pin header. If the load options on the schematic are followed, a Philips SAA7121 may be used in place of the SAA7127. However, the former device does not support RGB output. The termination filter on the LLC input should be omitted if the NanoBoard USER I/O headers are not used.

The encoder sheet includes the pullup resistors for the I2C bus.

PCB_DecoderA/B

These schematics are derived from the application notes for the SAA7111A. Series termination is provided on all high speed digital outputs. The analogue input termination circuits have been modified to present a 150 ohm load to the inputs. Since each input is shared by two decoders, the parallel load seen by the input is 75 ohms, as required. Resistor load options are provided to include the decoders' JTAG ports in the hardware JTAG chain, if required.

PCB_Controller

The Spartan2e is wired with the same pin allocation as on the NanoBoard. Because of this, it is possible to omit the on-board Spartan and drive the multiplexer board via the USER I/O headers on the NanoBoard. In this case, the NanoBoard LEDs and switches substitute for those on the PCB. The external SRAM is wired identically to RAM1 on the NanoBoard. Wiring of the Platform Flash, JTAG and Nexus chains is also based on the NanoBoard schematics.

PCB_IO

For the purpose of the LEDs and switches, see the section Operation, at the beginning of this document.

PCB_Headers

As described earlier, headers are provided for connecting to the NanoBoard through its USER I/O headers although, in practice, signal integrity is less than acceptable at 27MHz even with the Spartan's output pins set for 4mA drive and slow rise time.

Revision History

Date	Version No.	Revision
30-Jan-2004	1.0	New product release
27-Feb-2008	2.0	Updated for Altium Designer Summer 08

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