

Objective:

To design the circuit for a BCD Adder.

Theory:

In computing and electronic systems, **binary-coded decimal (BCD)** is a class of binary encodings of decimal numbers where each decimal digit is represented by a fixed number of bits. A BCD adder is a circuit that adds two BCD digits in parallel and produces a sum digit which is also in BCD. This circuit includes correction logic. For sums > 9 the circuit need to add 2's complement of 10_{10} (0110_2) to the uncorrected result ($S_3' S_2' S_1' S_0'$). Correction is also needed when a Carry out (C_o) is generated (for numbers 16-19).

BCD was used in many early decimal computers.

Component Required:

Sl No.	Item	Specification	Qty.
1	IC4008	4-bit binary full adder	2
2	IC4071	OR Gate	1
3	IC4081	AND Gate	1
4	Digital Trainer Kit	-	1
5	Breadboard	-	1
6	Wires	-	-

Decimal to BCD Table:

Decimal	Binary Sum					BCD Sum				
	C_{out}'	S_3'	S_2'	S_1'	S_0'	C_{out}	S_3	S_2	S_1	S_0
0		0	0	0	0		0	0	0	0
1		0	0	0	1		0	0	0	1
2		0	0	1	0		0	0	1	0
3		0	0	1	1		0	0	1	1
4		0	1	0	0		0	1	0	0
5		0	1	0	1		0	1	0	1
6		0	1	1	0		0	1	1	0
7		0	1	1	1		0	1	1	1
8		1	0	0	0		1	0	0	0
9		1	0	0	1		1	0	0	1
10		1	0	1	0	1	0	0	0	0
11		1	0	1	1	1	0	0	0	1
12		1	1	0	0	1	0	0	1	0
13		1	1	0	1	1	0	0	1	1
14		1	1	1	0	1	0	1	0	0
15		1	1	1	1	1	0	1	0	1
16	1	0	0	0	0	1	0	1	1	0
17	1	0	0	0	1	1	0	1	1	1
18	1	0	0	1	0	1	1	0	0	0
19	1	0	0	1	1	1	1	0	0	1

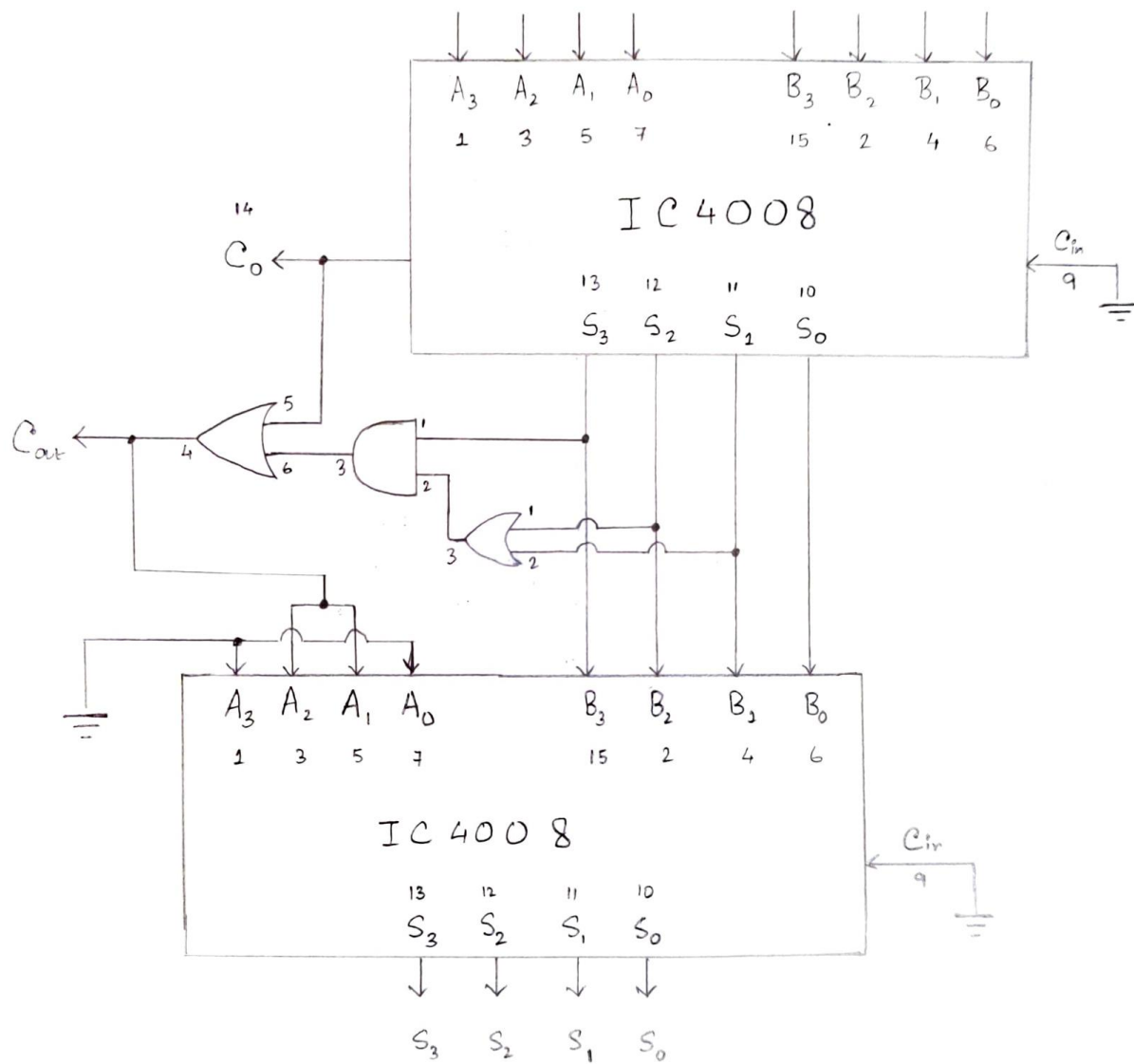
K-map for BCD Adder:

$S_3' S_2' \backslash S_1' S_0'$		$S_1' S_0'$			
		00	01	11	10
00	00	0	1	3	2
01	01	4	5	7	6
11	11	12	13	15	14
10	10	8	9	11	10

$$C_{out} = C_0 + S_3' \cdot S_2' + S_3' \cdot S_1'$$

$$C_{out} = C_0 + S_3' \cdot (S_2' + S_1')$$

Circuit Diagram:



Circuit Diagram of BCD Adder

Truth Table:

Input								Output				
A ₃	A ₂	A ₁	A ₀	B ₃	B ₂	B ₁	B ₀	C _{out}	S ₃	S ₂	S ₁	S ₀
0	0	1	1	0	0	1	0	0	0	1	0	1
0	0	1	0	0	1	0	0	0	0	1	1	0
1	0	1	0	0	1	0	1	1	0	1	0	1
0	1	1	0	1	1	0	0	1	1	0	0	0

Conclusion:

BCD adder circuit was made and truth table was verified.