University of Engineering & Management, Kolkata

Subject Name: Computer Organization & Architecture Laboratory

Subject Code: PCCCS492

ASSIGNMENT – 7

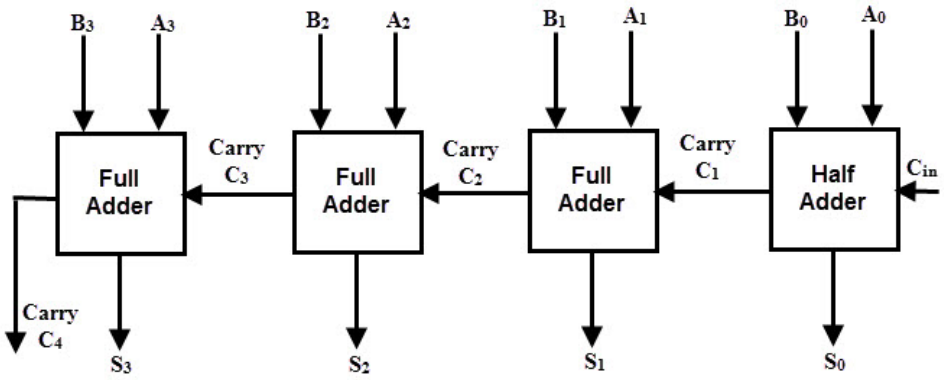
7.1. TITLE: Implementation of 4-bit carry propagation adder in VHDL (Behavioral Model).

7.2. APPARATUS REQUIRED:

a. ModelSim software.

7.3. THEORY:

A parallel adder, is a combination of multiple full adders and is used for adding all bits of the two numbers simultaneously. By connecting 'n' number of full adders in parallel, an n-bit parallel adder can be constructed. The following figure shows a parallel 4-bit binary adder, which has four full adder. The two binary numbers to be added are 'A3 A2 A1 A0' and 'B3 B2 B1 B0', which are applied to the corresponding inputs of the full adders. This parallel adder produces their result as 'C4 S3 S2 S1 S0', where C4 is the final carry.



In the 4 bit adder, first block is a full-adder that has three inputs as A0 B0 C0 (Cin) and produces a sum S0 and a carry bit C1. Next three blocks should also be full adders, as there are three inputs applied to them (two main binary bits and a Carry bit from the previous stage).

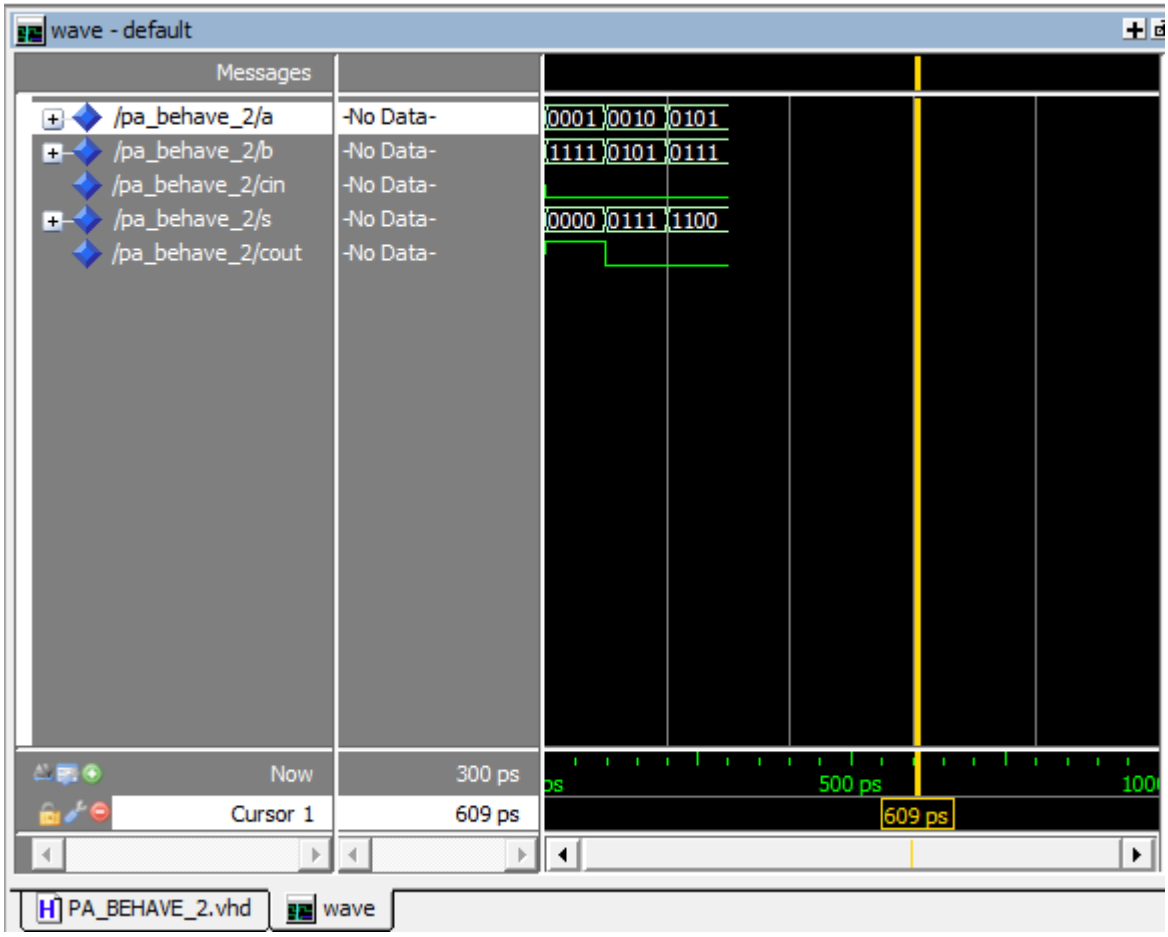
Hence, the second block full adder produces a sum S1 and a carry C2. This will be followed by other two full adders and thus the final result is C4 S3 S2 S1 S0.

7.4. VHDL CODE:

7.4.1. Behavioral Model:

```
library IEEE;
use IEEE.STD_LOGIC_1164.ALL;
use IEEE.STD_LOGIC_ARITH.ALL;
use IEEE.STD_LOGIC_UNSIGNED.ALL;

entity PA_BEHAVE_2 is
   Port ( a : in std_logic_vector(3 downto 0);
          b : in std_logic_vector(3 downto 0);
          cin : in std_logic;
          s : out std_logic_vector(3 downto 0);
          cout : out std_logic);
end PA_BEHAVE_2;

architecture BEHAVIOURAL of PA_BEHAVE_2 is

begin

process(a,b,cin)

variable u:std_logic_vector(4 downto 0);

begin

u(0):='0';

for i in 0 to 3 loop
s(i)<=a(i) xor b(i) xor u(i);
u(i+1):=(a(i) and b(i))or(b(i) and u(i)) or(u(i) and a(i));
end loop;

cout<=u(4);

end process;

end BEHAVIOURAL;
```

7.4.2. Testbench waveform:



7.5. PROCEDURE:

I. Create a new project in ModelSim platform.
II. Create a new file under this project.
III. Write the VHDL code in the editor window.
IV. Save and compile the written code.
V. Simulate the code and generate the testbench waveform.

7.6. CONCLUSION: