

Objective : Realization of all types of basic gates & universal gates using IC 4000 <sub>501, 40</sub>.

Theory : OR  $\rightarrow$  The OR gate produces the output 1, if the input A or B <sup>or</sup> both inputs are 1, otherwise the output is 0.

AND  $\rightarrow$  The AND gate produces the output 1, if the input A and input B both equals to 1, otherwise the output is 0.

NOT  $\rightarrow$  The NOT gate, produce output 1 if the single input A is equal to 0.

XOR  $\rightarrow$  The output of the XOR gate is 1, if any input is 1, but excludes the combination when both inputs are 1.

NOR  $\rightarrow$  The NOR gate or NOT-OR gate produces the output 0, if input A or B or both inputs are 1, otherwise the output is 1.

NAND  $\rightarrow$  The NAND gate or NOT-AND gate produces the output 0 if the input A and input B, both the inputs are 1, otherwise the output is 1.

### Components Required :

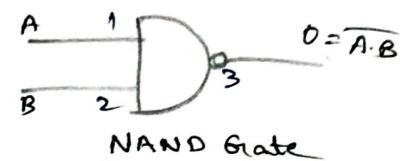
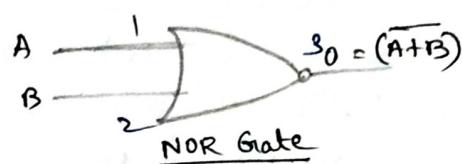
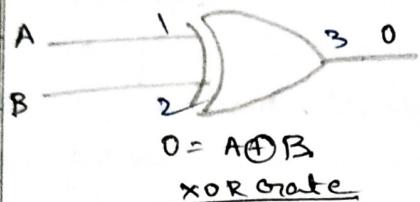
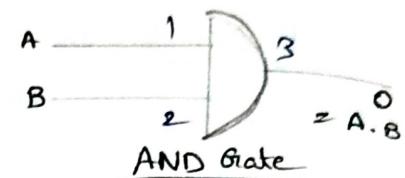
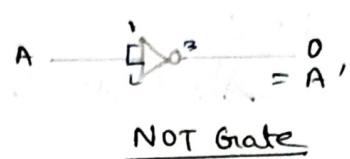
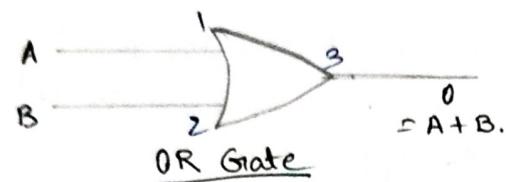
SL.No.	Item.	Specification.	Qty.
1.	NOR gate	IC - 4001	1
2.	NAND gate	IC - 4011	1
3.	XOR gate	IC - 4070	1
4.	OR gate	IC - 4071	1
5.	AND gate	IC - 4081	1
6.	NOT gate	IC - 4069	1.

### TRUTH TABLE :

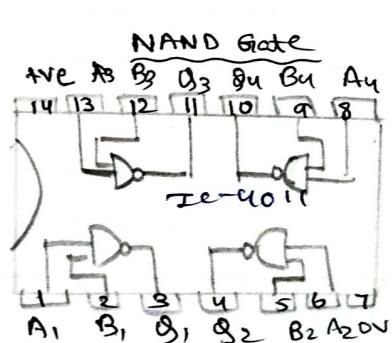
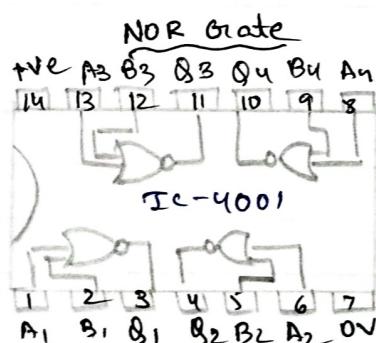
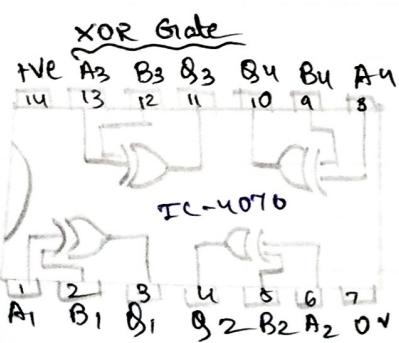
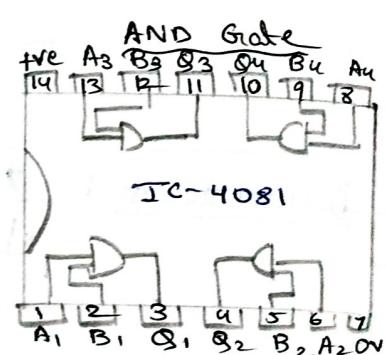
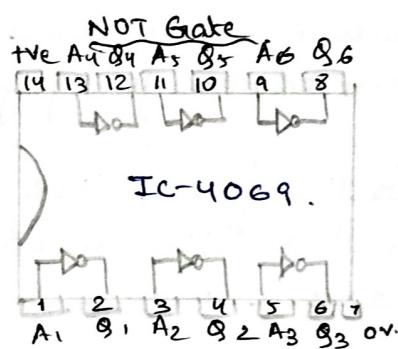
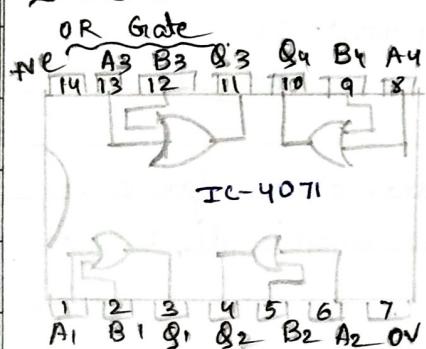
<u>AND Gate</u>		<u>OR Gate</u>		<u>NOR Gate</u>		<u>XOR Gate</u>		<u>NOT Gate</u>		<u>NAND Gate</u>	
A	B	$O = A \cdot B$	A	B	$O = A + B$	A	B	$O = A \oplus B = (A+B)'$	A	B	$O = A \bar{B}$
0	0	0	0	0	0	0	0	1	0	1	0
0	1	0	1	0	1	1	0	1	1	0	1
1	0	0	1	1	1	0	1	0	0	0	1
1	1	1	1	1	0	1	1	0	1	0	0

Teacher's Signature \_\_\_\_\_

## CIRCUIT DIAGRAM :



## PIN DIAGRAM :



Realization of Basic Gates using Universal GatesTRUTH TABLESOR Gate (using NOR)

A	B	$A+B$	$(A+B)'$	$O = ((A+B)' + (A+B)')'$
0	0	0	1	0
0	1	1	0	1
1	0	1	0	1
1	1	1	0	1

Using NORAND Gate (using NOR)

A	B	$A+A$	$B+B$	$A'B' (A+B)'$	$(A+B)'$	$O = A \cdot B$
0	0	0	0	1	1	0
0	1	1	0	1	0	0
1	0	0	1	0	1	0
1	1	1	1	0	0	1

XOR (using NOR)

A	B	$A$	$A'$	$B$	$B'$	$A \oplus B$
0	0	1	1	0	0	0
0	1	1	0	0	1	1
1	0	0	1	1	0	1
1	1	0	0	0	0	0

NOT Gate (using NOR)

A	$A+A$	$O = (A+A)'$	$= A'$
0	0	1	1
1	1	0	0

OR Gate (using NAND)

A	B	$(A \cdot A)'$	$(B \cdot B)'$	$O = A \cdot B' = A+B$
0	0	1	1	0
0	1	1	0	1
1	0	0	1	1
1	1	0	0	1

AND Gate (using NAND)

A	B	$(A \cdot B)'$	$O = ((A \cdot B)')' = A \cdot B$
0	0	1	0
0	1	1	0
1	0	1	0
1	1	0	1

XOR (using NAND)

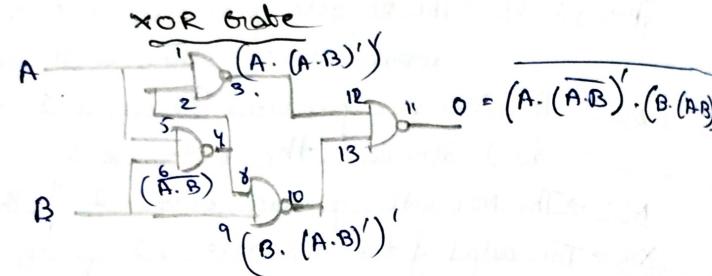
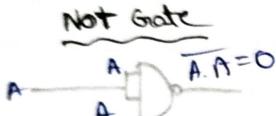
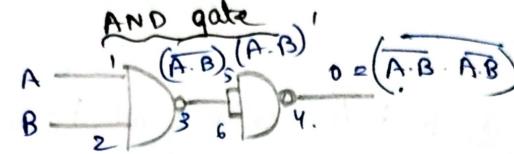
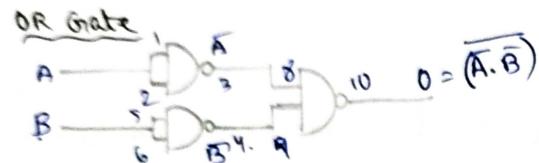
A	B	$(A \cdot B)'$	$((A \cdot (A \cdot B))')'$	$((B \cdot (A \cdot B))')'$	$O = A \oplus B$
0	0	1	1	1	0
0	1	1	1	0	1
1	0	1	0	1	1
1	1	0	0	0	0

NOT (using NAND)

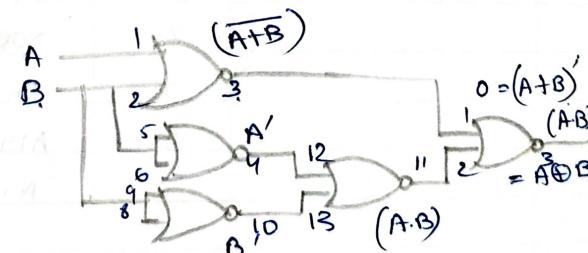
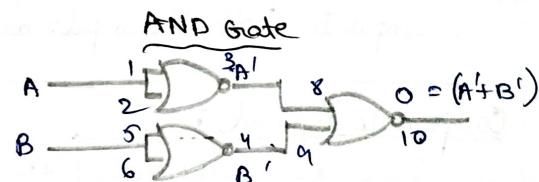
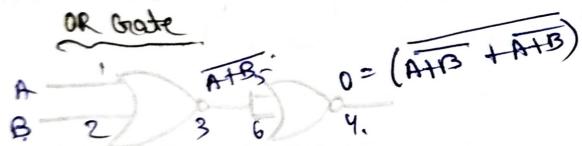
A	$A \cdot A$	$O = (A \cdot A)'$
0	0	1
1	1	0

## CIRCUIT DIAGRAMS

## Using NAND gate



## Using NOR Gate



**vivo Y100A**  
Anwesha

Objective : Realization of Half Adder & Subtractor using universal gates.

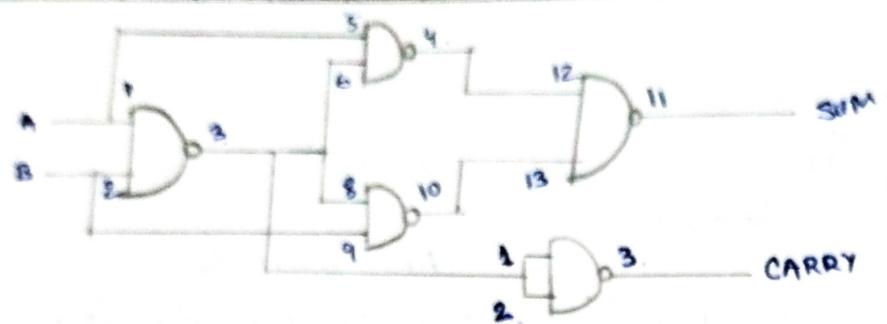
Truth Table

Input		Output	
A	B	$S = A \oplus B$	$C = A \cdot B$
0	0	0	0
0	1	1	0
1	0	1	0
1	1	0	1

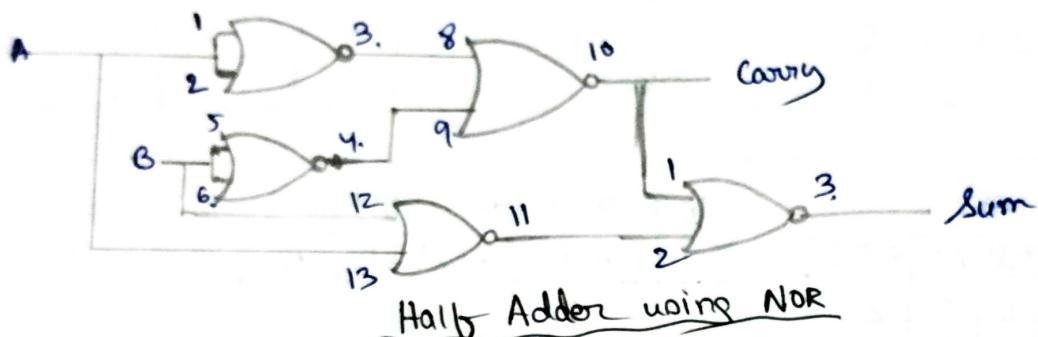
Objective : Realization of Half Subtractor using Universal gates.

Truth Table

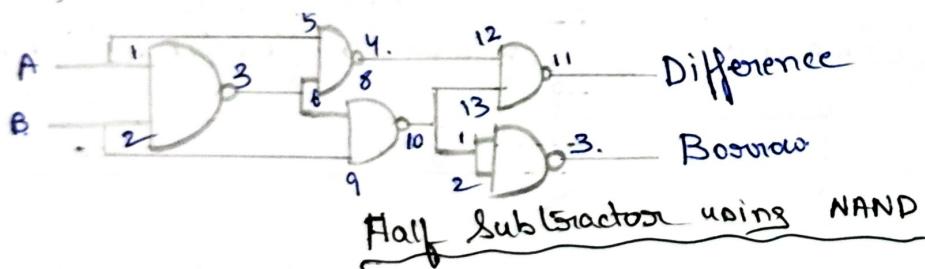
Input		Output	
A	B	$D = A \oplus B$	$B = A \cdot B$
0	0	0	0
0	1	1	1
1	0	1	0
1	1	0	0



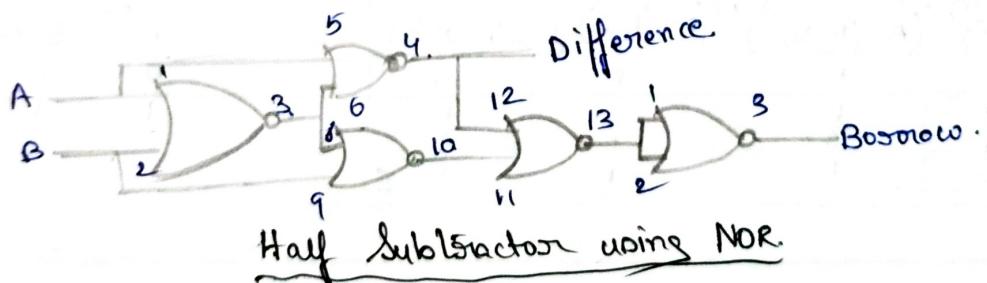
Half Adder using NAND.



Half Adder using NOR.



Half Subtractor using NAND



Half Subtractor using NOR.

Objective: Realization of Full Adder using Universal gate.

Truth Table:

Input			Output	
A	B	C	Sum = A ⊕ B ⊕ C	Carry = A · B + (A ⊕ B) · C
0	0	0	0	0
0	0	1	1	0
0	1	0	1	0
0	1	1	0	1
1	0	0	1	0
1	0	1	0	1
1	1	0	0	1
1	1	1	1	1

Objective: Realization of Full Subtractor using Universal Gate.

Truth Table:

Input			Output	
A	B	C	D = A ⊕ B ⊕ C	B = AB + BC + AC
0	0	0	0	0
0	0	1	1	1
0	1	0	1	1
0	1	1	0	1
1	0	0	1	0
1	0	1	0	0
1	1	0	0	0
1	1	1	1	1

