University of Engineering & Management, Kolkata

Subject Name: Computer Organization & Architecture Laboratory

Subject Code: PCCCS492

ASSIGNMENT – 5

5.1.TITLE: Implementation of AND gate, OR gate and XOR gate using VHDL (Dataflow Model).

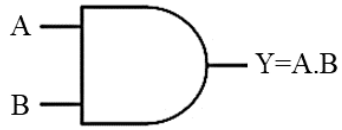
5.2. APPARATUS REQUIRED:

a. ModelSim software.

5.3. THEORY:

5.3.1. AND gate: The AND gate performs a logical multiplication commonly known as AND function. The output is high when both the inputs are high. The output is low level when any one of the inputs is low. 7408 is the two Inputs AND gate IC. A & B are the Input terminals & Y is the Output terminal. Its logical equation is, Y = A.B.

Symbol:



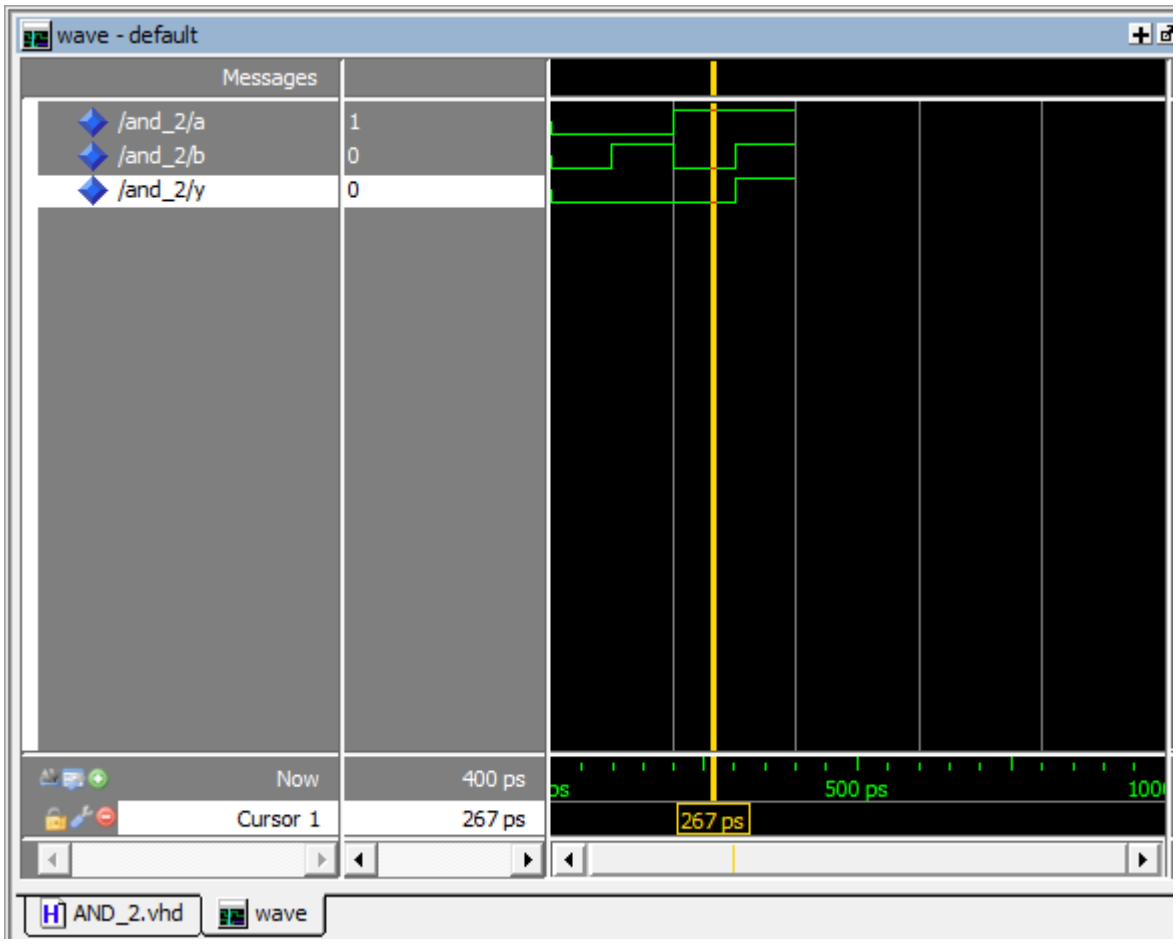
Truth table:

Input		Output
A	**B**	**Y**
0	0	0
0	1	0
1	0	0
1	1	1

VHDL code:

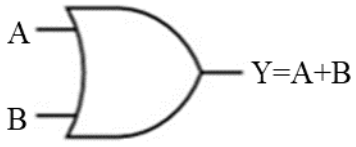
```
library IEEE;
use IEEE.std_logic_1164.all;

-- Entity declaration

entity AND_2 is

    port(A : in std_logic;      -- AND gate input
         B : in std_logic;      -- AND gate input
         Y : out std_logic);    -- AND gate output

end AND_2;

-- Dataflow Modelling Style
-- Architecture definition

architecture DATAFLOW of AND_2 is

 begin

    Y <= A AND B;

end DATAFLOW;
```

Testbench waveform:



5.3.2. OR gate: The OR gate performs a logical addition commonly known as OR function. The output is high when any one of the inputs is high. The output is low level when both the inputs are low. 7432 is the two Input OR gate IC. A & B is the input terminals & Y is the Output terminal. Its logical equation is, Y = A + B.

Symbol:



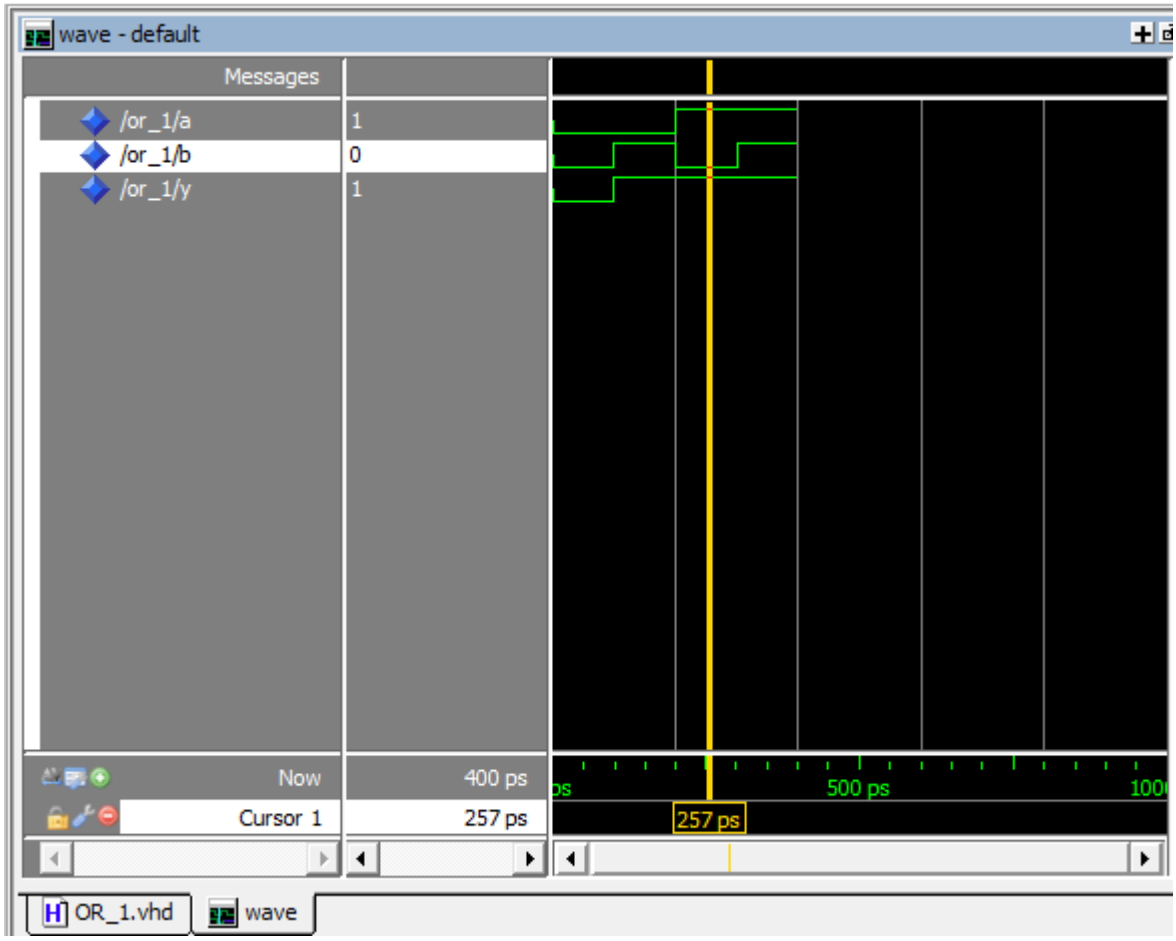
Truth table:

Input		Output
A	**B**	**Y**
0	0	0
0	1	1
1	0	1
1	1	1

VHDL code:

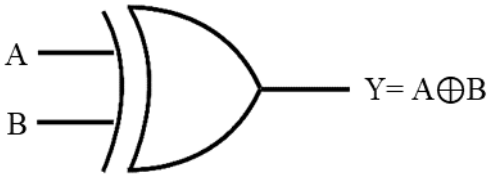
```
library IEEE;
use IEEE.std_logic_1164.all;

-- Entity declaration

entity OR_1 is

    port(A : in std_logic;      -- AND gate input
         B : in std_logic;      -- AND gate input
         Y : out std_logic);    -- AND gate output

end OR_1;

-- Dataflow Modelling Style
-- Architecture definition

architecture DATAFLOW of OR_1 is

 begin

    Y <= A OR B;

end DATAFLOW;
```

Testbench waveform:



5.3.3. XOR gate: XOR gate is not a basic gate. XOR operation can be performed using basic gates. Output of XOR gate is high when any one of the inputs is high. The output is low when both the inputs are low and both the inputs are high. The IC no. for XOR gate is 7486. Its logical equation is, Y= A⊕B.

Symbol:



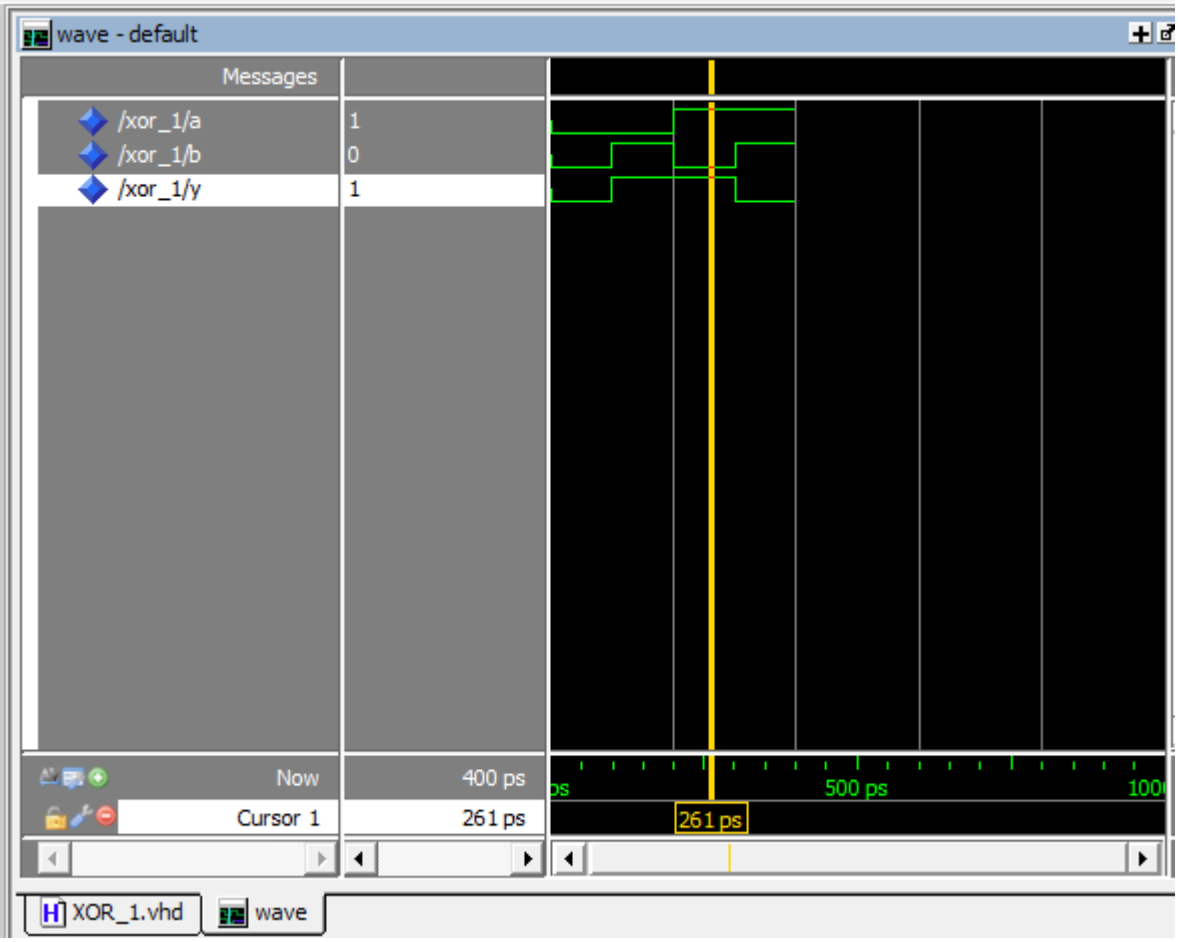
Truth table:

Input		Output
A	**B**	**Y**
0	0	0
0	1	1
1	0	1
1	1	0

VHDL code:

```
library IEEE;
use IEEE.std_logic_1164.all;

-- Entity declaration

entity XOR_1 is

    port(A : in std_logic;      -- AND gate input
         B : in std_logic;      -- AND gate input
         Y : out std_logic);    -- AND gate output

end XOR_1;

-- Dataflow Modelling Style
-- Architecture definition

architecture DATAFLOW of XOR_1 is

 begin

    Y <= A XOR B;

end DATAFLOW;
```

Testbench waveform:



5.4. PROCEDURE:

I. Create a new project in ModelSim platform.
II. Create a new file under this project.
III. Write the VHDL code in the editor window.
IV. Save and compile the written code.
V. Simulate the code and generate the testbench waveform.

5.5. CONCLUSION: