

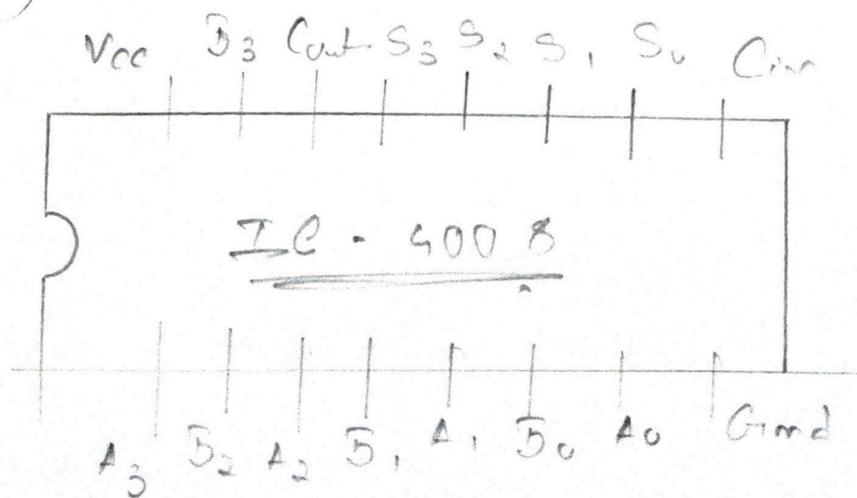
# Experiment No : 01

• Title : Verification of adder (IC - 4008) & realization of an adder subtractor composite unit using the IC.

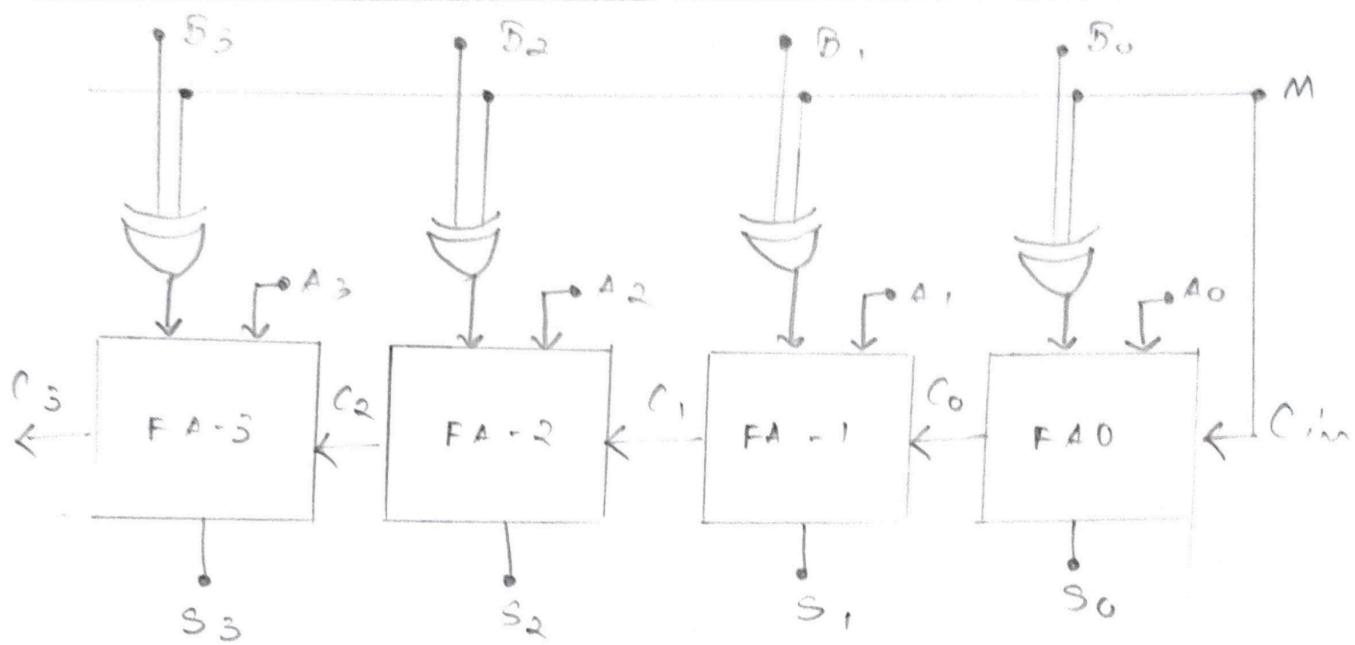
- Objective : To verify the working of IC - 4008 & then implement a adder - subtractor composite unit using it.
- Components :

Component	Specification	Quantity
1> IC - 4008	IC - 4008	01
2> XOR gates	IC - 9	01
3> Comm. Wires	—	as per req.
4> Breadboard	—	01
5> GND & VCC	+5V	—

- Pin diagram of IC :



- SD of adder-subtractor composite circuit!



- Truth Table / Observation Table : i. For Adder

- For subtraction configuration

Cin	A <sub>3</sub>	A <sub>2</sub>	A <sub>1</sub>	A <sub>0</sub>	B <sub>3</sub>	B <sub>2</sub>	B <sub>1</sub>	B <sub>0</sub>	S <sub>3</sub>	S <sub>2</sub>	S <sub>1</sub>	S <sub>0</sub>	Count	
1	0	0	0	0	0	0	0	0	0	0	0	0	0	0
1	0	0	0	1	0	0	0	1	0	0	0	0	0	0
1	0	0	1	0	0	0	1	0	0	0	0	0	0	0
1	0	0	1	1	0	0	1	1	0	0	0	0	0	0
1	0	1	0	0	0	1	0	0	0	0	0	0	0	0
1	0	1	0	1	0	1	0	1	0	0	0	0	0	0
1	0	1	1	0	0	1	1	1	0	0	0	0	0	0
1	0	1	1	1	0	1	1	1	1	0	0	0	0	0
1	1	0	0	0	1	0	0	0	0	0	0	0	0	0
1	1	0	0	1	1	0	0	1	0	0	0	0	0	0
1	1	0	1	0	1	0	1	0	0	0	0	0	0	0
1	1	0	1	1	1	0	1	1	0	0	0	0	0	0
1	1	1	0	0	1	1	0	0	0	0	0	0	0	0
1	1	1	0	1	1	1	0	1	0	0	0	0	0	0
1	1	1	1	0	1	1	1	0	0	0	0	0	0	0
1	1	1	1	1	1	1	1	1	0	0	0	0	0	0

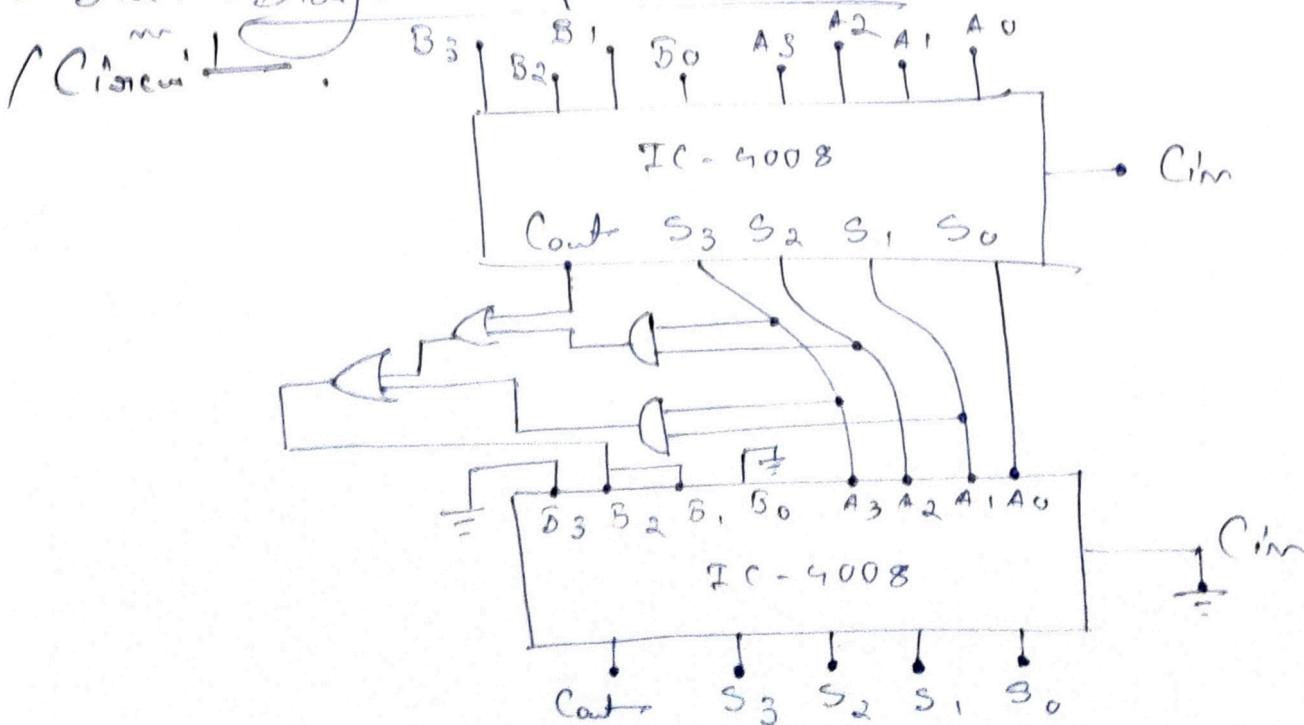
- Conclusion: The adder IC - 4008 is successfully verified & implementation of adder subtractor composite circuit using it has been performed.

- Experiment No : 02
- Title : Realization of a BCD adder circuit using the adder IC = 4008
- Objective : To implement a BCD adder circuit using IC = 4008.

• Component Table :

SI No.	Component Name	Specification	Ref.
01	IC = 4008 adder	IC = 4008	0 2
02	AND gate	IC = 4081	0 1
03	OR gate	IC = 4081	0 1
04	Com. resist	=	As reqd.
05	Bread board	-	"
06	Power	$\pm 5V$	"

• Block Diagram of the circuit :



Theory:

Input to the  $B_1$  &  $B_2$  to the 2nd adder IC be  $\Sigma$ .

$$\therefore \Sigma = \underline{\text{Carry}} + S_3 S_2 + S_3 S_1$$

Truth table / observation table:

Dec	B <sub>1</sub> in					BCD				
	C <sub>0</sub>	S <sub>3</sub>	S <sub>2</sub>	S <sub>1</sub>	S <sub>0</sub>	C <sub>0</sub>	S <sub>3</sub>	S <sub>2</sub>	S <sub>1</sub>	S <sub>0</sub>
0	0	0	0	0	0	0	0	0	0	0
1	0	0	0	0	1	0	0	0	0	1
2	0	0	0	1	0	0	0	0	1	0
3	0	0	0	1	1	0	0	0	1	1
4	0	0	1	0	0	0	0	1	0	0
5	0	0	1	0	1	0	0	1	0	1
6	0	0	1	1	0	0	0	1	1	0
7	0	0	1	1	1	0	0	1	1	1
8	0	1	0	0	0	0	1	0	0	0
9	0	1	0	0	1	0	1	0	0	1
10	0	1	0	1	0	1	0	0	0	1
11	0	1	0	1	1	1	0	0	1	0
12	0	1	1	0	0	1	0	0	1	0
13	0	1	1	0	1	1	0	0	1	1
14	0	1	1	1	0	1	0	1	0	1
15	0	1	1	1	1	1	0	1	1	0
16	1	0	0	0	0	1	0	1	1	1
17	1	0	0	0	1	1	0	1	1	1

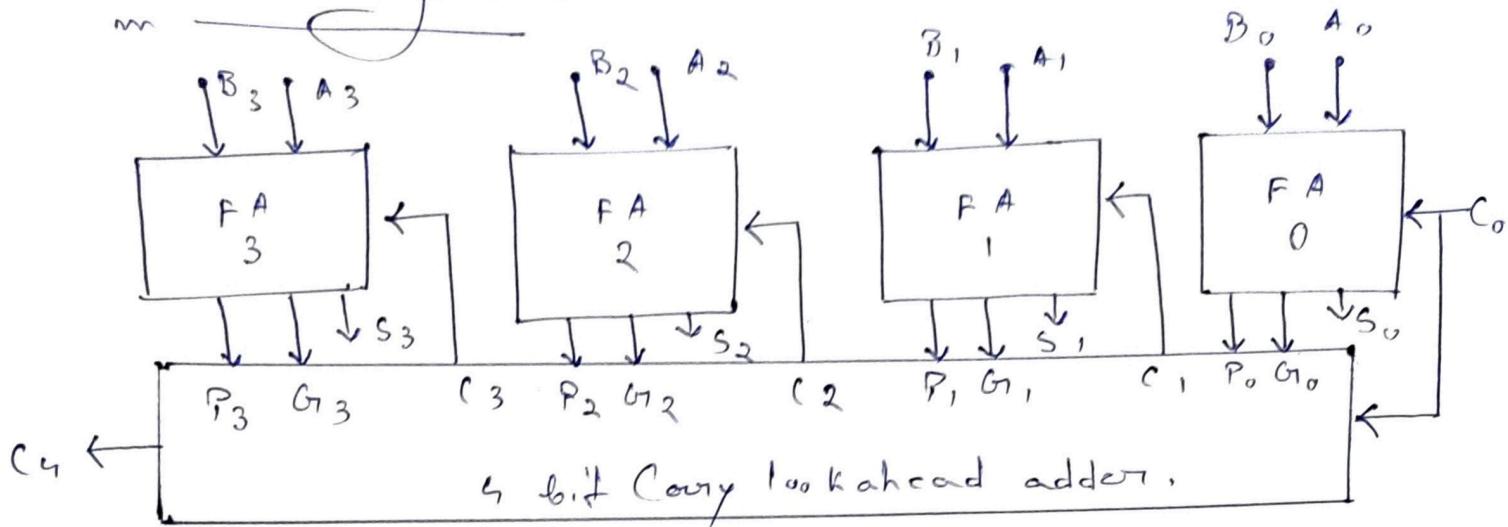
- Conclusion: A BCD adder circuit using IC - 4008 is successfully implemented & the truth table has been verified.

## Experiment No : 03

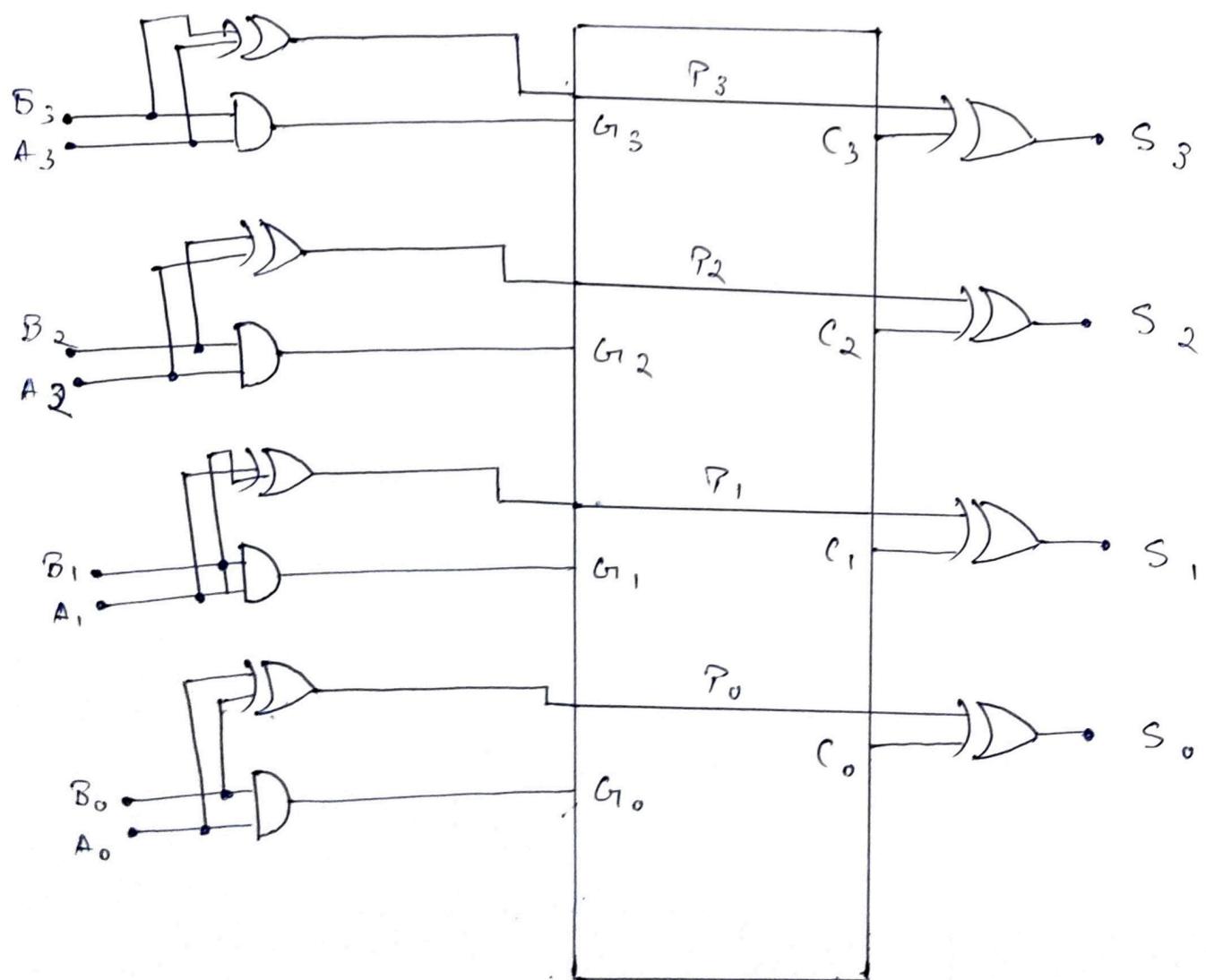
- Title : Designing a 4 bit carry look-ahead adder circuit using adder IC.
- Objective : To design a 4 bit carry look-ahead adder circuit using adder IC - 4008 & also to record the experiment results.
- Components Required :

<u>S.I No.,</u>	<u>Component</u>	<u>Specification</u>	<u>Qty</u>
01	AND gate	IC - 4081	0 1
02	XOR gate	IC - 4070	0 2
03	Adder	IC - 4008	0 1
04	Bread-board	-	0 1
05	Com. wires	-	as req.
06	Power & GND	± 5 V	"

• Block - Diagram:



• Circuit - Diagram:



• Theory:

A / B / C	Out	
0 0 0	0	No carry generation
0 0 1	0	
0 1 0	0	Carry Propagation
0 1 1	1	
1 0 0	0	
1 0 1	1	Carry generation
1 1 0	1	
1 1 1	1	

$$\begin{aligned}
 C_{i+1} &= P_i C_i + G_i \\
 &= (A_i \oplus B_i), C_i + A_i \cdot B_i
 \end{aligned}$$

$$\therefore C_1 = P_0 C_0 + G_0$$

$$\therefore C_2 = P_1 C_1 + G_1 = P_1 P_0 C_0 + P_1 G_0 + G_1$$

$$\therefore C_3 = P_2 C_2 + G_2$$

$$= P_2 P_1 P_0 C_0 + P_2 P_1 G_0 + P_2 G_1 + G_2$$

- Observation table :

Cin / A / B

Cin	A	B	Sum	Carry
	$A_3/A_2/A_1/A_0$	$B_3/B_2/B_1/B_0$	$S_3/S_2/S_1/S_0$	
0	0 0 1 0	0 0 1 0	0 1 0 0	0
0	0 1 1 0	0 1 1 0	1 1 0 0	0
0	1 0 1 1	1 0 1 1	0 1 1 0	1
0	1 1 1 0	1 1 1 1	1 1 0 1	1

- Conclusion : A Carry look ahead adder has been successfully implemented using adder IC & other required logic gates & the experiment results are recorded.

## Experiment no: 084

- Title: Designing of an ALU model using multiplexer IC - 4539B ,
- Objectives: To implement a logic ALU model using ZC - 4539B & verify the output .

- Component table:

SI no.	Component	Specification	Ref.
01	AND gate	IC - 4081	01
02	OR gate	IC - 4071	01
03	NOT gate	IC - 4069	01
04	XOR gate	IC - 4070	01
05	Half adder	IC - 4008	01
06	Half sub.	IC - 4008	01
07	MUX	IC - 4539B	01 of ref.
08	Bread-board	—	a
09	Components	—	a
10	Vcc & GND	$\pm 5V$	a

Theory:

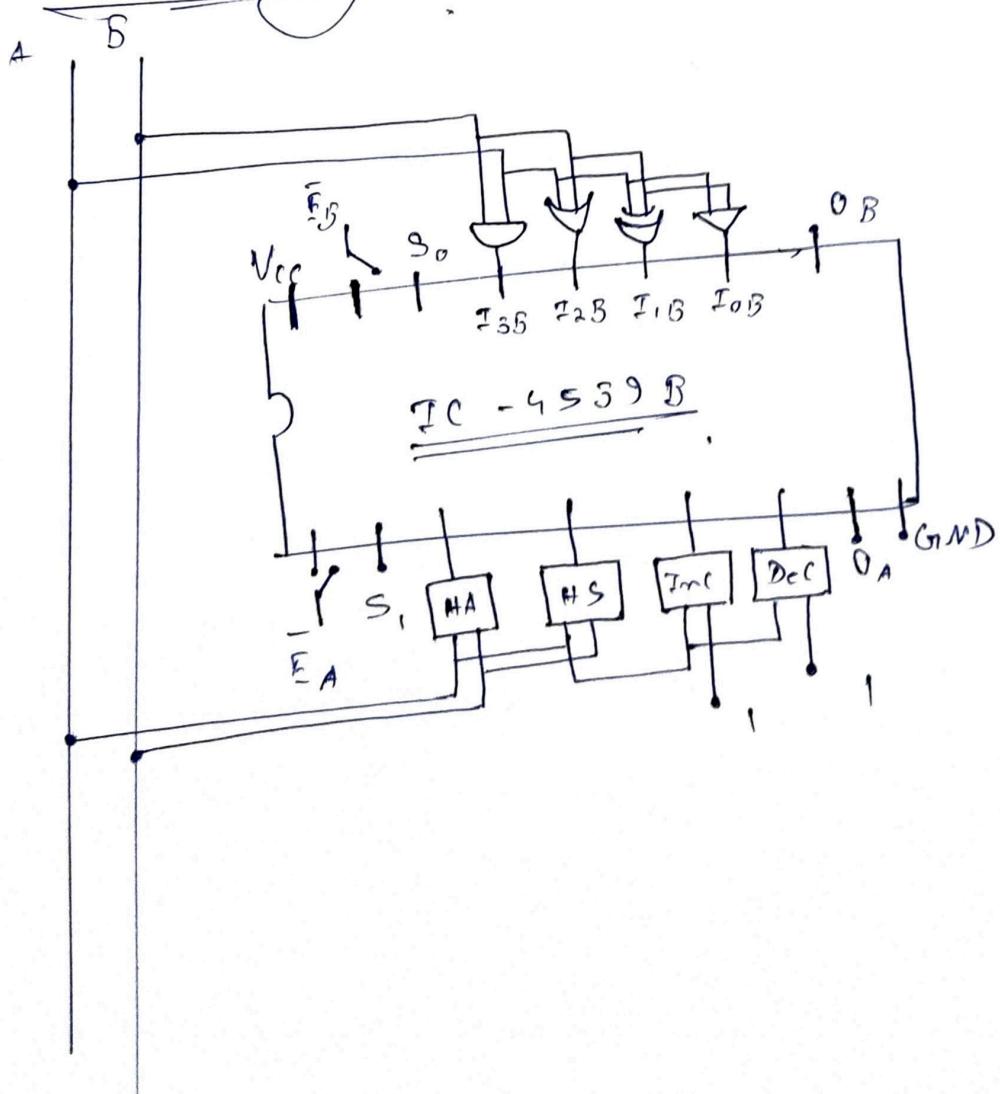
Arithmetic (MUX A)  
operations

- $I_3A : A + D$  (Half add)
- $I_2A : A - B$  (Half sub)
- $I_3A : A + 1$  (Half add)
- $I_0A : A - 1$  (Half sub)

Logical (MUX B)  
operations

- $I_3B : \text{AND}$
- $I_2B : \text{OR}$
- $I_1B : \text{xOR}$
- $I_0B : \text{NOT}$

Circuit Diagram:



- Observation table:

↳ for arithmetic configuration :

$s_1$	$s_0$	$0_A$
0	0	$I_{0A}$ (Adding $A \oplus B$ )
0	1	$I_{1A}$ (Incrementing $A$ )
1	0	$I_{2A}$ (Subtracting $A \otimes B$ )
1	1	$I_{3A}$ (Decrementing $A$ )

↳ for logical configuration :

$s_1$	$s_0$	$0_B$
0	0	$I_{0B}$ (Complement)
0	1	$I_{1B}$ ( $\neg A$ )
1	0	$I_{2B}$ ( $A$ )
1	1	$I_{3B}$ (AND operation)

- Conclusion: An ALU model capable of performing logic arithmetic & logical operation has been successfully implemented using mux & other gates & the observation is recorded.

# Experiment : 05

- Title : Designing of a 4 bit Carry Save adder using adder IC
- Objective : To implement a 4 bit carry save adder using IC - 4008 & other logic gates to verify the results.
- Components Required :

<u>S.I No.</u>	<u>Component</u>	<u>Specification</u>	<u>Qty.</u>
01	AND gate IC	IC - 4081	01
02	XOR gate IC	IC - 4070	01
03	IC - Adder (RCA)	IC - 4008	01
04	Conn. wires	-	As required
05	BreadBoard	-	01
06	Power supply 8 VND	± 5 V	As required

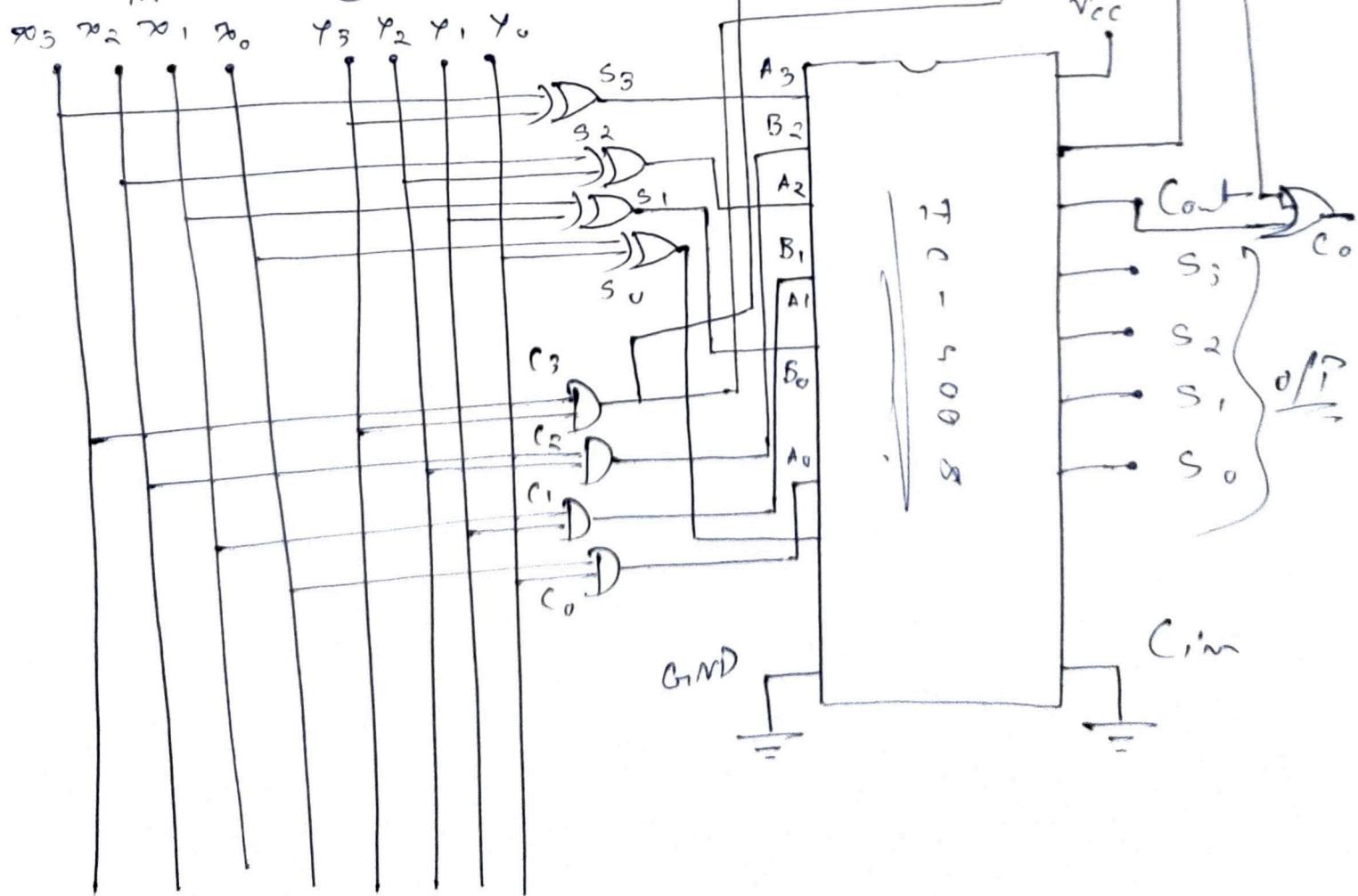
Theory: Adding  $x_3 x_2 x_1 x_0$  with  $y_3 y_2 y_1 y_0$ .

$$\begin{array}{l|l} s_3 = x_3 \oplus y_3 & c_3 = x_3 \cdot y_3 \\ s_2 = x_2 \oplus y_2 & c_2 = x_2 \cdot y_2 \\ s_1 = x_1 \oplus y_1 & c_1 = x_1 \cdot y_1 \\ s_0 = x_0 \oplus y_0 & c_0 = x_0 \cdot y_0 \end{array}$$

For IC - 4008:  $C_{in} = \text{AND}$ .

$$\begin{array}{l|l} c_3 \rightarrow b_3 & s_3 \rightarrow a_3 \\ c_2 \rightarrow b_2 & s_2 \rightarrow a_2 \\ c_1 \rightarrow b_1 & s_1 \rightarrow a_1 \\ c_0 \rightarrow b_0 & s_0 \rightarrow a_0 \end{array}$$

Circuit Diagram:



- Observation table:

$x_3/x_2/x_1/x_0$	$y_3/y_2/y_1/y_0$	$s_3/s_2/s_1/s_0$	Cot
0 1 1 0	1 0 0 0	1 1 1 0	0
0 1 0 0	0 0 0 1	0 1 0 1	0
0 0 1 1	0 0 1 1	0 1 1 0	0
1 0 1 0	1 0 0 1	0 0 1 1	1

- Conclusion:

A 4 bit carry save adder (CSA) has been successfully implemented using adder (IC-4008) & other logic gates & the output is observed & verified.