University of Engineering & Management, Kolkata

Subject Name: Computer Organization & Architecture Laboratory

Subject Code: PCCCS492

ASSIGNMENT – 6

6.1. TITLE: Implementation of Full Adder using VHDL (Dataflow and Behavioral Model).

6.2. APPARATUS REQUIRED:

a. ModelSim software.

6.3. THEORY:

A full adder adds binary numbers and accounts for values carried in as well as out. A one-bit full adder adds three one-bit numbers, often written as A, B, and C_{in}; A and B are the operands, and C_{in} is a bit carried in from the previous less-significant stage. The circuit produces a two-bit output such as sum (S) and carry (C_{out}).

6.3.1. TRUTH TABLE FOR FULL ADDER:

Input			Output	
A	**B**	**C_{in}**	**S**	**C_{out}**
0	0	0	0	0
0	0	1	1	0
0	1	0	1	0
0	1	1	0	1
1	0	0	1	0
1	0	1	0	1
1	1	0	0	1
1	1	1	1	1

6.3.2. K-MAP FOR SUM AND CARRY FOR FULL ADDER:

K-Map for sum:

A \ BC_{in}	00	01	11	10
0	0	(1)	0	(1)
1	(1)	0	(1)	0

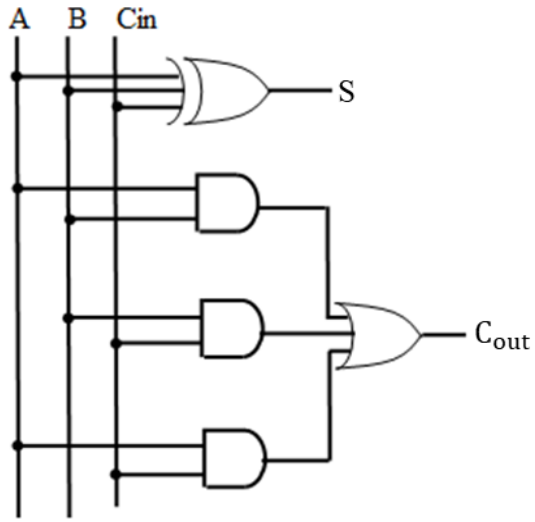
$S = A \oplus B \oplus C_{in}$

K-Map for carry:

A \ BC_{in}	00	01	11	10
0	0	0	1	0
1	0	1	1	1

$C_{out} = AB + AC_{in} + BC_{in}$

6.3.3. FULL ADDER USING BASIC GATES:



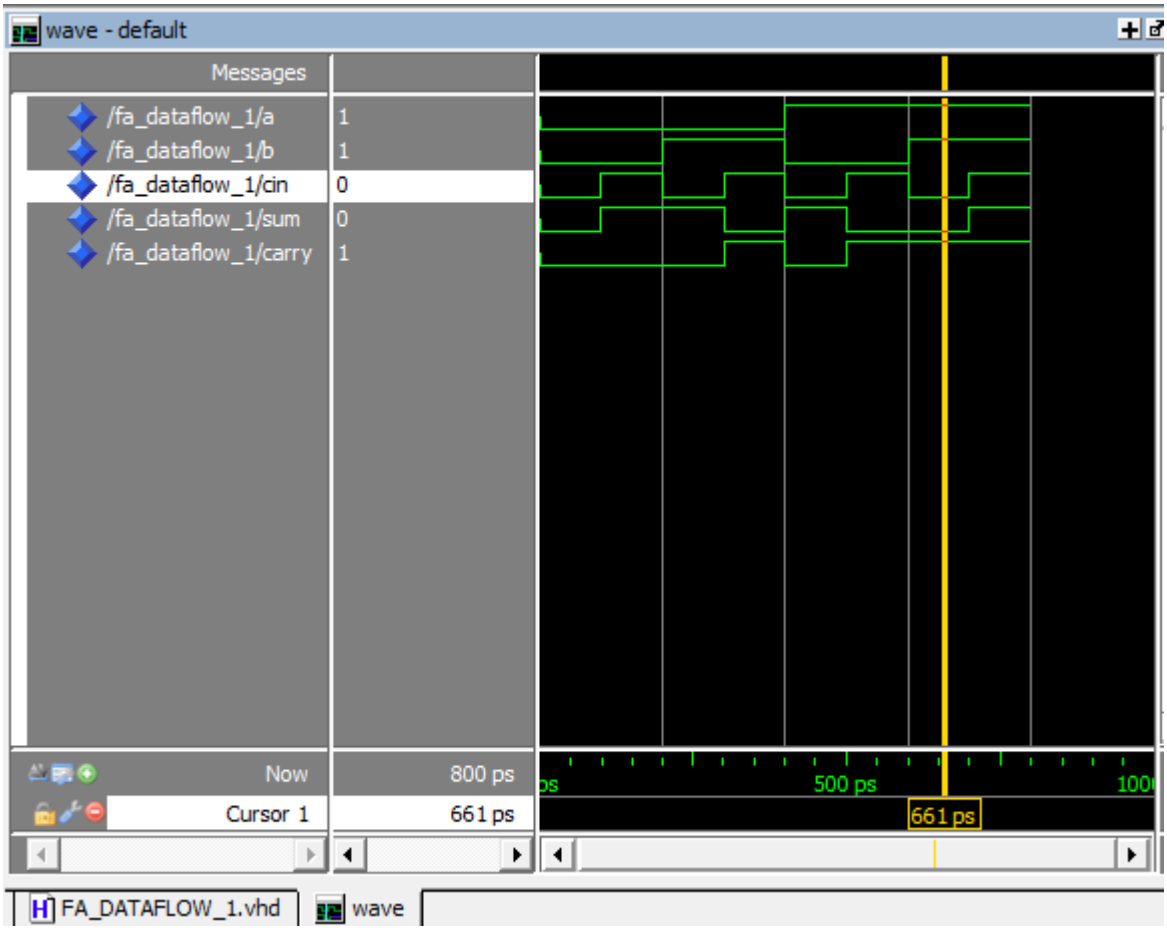
6.3.4. VHDL CODE:

6.3.4.1. Dataflow Model:

```
library IEEE;
use IEEE.std_logic_1164.all;

-- Entity declaration

entity FA_DATAFLOW_1 is

    port(A : in std_logic;      -- FA input
         B : in std_logic;      -- FA input
         CIN : in std_logic;      -- FA input
         SUM : out std_logic;    -- FA output
         CARRY : out std_logic);    -- FA output

end FA_DATAFLOW_1;

-- Dataflow Modelling Style
-- Architecture definition
```

```
architecture DATAFLOW of FA_DATAFLOW_1 is

begin

    SUM <= A XOR B XOR CIN;
    CARRY <= (A AND B) OR (A AND CIN)OR (B AND CIN);

end DATAFLOW;
```

6.3.4.2. Testbench waveform:

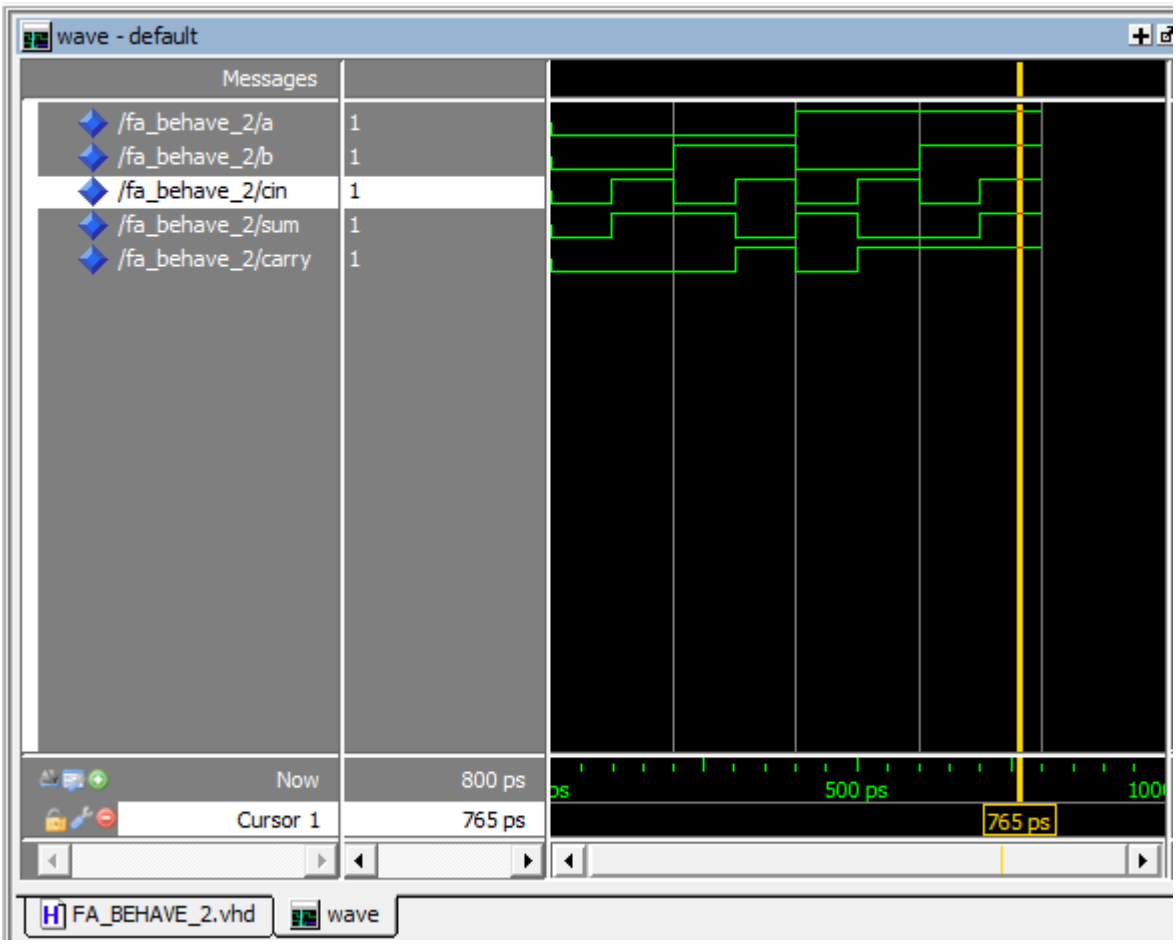


6.3.4.3. Behavioral Model:

```
library IEEE;
use IEEE.std_logic_1164.all;

-- Entity declaration

entity FA_BEHAVE_2 is

    port(A : in std_logic;      -- FA input
```

```
        B : in std_logic;      -- FA input
        CIN : in std_logic;      -- FA input
        SUM : out std_logic;    -- FA output
        CARRY : out std_logic);    -- FA output

end FA_BEHAVE_2;

-- Behavioural Modelling Style
-- Architecture definition

architecture BEHAVIOURAL of FA_BEHAVE_2 is
begin
process (A,B,CIN)
begin

if A = '0' then
    if B = '0' then
       SUM <= CIN;
       CArry <='0';

    else

        SUM <= not CIN;
        CArry <= CIN;

    end if;

else

     if B = '0' then

       SUM <= not CIN;
       CArry <= CIN;

    else

        SUM <= CIN;
       CArry <='1';

    end if;

end if;

end process;


end BEHAVIOURAL;
```

6.3.4.4. Testbench waveform:



6.4. PROCEDURE:

I. Create a new project in ModelSim platform.
II. Create a new file under this project.
III. Write the VHDL code in the editor window.
IV. Save and compile the written code.
V. Simulate the code and generate the testbench waveform.

6.5. CONCLUSION: