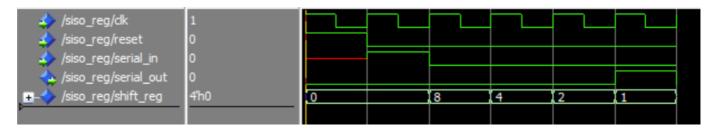
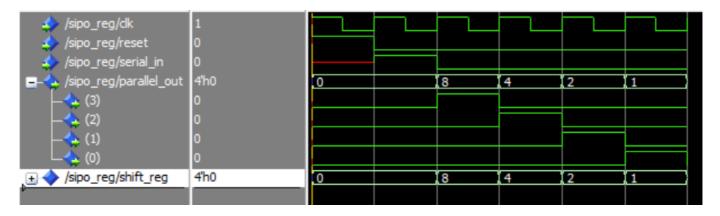
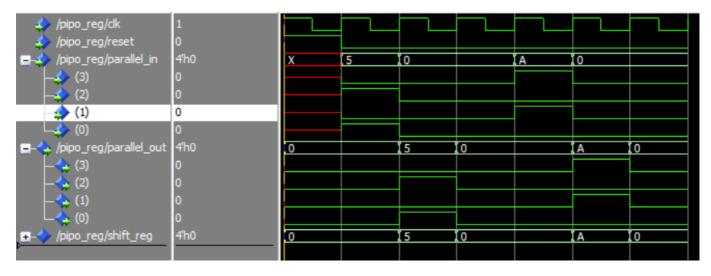
## Shift Registers VHDL Output



**SISO Shift Register** 

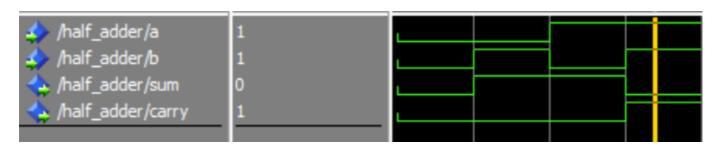


**SIPO Shift Register** 

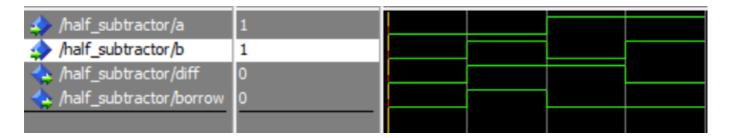


**PIPO Shift Register** 

## Adder & Subtractor VHDL Output



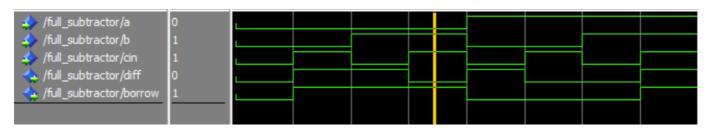
**Half Adder** 



**Half Subtractor** 

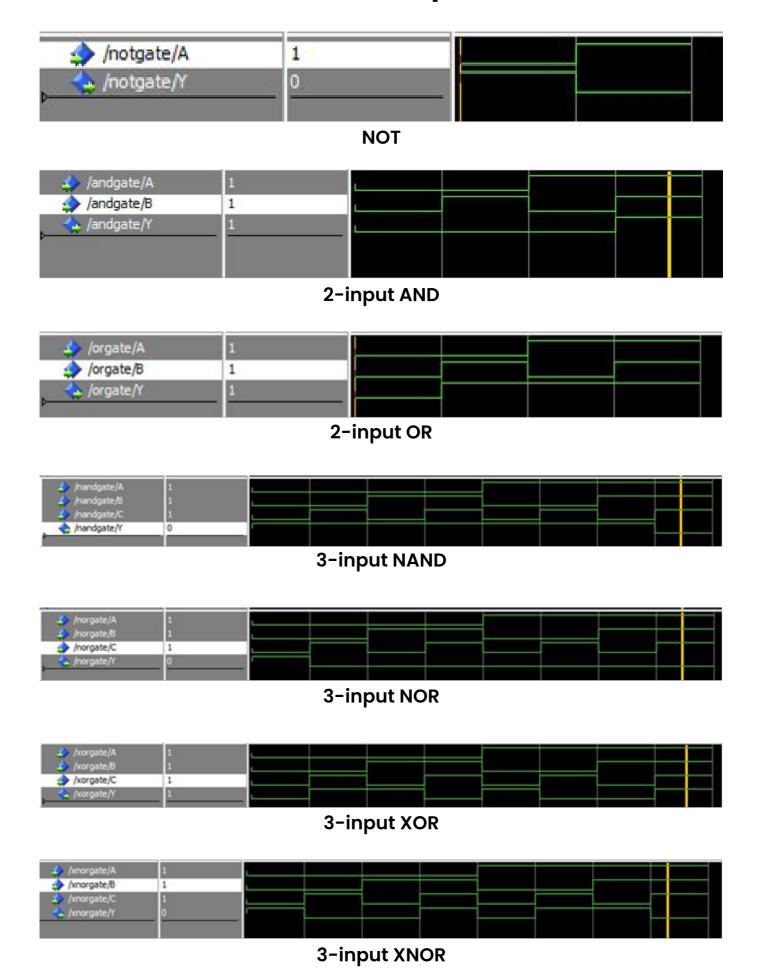


**Full Adder** 

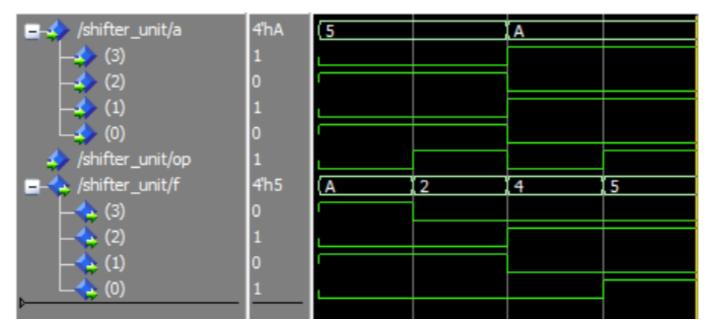


**Full Subtractor** 

## Basic Gates VHDL Output



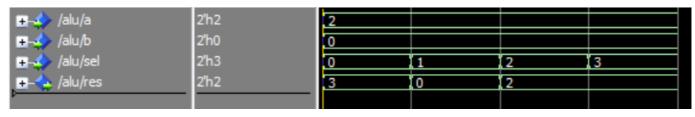
## Arithmetic Operations VHDL Output



**Shifter Unit** 



**Arithmetic Unit** 



**ALU**