University of Engineering and Management
Institute of Engineering & Management, New Town Campus
Department of Computer Science & Engineering

Computer Organization & Architecture Laboratory
PCCCS492

EXPERIMENT NO.:

TITLE: Design Register circuit.

OBJECTIVE: To design Register circuit.

THEORY: A register is a group of binary cells suitable for holding binary information. The information stored within the registers can be transferred with the help of shift registers. Shift Register is a group of flip flops used to store multiple bits of data. The bits stored in such registers can be made to move within the registers and in/out of the registers by applying clock pulses.

An n-bit shift register can be formed by connecting n flip-flops where each flip flop stores a single bit of data. The registers which will shift the bits to left are called "Shift left registers". The registers which will shift the bits to right are called "Shift right registers".

Shift registers are basically of 4 types. These are:

1. Serial In Serial Out shift register
2. Serial In parallel Out shift register
3. Parallel In Serial Out shift register

flip flops used to store multiple bits of data. The bits stored in such registers can be made to move within the registers and in/out of the registers by applying clock pulses.

An n-bit shift register can be formed by connecting n flip-flops where each flip flop stores a single bit of data. The registers which will shift the bits to left are called "Shift left registers". The registers which will shift the bits to right are called "Shift right registers".

Shift registers are basically of 4 types. These are:

1. Serial In Serial Out shift register
2. Serial In parallel Out shift register
3. Parallel In Serial Out shift register
4. Parallel In parallel Out shift register

Serial-In Serial-Out Shift Register (SISO) –

Serial-In Serial-Out Shift Register (SISO) –

The shift register, which allows serial input (one bit after the other through a single data line) and produces a serial output is known as Serial-In Serial-Out shift register. Since there is only one output, the data leaves the shift register one bit at a time in a serial pattern, thus the name Serial-In Serial-Out Shift Register.

The logic circuit given below shows a serial-in serial-out shift register. The circuit consists of four D flip-flops which are connected in a serial manner. All these flip-flops are synchronous with each other since the same clock signal is applied to each flip flop. The main use of a SISO is to act as a delay element.

Serial-In Serial-Out Shift Register (SISO) –

The shift register, which allows serial input (one bit after the other through a single data line) and produces a serial output is known as Serial-In Serial-Out shift register. Since there is only one output, the data leaves the shift register one bit at a time in a serial pattern, thus the name Serial-In Serial-Out Shift Register.

The logic circuit given below shows a serial-in serial-out shift register. The circuit consists of four D flip-flops which are connected in a serial manner. All these flip-flops are synchronous with each other since the same clock signal is applied to each flip flop. The main use of a SISO is to act as a delay element.

Institute of Engineering & Management, New Town Campus
Department of Computer Science & Engineering

Computer Organization & Architecture Laboratory
PCCCS492

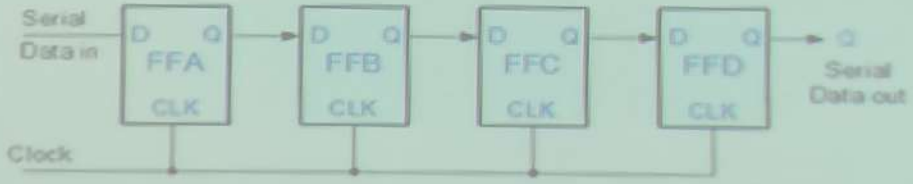


Fig: Logic diagram of 4-bit Serial In Serial Out shift register using D-flip-flop

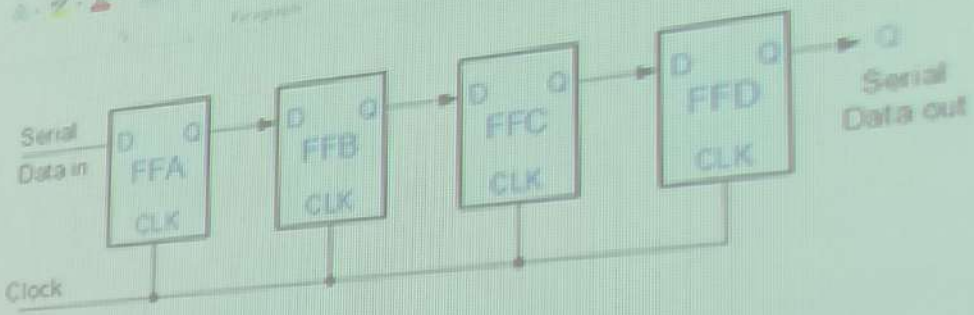


Fig: Logic diagram of 4-bit Serial In Serial Out shift register using D-flip-flop

Serial-In Parallel-Out shift Register (SIPO) –

The shift register, which allows serial input (one bit after the other through a single data line) and produces a parallel output is known as Serial-In Parallel-Out shift register. the main use of the SIPO register is to convert serial data into parallel data.

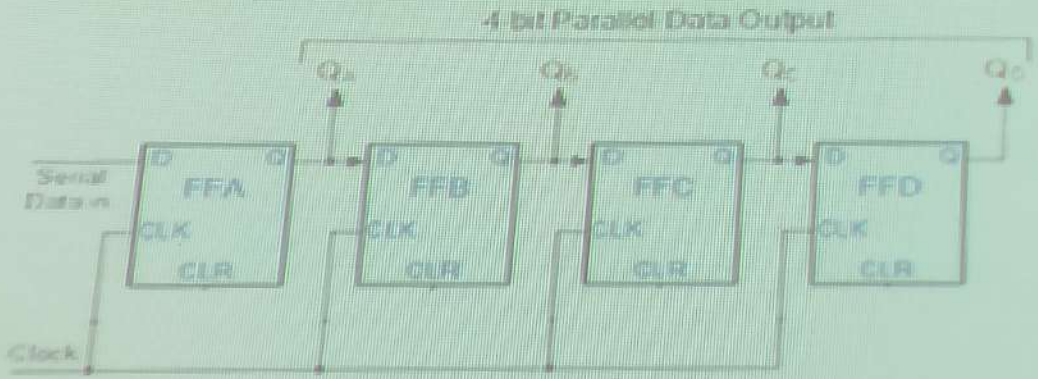
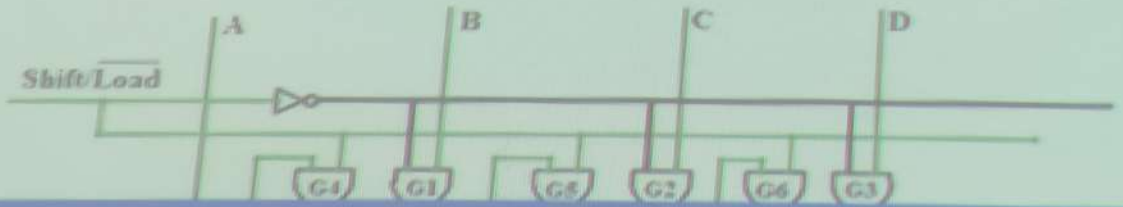


Fig: Logic diagram of 4-bit Serial In parallel Out shift register using D-flip-flop

Parallel-In Serial-Out Shift Register (PISO)

The shift register, which allows parallel input (data is given separately to each flip flop and in a simultaneous manner) and produces a serial output is known as Parallel-In Serial-Out shift register. A Parallel in Serial out (PISO) shift register us used to convert parallel data to serial data.



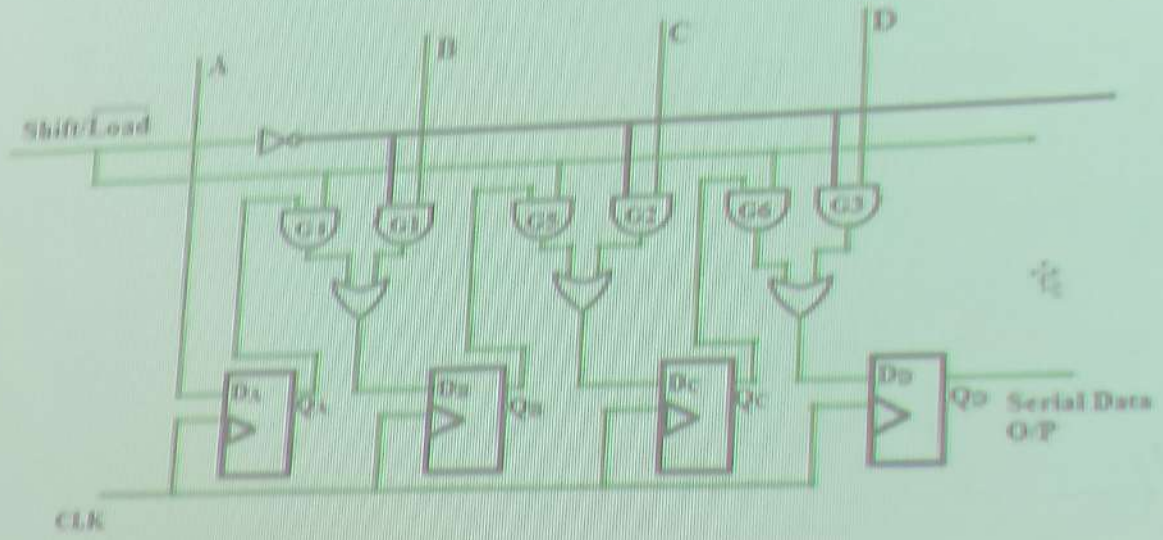


Fig. Logic diagram of 4-bit Parallel In Serial Out shift register using D-flip-flops

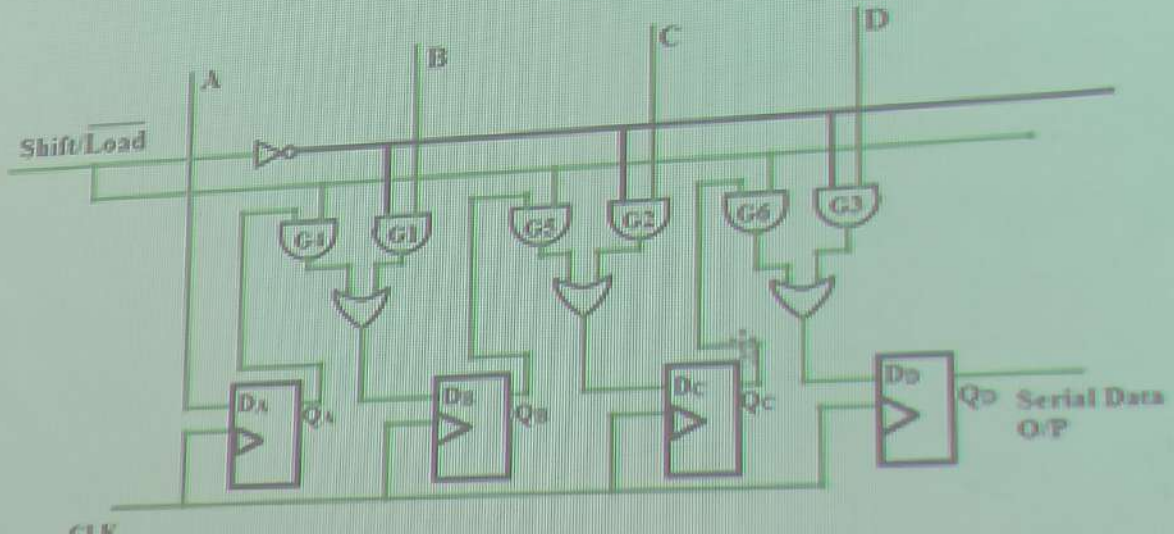


Fig: Logic diagram of 4-bit Parallel In Serial Out shift register using D-flip-flop

Parallel-In Parallel-Out Shift Register (PIPO) –

The shift register, which allows parallel input (data is given separately to each flip flop and in a simultaneous manner) and also produces a parallel output is known as Parallel-In parallel-Out shift register. A Parallel in Parallel out (PIPO) shift register is used as a temporary storage device

Parallel-In Parallel-Out Shift Register (PIPO) –

The shift register, which allows parallel input (data is given separately to each flip flop and in a simultaneous manner) and also produces a parallel output is known as Parallel-In parallel-Out shift register. A Parallel in Parallel out (PIPO) shift register is used as a temporary storage device

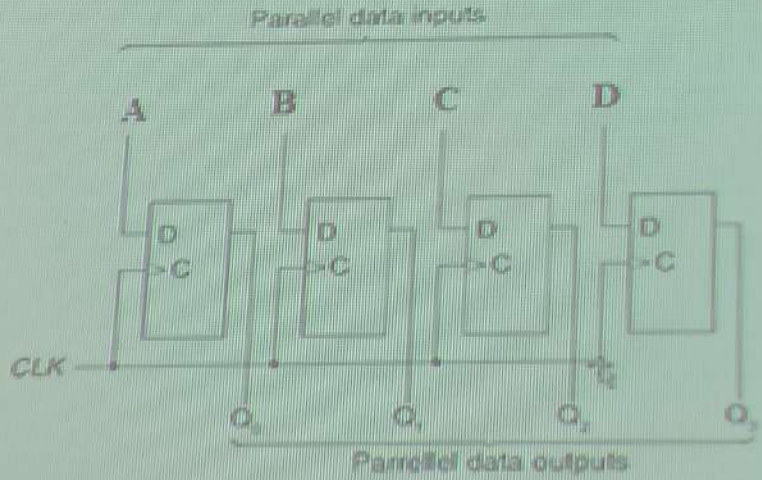
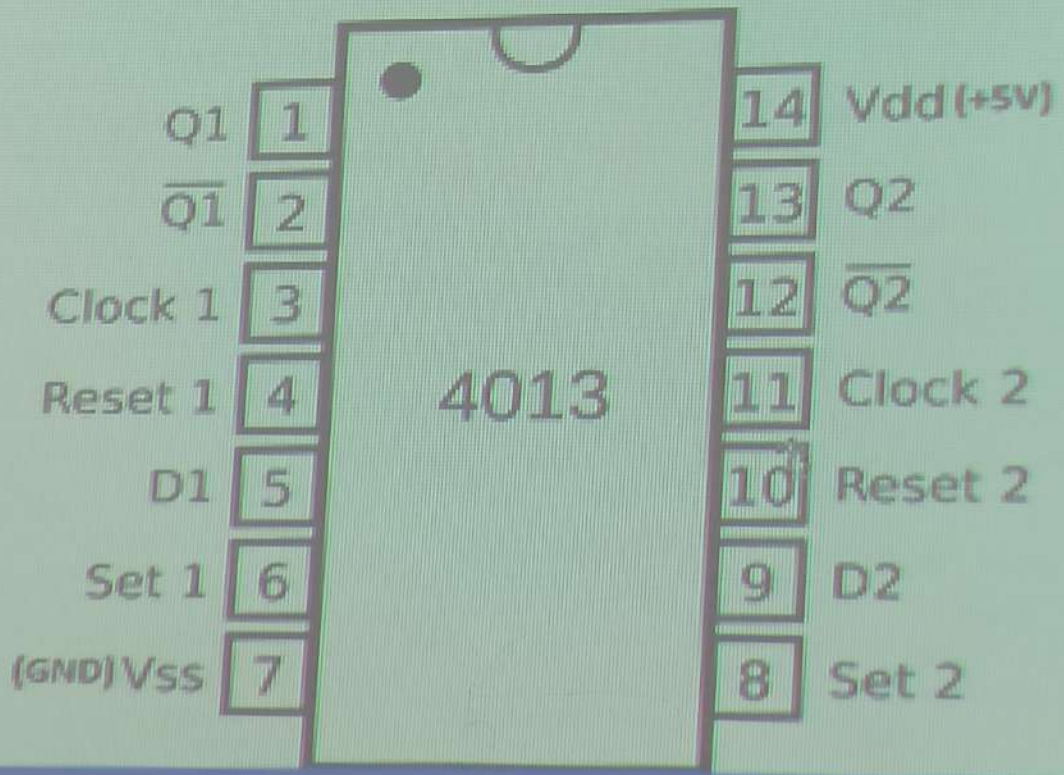


Fig: Logic diagram of Parallel In parallel Out shift register using D-flip-flop

PIN DIAGRAM:


Q1
1
$\overline{Q1}$
2
Clock 1
3
Reset 1
4
D1
5
Set 1
6
(GND) Vss
7
4013
14
Vdd (+5V)
13
Q2
12
$\overline{Q2}$
11
Clock 2
10
Reset 2
9
D2
8
Set 2

INSTRUMENT & COMPONENT REQUIRED:

Sl. No.	Item	Specification	Qty.

VERIFICATION TABLE:

1. Serial-In Serial-Out Shift Register (SISO)

Clock	Serial Data Input(D)	Serial Data Output(Q)
0		
1		
2		
3		
4		

2. Serial-In Parallel-Out shift Register (SIPO) –

Clock	Serial Data Input(D)	Parallel Data Output			
		Q_A	Q_B	Q_C	Q_D
0					
1					
2					
3					
4					

3. Parallel-In Serial-Out Shift Register (PISO) –

Clock	Parallel Data Input				Serial Data Output
	A	B	C	D	
0					
1					
2					
3					
4					

4. Parallel-In Parallel-Out Shift Register (PIPO) –

Clock	Parallel Data Input				Parallel Data Output			
	A	B	C	D	Q_0	Q_1	Q_2	Q_3
0								
1								
2								
3								
4								

CONCLUSION: