University of Engineering & Management, Kolkata

Subject Name: Computer Organization & Architecture Laboratory

Subject Code: PCCCS492

ASSIGNMENT – 8

8.1. TITLE: Implementation of 4:1 MUX using 2:1 MUX (using Structural Method) in VHDL.

8.2. APPARATUS REQUIRED:

a. ModelSim software.

8.3. THEORY:

A multiplexer (or mux), also known as a data selector, is a device that selects between several analog or digital input signals and forwards the selected input to a single output line. The selection is directed by a separate set of digital inputs known as select lines. A multiplexer of 2n inputs has n select lines, which are used to select which input line to send to the output.

8.3.1. TRUTH TABLE FOR 4:1 MULTIPLEXER:

E	Select		Input				Output
	S_1	S_0	D_3	D_2	D_1	D_0	Y
0	×	×	×	×	×	×	0
1	0	0	×	×	×	1	1
1	0	1	×	×	1	×	1
1	1	0	×	1	×	×	1
1	1	1	1	×	×	×	1

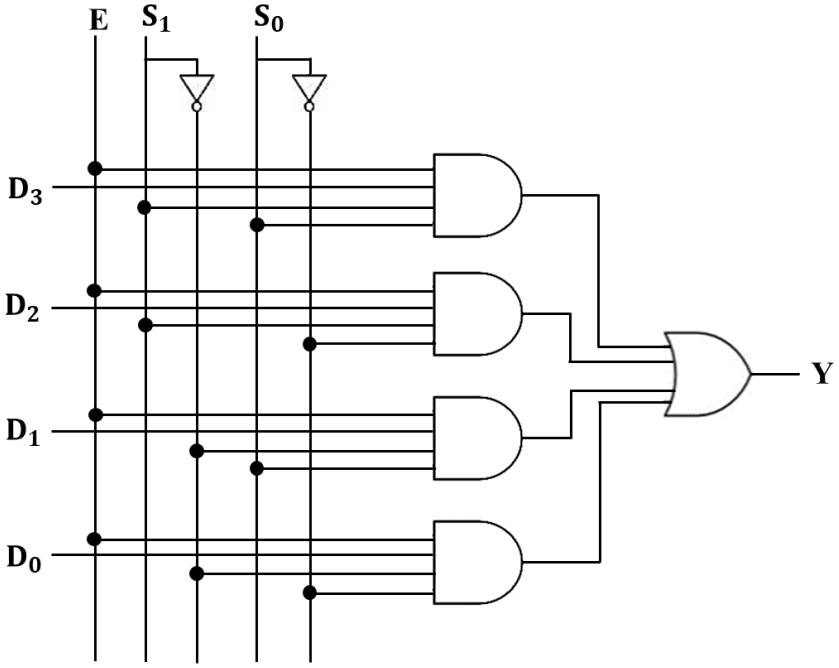
8.3.2. K-MAP FOR OUTPUT OF 4:1 MULTIPLEXER:

K-Map for Output:

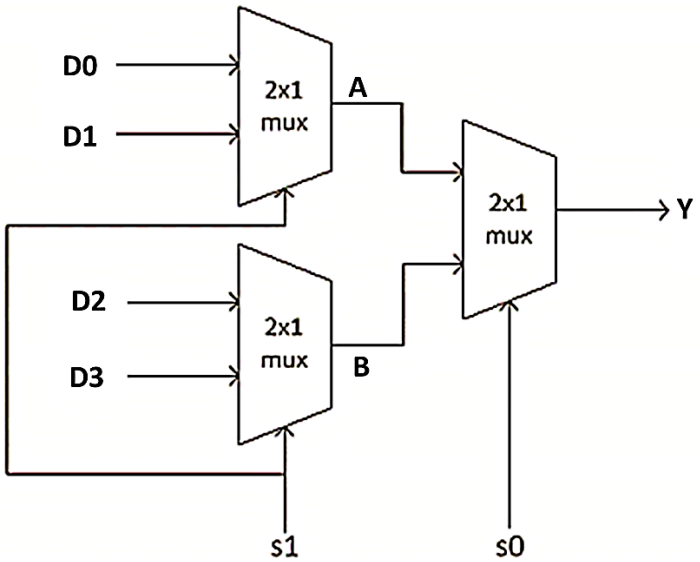
E \ S_1S_0	00	01	11	10
0	0	0	0	0
1	D_0	D_1	D_3	D_2

$$Y = E\overline{S_1}\,\overline{S_0}D_0 + E\overline{S_1}S_0D_1 + ES_1\overline{S_0}D_2 + ES_1S_0D_3$$

8.3.3. 4:1 MULTIPLEXER USING BASIC GATES:

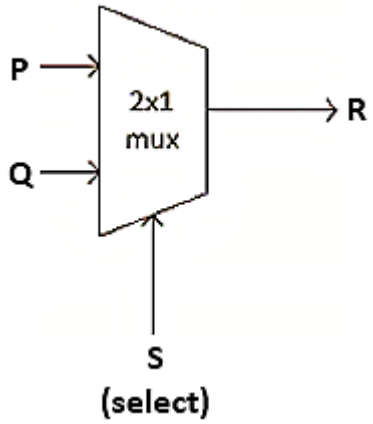


8.3.4. 4:1 MUX USING 2:1 MUX:



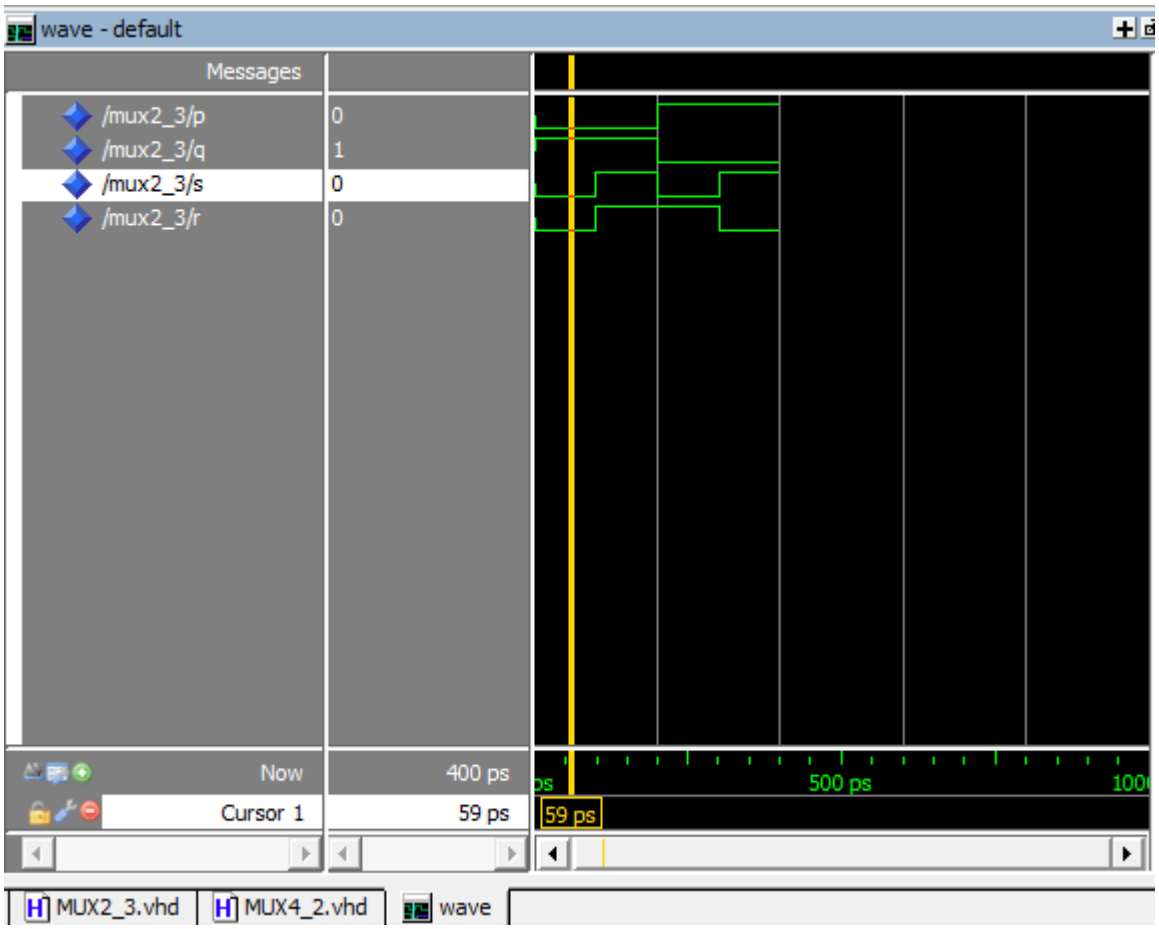
8.4. VHDL CODE:

8.4.1. Component 2:1 MUX (using Behavioral Method):




```
library IEEE;
use IEEE.STD_LOGIC_1164.ALL;

entity MUX2_3 is
port(P,Q : in STD_LOGIC;
S: in STD_LOGIC;
R: out STD_LOGIC);
end MUX2_3;

architecture BEHAVIORAL of MUX2_3 is

begin

process (P,Q,S) is
begin
if (S ='0') then
R <= P;
else
R <= Q;
end if;
end process;

end BEHAVIORAL;
```

8.4.2. Testbench waveform:

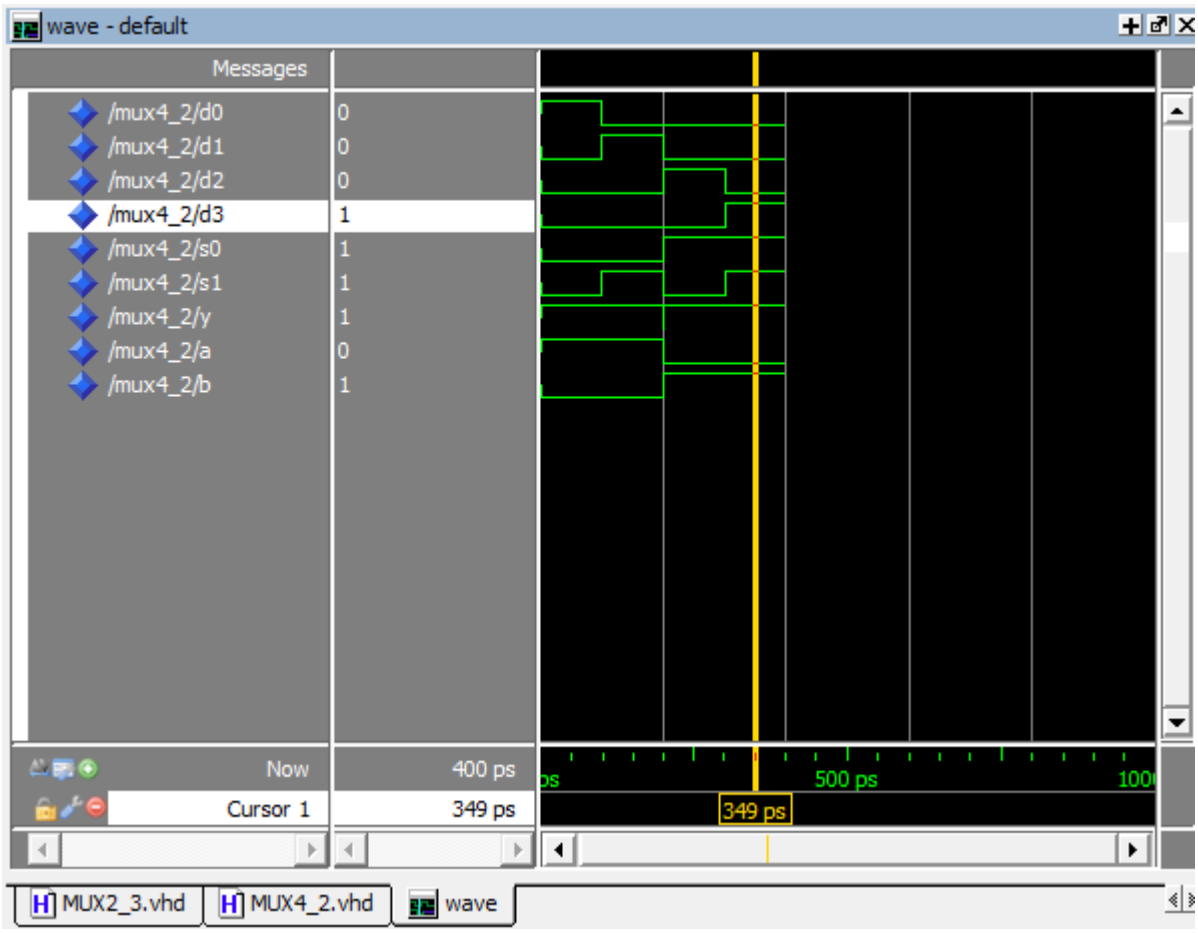


8.4.3. 4:1 MUX using 2:1 MUX (using Structural Method):

```
library IEEE;
use IEEE.STD_LOGIC_1164.ALL;

entity MUX4_2 is
port(D0,D1,D2,D3 : in STD_LOGIC;
    S0,S1: in STD_LOGIC;
    Y: out STD_LOGIC);
end MUX4_2;

architecture STRUCTURAL of MUX4_2 is

component MUX2_3 is
port(P,Q : in STD_LOGIC;
    S: in STD_LOGIC;
    R: out STD_LOGIC);
end component;

signal A, B: std_logic;
```

```
begin
m1: MUX2_3 port map(D0,D1,S1,A);
m2: MUX2_3 port map(D2,D3,S1,B);
m3: MUX2_3 port map(A,B,S0,Y);

end STRUCTURAL;
```

8.4.4. Testbench waveform:



8.5. PROCEDURE:

I. Create a new project in ModelSim platform.
II. Create a new file under this project.
III. Write the VHDL code in the editor window.
IV. Save and compile the written code.
V. Simulate the code and generate the testbench waveform.

8.6. CONCLUSION: