Page No./	
Date.	

Experiment-3

Realisation of Parallel odder using Ic 400 8.

Aim: To realise parallel adder rusing IC 4008.

Theory: A digital circuit that odds two lierary numbers of any but length in parallel form and produces the super of trase member in parallel form is called a parallel adder.

- => A parallel adder lasifally consists at free adders
- in a stain toum.

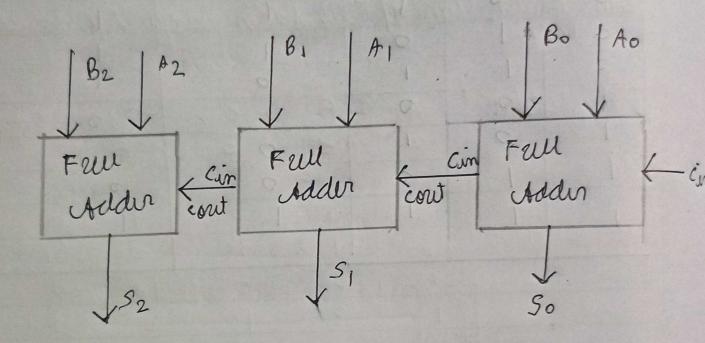
 Here, the ordered belt of each brill adder is sonneiled the the infect earry terminal of the new fruit adder circuit in the chain.

Working brimiple of Parallel Adder:

The parallel adder resporms the livary addition of two numbers as per the following step:

Dhe 1: Firstly the full addr circuit FAI, adds the lits AI and BI along with the inpert carry lit cin to produce the sum lit SI, where it is the LSB of the output sum. At this stage,

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Block diagram of 3-lit parallel addes

Page No./

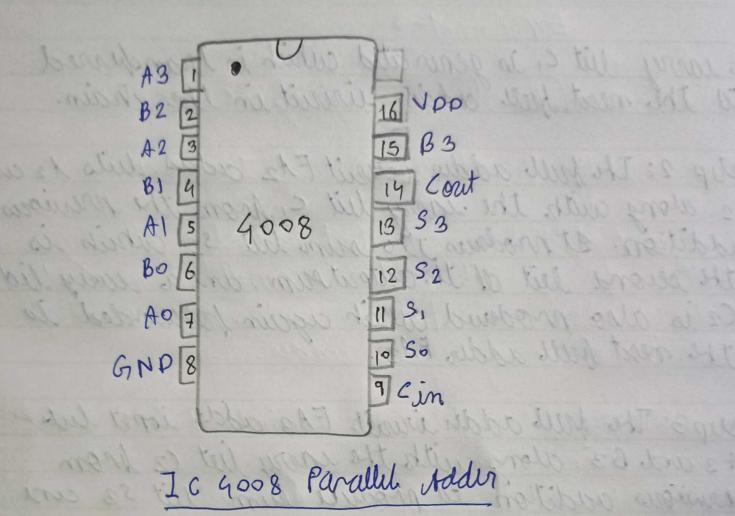
a earry but c, is generated which is transperred to the ment been adder circuit in the chain.

By along with the earry leit c, from the previous addition. It produces the sum let 32 which is the second leit of the output sum, and a way lid C2 is also produced which again forwarded to the next full adder #A3.

A3 and B3 along with the varry list (2 from runious addition to produce sum list 53 and sarry list (3.

Dup 9: The full adder circuit FAG adds is pet lits AG and BG along with the early let C3 troward from FA3. It generales the last rum lit 39 and a last early leit C9.

stip5: The output sum of the parallel adder is then given ly Sout = C434 S3 S2 S1



generates the fast sound

dig to the full adding issuit EAG adda wordt

siste for action day with the word let co

Judy Jui Cs

lonstruting a Paralle Adder

- 1) The AO to A3 rins are the inpects Nor the 4 Luits at the mumber A.
- 2) The BO tu B3 rins are the inputs for the 9 lids at mimber B.
- 3) The Cin Pin in the input bor a surry in lit. It's only wred il you are sonlining reveral assures set to Low when root in weed.
- 9) The so Iv s3 pins are the outputs for the 4 luts of the sum s.
- 5) The coutpin is the output for the 5th lid of the sum 3 (or carry out lit)

Pir Overview:

un supply vallage (-3 tr - 15 v)
(-3 lu - 154)

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Page No./ Date./

GND	8	Power	Ground (0V)
Ao tu A3	7,5,3,1	Input	Bits Ola 3 hor input member A
Bo ta B	3 6, 4, 3,13	Input	Bits ota 3 Nor input mumber B
712	9	Input	Jarry-In list
5= tu 53	10,11,12,	output	Bits o to 3 dos
Cont	14	Output	larry out Bit (Bit 4

Sondrision:

sonsider an example of (100)2+ (011)2

Hure, X=100 (A2=1, X1=0, X0=0) Y=011 (72 = 0, 71=1, 70=1)

In 1st Frell Adder,

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Sum = 011/27