University of Engineering and Management

Institute of Engineering & Management, Salt Lake Campus
Institute of Engineering & Management, New Town Campus
University of Engineering & Management, Jaipur

Syllabus for B.Tech Admission Batch 2023

Subject Name: Computer Organization & Architecture **Subject Code: PCCCS402**
Credit:3 **Lecture Hours: 36**

Pre-requisite: Digital Electronics, Basic Electronics

Relevant Links:

Study Material | Coursera | NPTEL | LinkedIn Learning | Infosys Springboard

Module number	Topic	Sub-topics	Mapping with Industry and International Academia	Lecture Hours	Corresponding Lab Assignment
1	**Introduction and Performance Evaluation**	**Role of abstraction, basic functional units of a computer, Stored Program Architecture, Von-Neumann model of computation, A note on Moore's law, clocking methodology, Amdahl's law, Notion of IPC, and performance.**	***International Academia: https://ocw.mit.edu/courses/6-823-computer-system-architecture-fall-2005/pages/lecture-notes/*** ***AICTE-prescribed syllabus: https://www.aicte-india.org/sites/default/files/Model_Curriculum/Updated-AICTE%20-%20UG%20CSE.pdf*** ***Industry Mapping: SPEC***	**3L**	1. Familiarization of Hardware assembling for a digital computer. 2. Familiarization of SPEC Benchmark Application for CPU.

		"Computer Organization and Design: The Hardware/Software Interface", David A. Patterson and John L. Hennessy, 5th Edition, Elsevier. – Chapter1	***(https://www.spec.org)***		
2	**Data representation and basic operations**	**Fixed and floating point (IEEE 754 Single and double precision format) representation of numbers; Overflow; Design of Adders - Ripple Carry Adder, Carry Look Ahead Adder, multiplication - shift-and-add, Booth multiplier, carry save multiplier, etc. Division - non-restoring and restoring techniques, floating point arithmetic.** **1. Computer System Architecture: Third Edition, Morris Mano. – Chapter 3** **2. Computer Organization: Fifth Edition Carl Hamacher, Zvonko Vranesic and Safwat Zaky. – Chapter 6**	***International Academia: https://web.stanford.edu/class/cs107/*** ***AICTE-prescribed syllabus: https://www.aicte-india.org/sites/default/files/Model_Curriculum/Updated-AICTE%20-%20UG%20CSE.pdf*** ***Industry Mapping:*** ***VHDL - online platform (https://www.edaplayground.com/)*** ***VHDL- Xilinx ISE*** ***Hardware Chipsets (TTl IC Chipsets 7400, 7402, 7404, 7408, 7432,7486, 74151, 74153, 7483; CMOS IC Chipsets 4081,4011,4071,4001,4070, 4013D)***	**7L**	1. Implementation of Half Adder, Half Subtractor, Full Adder, Full Subtractor using VHDL (Dataflow Model). 2. a) Implementation of Full Adder using VHDL (Behavioral Model). b) Implementation of n-bit Carry propagation adder in VHDL (Behavioral Model). 3. Implementation of 4:1 MUX using 2:1 MUX (using Structural Method) in VHDL. 4. Implementation of signed multiplier using VHDL. 5. Implementation of Non-Restoring Division algorithm using VHDL. 6. Realization of Boolean Expressions Using Basic Gates (IC Chips). 7. Design an 8 to 1 multiplexer unit (MUX) using basic gates and using IC 74151.

					8. Design of A 4-Bit Parallel Binary Adder Circuit Using The IC-Chip7483. 9. Use a multiplexer unit to design a composite ALU [ALU Logic circuit, shift circuit and arithmetic circuit]. 10. Implementation of Full adder using FPGA kit.
3	**Instruction Set Architecture**	**CPU registers, instruction format and encoding, addressing modes, instruction set, instruction types, instruction decoding and execution, basic instruction cycle, Reduced Instruction Set Computer (RISC), Complex Instruction Set Computer (CISC), Case study - instruction sets of some common CPUs.** **1. Computer System Architecture: Third Edition, Morris Mano. – Chapter 8**	***International Academia: https://ocw.mit.edu/courses/6-823-computer-system-architecture-fall-2005*** ***https://www.cse.iitd.ac.in/~srsarangi*** ***AICTE-prescribed syllabus: https://www.aicte-india.org/sites/default/files/Model_Curriculum/Updated-AICTE%20-%20UG%20CSE.pdf*** ***Industry Mapping: Keil MDK (https://www.keil.com)*** ***TRACE32 Simulator (https://www.lauterbach.com)*** ***Arm Instruction Emulator (https://developer.arm.com/Tools%20and%20Software/Arm%20Instruction%20Emulator)***	**6L**	1. Generate Happy numbers. 2. Generate Autonomic numbers 3. Generate Hardy-Ramanujan number 4. Implement a 4-function calculator.
4	**Processor Design**	**hardwired and micro-programmed**	***International Academia: https://ocw.mit.edu/courses/6-823-computer-system***	**3L**	Design a primitive CPU for the given instruction subset-

		design approaches, Case study - design of a simple hypothetical CPU **1. Computer System Architecture: Third Edition, Morris Mano. –Chapter 7** **2. Computer Organization: Fifth Edition Carl Hamacher, Zvonko Vranesic and Safwat Zaky. – Chapter 7**	***-architecture-fall-2005*** ***AICTE-prescribed syllabus: https://www.aicte-india.org/sites/default/files/Model_Curriculum/Updated-AICTE%20-%20UG%20CSE.pdf*** ***Industry Mapping: Keil MDK (https://www.keil.com)*** ***TRACE32 Simulator (https://www.lauterbach.com)*** ***Arm Instruction Emulator (https://developer.arm.com/Tools%20and%20Software/Arm%20Instruction%20Emulator)***		i) data transfer ii) arithmetic operations iii) logical operations iv) branch statements
5	**Memory hierarchy**	**Memory hierarchy; Main memory organization - paging, segmentation, virtual memory;** **Cache memory- different indexing mechanisms, Trade-offs related to block size, associativity, and cache size,** **Processor-cache interactions for a read/write request, basic optimizations like write through/write-back caches, Average memory access time, Cache replacement policies (LRU), locality of reference, Memory interleaving; introduction to magnetic disks (notion of tracks, sectors).** **1. Computer System Architecture: Third Edition, Morris Mano. –Chapter 12**	***International Academia: https://ocw.mit.edu/courses/6-823-computer-system-architecture-fall-2005*** ***AICTE-prescribed syllabus: https://www.aicte-india.org/sites/default/files/Model_Curriculum/Updated-AICTE%20-%20UG%20CSE.pdf*** ***Industry Mapping:*** ***VHDL - online platform (https://www.edaplayground.com/)*** ***VHDL- Xilinx ISE***	**7L**	1. Implementation of memory unit consisting of 16X4 RAM and 8X 4 ROM. 2. Implement Read Write operation using 16X4 RAM.

6	**Input/Output Organization**	**Programmed I/O, Interrupt-driven I/O, and DMA.** **1. Computer System Architecture: Third Edition, Morris Mano. – Chapter 11**	***International Academia: https://ocw.mit.edu/courses/6-823-computer-system-architecture-fall-2005*** ***AICTE-prescribed syllabus: https://www.aicte-india.org/sites/default/files/Model_Curriculum/Updated-AICTE%20-%20UG%20CSE.pdf*** ***Industry Mapping: 8051 Microcontroller***	**2L**	1. Interface 7 segment display using 8051 Microcontroller and requisite I/O modules. 2. Interface 4X4 keypad using 8051 Microcontroller and requisite I/O modules.
7	**Parallel Processing**	**Pipelining - Basic concepts, instruction and arithmetic pipeline, different types of dependencies and hazards, techniques for handling hazards, Pipeline optimization techniques - reservation table;** **Superscalar, superpipelined and VLIW processor architectures; Array and vector processors;** **Multiprocessor architecture: taxonomy of parallel architectures; Centralized shared-memory architecture and distributed shared memory architecture; Cache Coherence;** **1. "Computer Organization and Design: The Hardware/Software Interface", David A. Patterson and John L. Hennessy, 5th Edition, Elsevier. – Chapter4 and Chapter 6**	***International Academia: https://ocw.mit.edu/courses/6-823-computer-system-architecture-fall- 2005*** ***AICTE-prescribed syllabus: https://www.aicte-india.org/sites/default/files/Model_Curriculum/Updated-AICTE%20-%20UG%20CSE.pdf*** ***Industry Mapping:*** ***1. RIPES (https://github.com/mortbopet/Ripe s)*** ***VHDL - online platform (https://www.edaplayground.com), VHDL-Xilinx ISE***	**6L**	1. Implement a Pipelined Multiplier using VHDL and FPGA Kit. 2. Implement a Pipeline Control Unit using RIPES

Text Books:

1. Computer System Architecture: Third Edition, Morris Mano.
2. Computer Organization: Fifth Edition Carl Hamacher, Zvonko Vranesic and Safwat Zaky.
3. Computer Organization and Design: The Hardware/Software Interface: David A. Patterson and John L. Hennessy.

Reference Books:

1. Computer Organization and Architecture – Designing for Performance: William Stallings
2. Computer Architecture and Organization: John P Hayes
3. Computer Architecture and Parallel Processing: K. Hwang, F. A. Briggs

List of Assignments:

1. Familiarization of Hardware assembling for a digital computer.
2. Familiarization of SPEC Benchmark Application for CPU.
3. Realization of Boolean Expressions Using Basic Gates (IC Chips).
4. Design an 8 to 1 multiplexer unit (MUX) using basic gates and using IC 74151.
5. Design of A 4-Bit Parallel Binary Adder Circuit Using The IC-Chip7483.
6. Implementation of Half Adder, Half Subtractor, Full Adder, Full Subtractor using VHDL (Dataflow Model).
7. a) Implementation of Full Adder using VHDL (Behavioral Model). b) Implementation of n-bit Carry propagation adder in VHDL (Behavioral Model).
8. Implementation of 4:1 MUX using 2:1 MUX (using Structural Method) in VHDL.
9. Implementation of signed multiplier using VHDL.
10. Implementation of Non-Restoring Division algorithm using VHDL.
11. Use a multiplexer unit to design a composite ALU [ALU Logic circuit, shift circuit and arithmetic circuit].
12. Implementation of Full adder using FPGA kit.
13. Design a primitive CPU for the given instruction subset-
    i) data transfer
    ii) arithmetic operations
    iii) logical operations
    iv) branch statements
14. Implementation of memory unit consisting of 16X4 RAM and 8X 4 ROM.
15. Implement Read Write operation using 16X4 RAM.
16. Interface 7 segment display using 8051 Microcontroller and requisite I/O modules.
17. Implement a Pipelined Multiplier using VHDL and FPGA Kit.