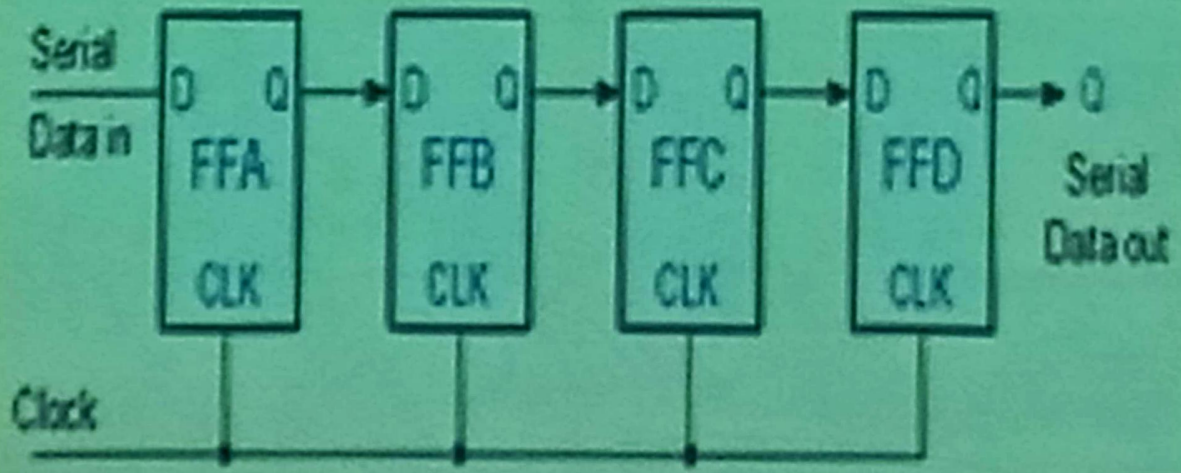
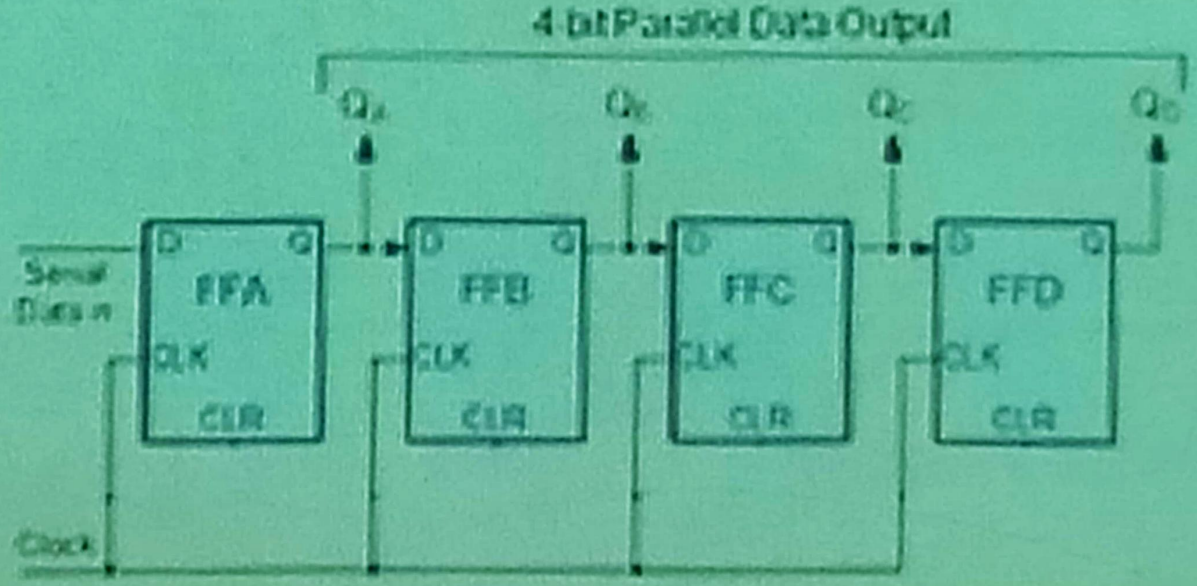
Serial In Serial Out (SISO)

- Data enters serially and exits serially.
- Simplest type of shift register.



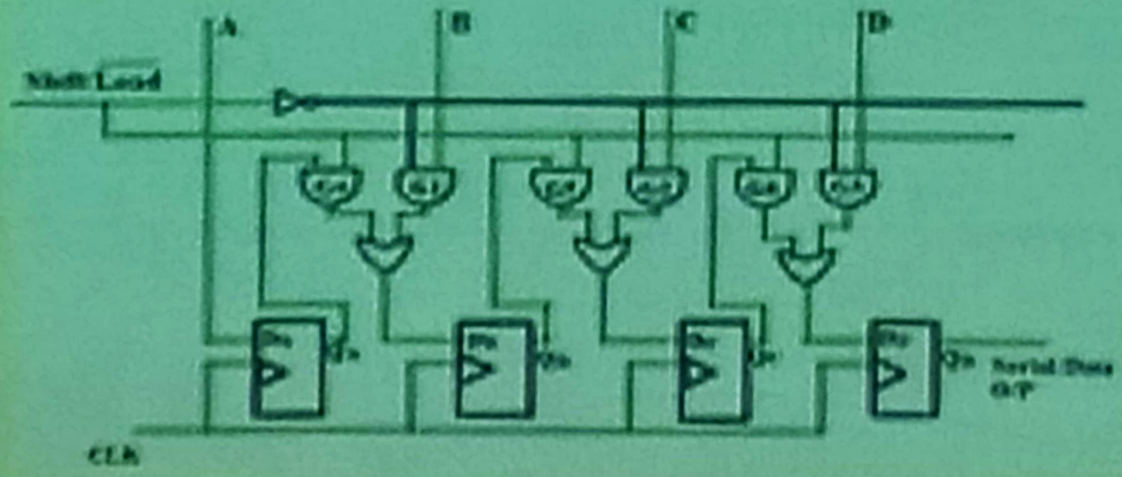
Serial In Parallel Out (SIPO)

- Data enters serially but is read out parallelly.
- Used when parallel output is needed.



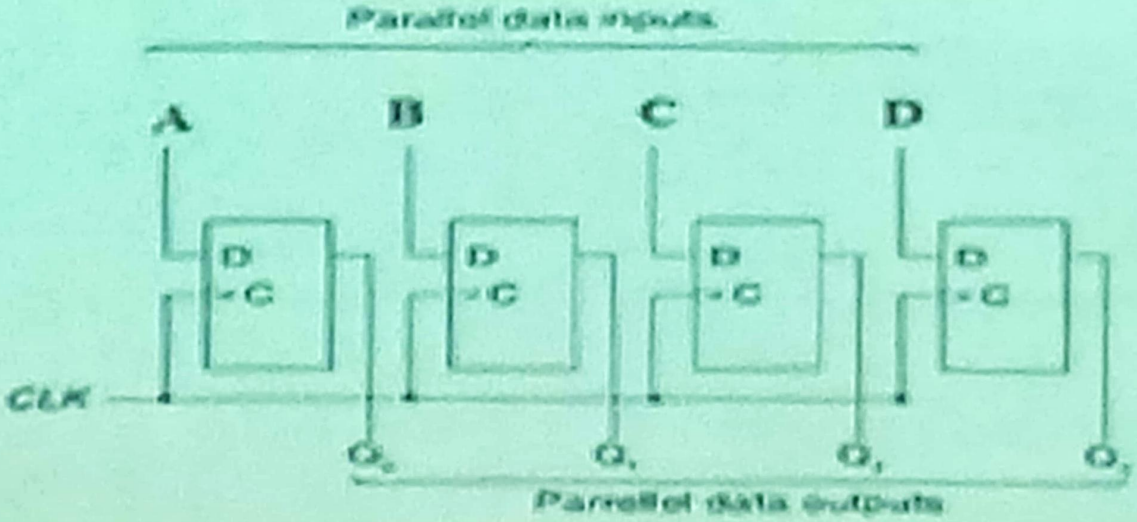
Parallel In Serial Out (PISO)

- Data is loaded in parallel and exits serially.
- Suitable for serial communication systems.

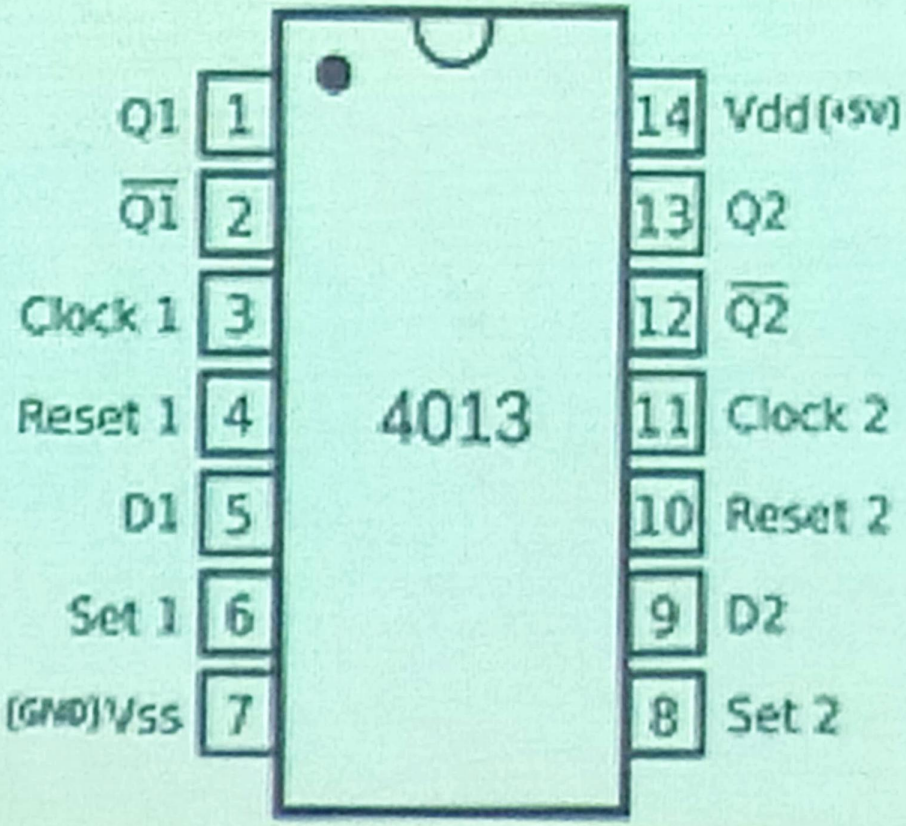


Parallel In Parallel Out (PIPO)

- Data is loaded and retrieved in parallel.
- Fastest data transfer method.



Pin Diagram of Dual D flip-flop IC-4013



VERIFICATION TABLE:

1. Serial-In Serial-Out Shift Register (SISO)

Clock	Serial Data Input(D)	Serial Data Output(Q)
0		
1		
2		
3		
4		

VERIFICATION TABLE:

2. Serial-In Parallel-Out shift Register (SIPO)

Clock	Serial Data Input(D)	Parallel Data Output			
		Q_A	Q_B	Q_C	Q_D
0					
1					
2					
3					
4					

VERIFICATION TABLE:

3. Parallel-In Serial-Out Shift Register (PISO)

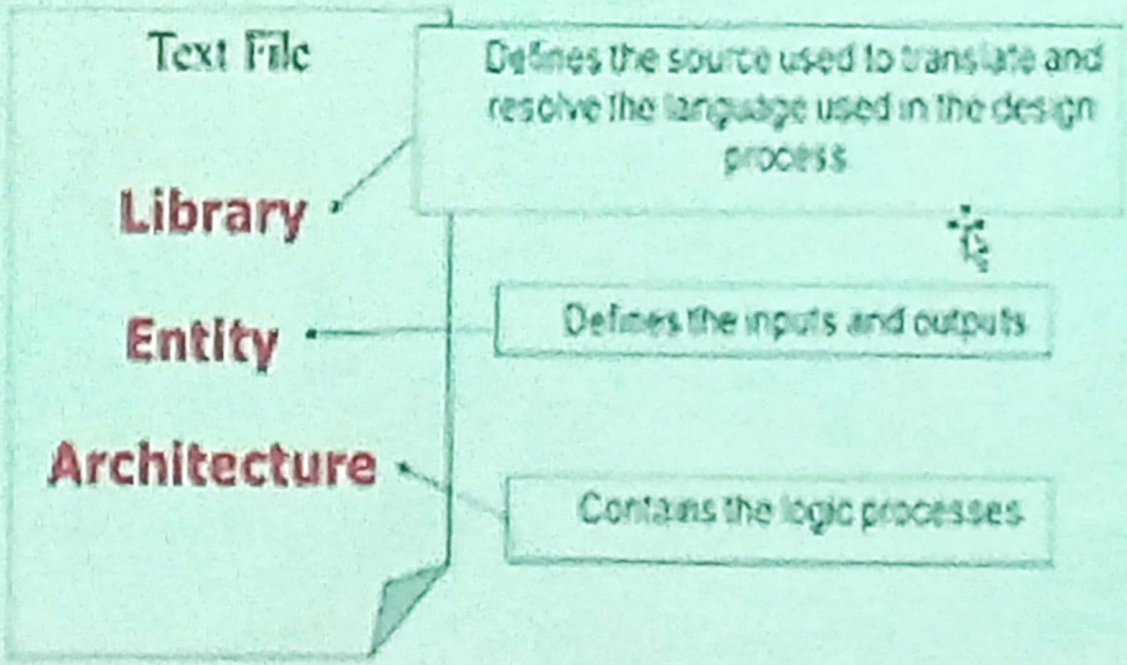
Clock	Parallel Data Input				Serial Data Output
	A	B	C	D	
0					
1					
2					
3					
4					

VERIFICATION TABLE:

4. Parallel-In Parallel-Out Shift Register (PIPO)

Clock	Parallel Data Input				Parallel Data Output			
	A	B	C	D	Q_0	Q_1	Q_2	Q_3
0								
1								
2								
3								
4								

Basic structure of VHDL



Two input OR GATE

- *VHDL Code for OR gate*

- *Header file declaration*

```
library IEEE;
use IEEE.std_logic_1164.all;
```

- *Entity declaration*

```
entity orGate is
port(A : in std_logic; -- OR gate input
B : in std_logic; -- OR gate input
Y : out std_logic); -- OR gate output
end orGate;
```

– Dataflow Modelling Style

- *Architecture definition*

```
architecture orLogic of orGate is
begin
Y <= A OR B:
end orLogic;
```