

# Inf2C Computer Systems

## Tutorial 3, Week 7

### 1. **Ripple Carry Adder**

Assume that the propagation delay in each gate in a 32-bit ripple carry adder is 100ps. How fast can a 32-bit addition be performed? Assuming that the adder delay is the major limiting factor on the clock speed, how fast can we clock the processor?

### 2. **Modulo-6 Counter**

Design a synchronous Modulo-6 counter that will be able to count up to 5 clock positive edges. When it reaches 5, it resets to 0 and it starts the whole process again. In order to design this counter you can use D flip-flops and any one, two or three input gate you like.

### 3. **Single-Cycle Processor**

Discuss the steps in executing the `sw` instruction in the single-cycle datapath presented in Figure 1.

Next discuss the changes needed to the datapath and control to support the `jr` instruction.

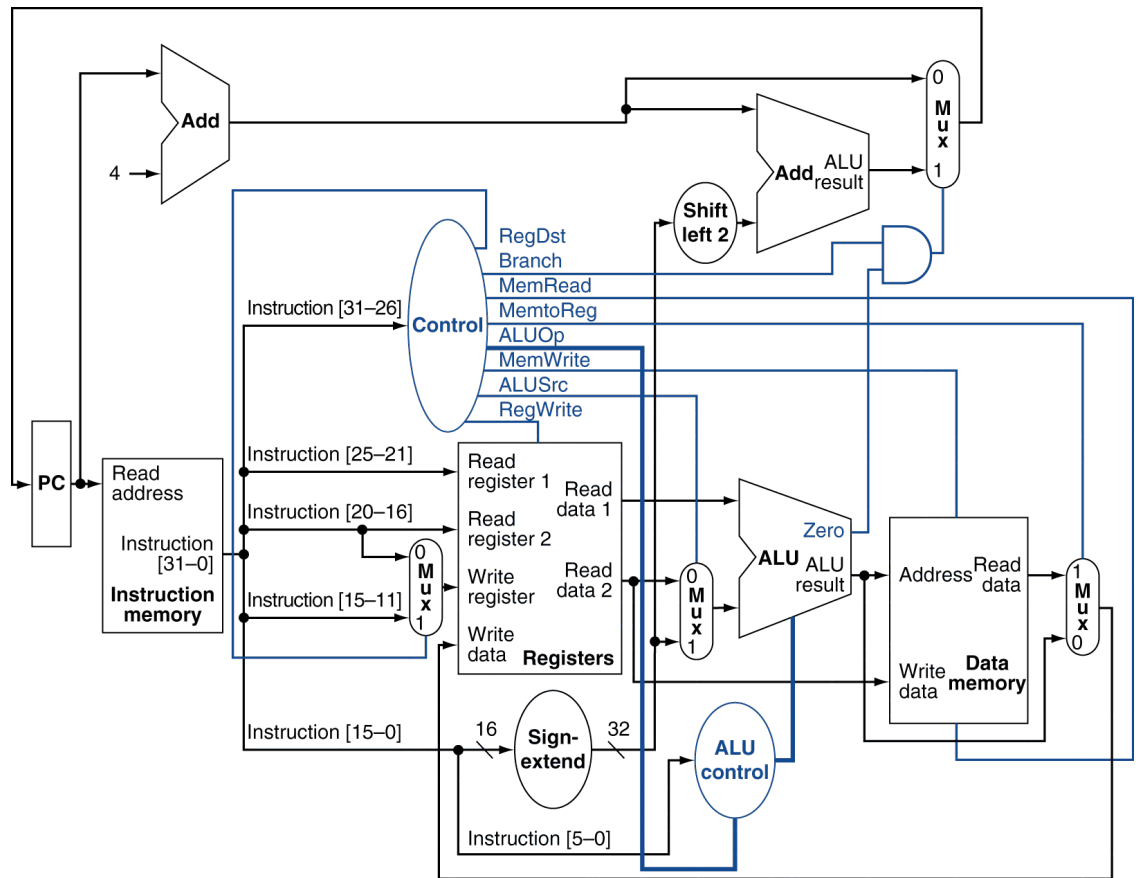


Figure 1: MIPS Single-Cycle Datapath