

# Interim Design Report

Micromouse Power Subsystem



**Prepared by:**

Ronald Walters

WLTRON002

**Prepared for:**

EEE3088F

Department of Electrical Engineering

University of Cape Town

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# Chapter 1

## Introduction

### 1.1 Problem Description

This report details the procedural and quantitative approach taken to aid the design, synthesis, and testing of one of the four compartmentalized subsystems, which comprise the hardware of an autonomous vehicular maze-solving robot. Colloquially called a micro-mouse, the robot (system) consists of the motherboard,  $\mu$ C, sensing, and power subsystems. The report is centered on the power subsystem and utilizes a systems engineering approach to segment the core functionality of the subsystem into micro-systems concerning power; distribution, availability, isolation, and power supply charging.

### 1.2 Scope and Limitations

**The scope of each power micro-system detailing their respective concepts of operation.**

$\alpha$ ) **The power distribution micro-system** distributes power within the subsystem to operate two motors. Additionally, a power supply rail is supplied to the motherboard which transfers power to the  $\mu$ C and sensing subsystem, enabling their operation.

This micro-system does not necessitate regulating the power supply rail voltage sent to the motherboard, as the  $\mu$ C contains a voltage regulator.  $\beta$ ) **The power availability micro-system** is implemented to sense the State of Charge (SoC) of the micro-mouse's battery, which is detected, measured as an analog voltage reference, and provided as an input to the  $\mu$ C's analog-to-digital converter (ADC). Due to the depth of complexity, this micro-system does not entail implementing an Unscented Kalman Filter (UKF) to model the non-linear voltage discharge of the battery accurately [1].

$\gamma$ ) **The power isolation micro-system** ensures that undesired currents do not over-discharge the battery when the micro-mouse is switched off. This micro-system does not permit the use of galvanic isolation or the utilization of an optocoupler.

$\delta$ ) **The power supply charging micro-system** provides a constant, voltage and current across the battery to recharge the system's power supply while providing a safe and effective Battery Management System (BMS). This micro-system does not warrant the inclusion of battery temperature monitoring.

**Power Subsystem Design and Testing Limitations** This design was hindered by an inability to perform simulation testing of the micro-systems, and the impact each has on the performance of the power subsystem overall. Additionally, the limitation of the project's budget placed constraints on the design decisions made in each micro-system. Furthermore, the power subsystem design was impeded, due to the encapsulation of information regarding the specific interoperability and intraoperability of the system and its component subsystems. Ultimately, the project's time constraint resulted in expediency being valued over meticulousness.

### 1.3 GitHub Link

[https://github.com/anh-duynguyen/UCT\\_Micromouse\\_EEE3088F.git](https://github.com/anh-duynguyen/UCT_Micromouse_EEE3088F.git)

# Chapter 2

## Requirements Analysis

### 2.1 Requirements

The requirements of the micro-mouse power module from the client are described in [Table 2.1](#) below.

Table 2.1: Functional Requirements of the power subsystem.

| Requirement ID | Description   |
|----------------|---|
| FR01           | Design an ON/OFF switch for the micro-mouse, which should draw less than $500 \mu\text{A}$ of current from the battery when the system is switched off, and supply the battery's rated output current when switched on. |
| FR02           | Charge the system's battery using two 5V input pins from the motherboard.   |
| FR03           | Provide an analog signal containing the battery's voltage information to the $\mu\text{C}$ 's ADC, through the motherboard to sense the battery's SoC.  |
| FR04           | Operate two brushed DC motors, each drawing a maximum of 840mW from the battery, implementing four pulse width modulated (PWM) signal inputs from the $\mu\text{C}$ through the motherboard.                            |
| FR05           | Provide the external subsystems with the battery voltage and the system's ground reference through the motherboard.   |
| FR06           | Remain within the maximum power subsystem budget for components of \$8.25.  |
| FR07           | Include a JST PH 2mm pin pitch connector footprint on the power subsystem PCB for the battery to connect to the power subsystem.  |
| FR08           | Include a 2x8 (2.54mm pin pitch) pin header footprint on the power subsystem PCB to connect the power subsystem to the motherboard.   |
| FR09           | Ensure there is a tab for the pin header that protrudes the power subsystem PCB to facilitate connection to the motherboard. The height of this tab should be a minimum of 18mm and the width, a maximum of 35mm.       |
| FR10           | Minimize the distance between the power PCB's center of mass and the micro-mouse's center of rotation.  |
| FR11           | Use KiCad to construct the power subsystem schematic, wherein the populated components are that which JLCPCB stocks, and generate the production files required using Bouni's KiCad JLCPCB tools.                       |
| FR12           | Submit the designed power subsystem production files to the client in 2 weeks.  |

## 2.2 Specifications

The specifications, refined from; the functional requirements in [Table 2.1](#), and the scope and limitations in [??](#), of the power subsystem are described in [Table 2.2](#) below.

Table 2.2: Specifications of the power subsystem derived from, the functional requirements in [Table 2.1](#), and the scope and limitations in [??](#).

| Specification ID | Description   |
|------------------|---|
| SP01             | Use Texas Instruments for all integrated circuit components to nullify the lack of simulation testing with in-depth component documentation.  |
| SP02             | Ensure test points are placed at various locations of interest to facilitate testing.   |
| SP03             | Mechanically isolate the electrical connection of the 1S1P battery, using a latching switch whose contact resistance is less than $50\text{ m}\Omega$ .   |
| SP04             | Ensure the charging of the 1S1P battery is at a maximum of $1\text{C} = 800\text{mA}$ .   |
| SP05             | Design the SoC output analog voltage signal to be less than the ADC's maximum input voltage of $3.6\text{V}$ <a href="#">[2]</a> for the STM32L476 $\mu\text{C}$ , over the voltage extrema of the battery.   |
| SP06             | Design the motor driver circuitry to withstand the maximum internal power dissipated when the motors draw $840\text{mW}$ each.  |
| SP07             | Minimize the quiescent current drawn by the power subsystem to under $10\text{ mA}$ .   |
| SP08             | In design decisions regarding a specific component, trade-off analyses must be conducted to ensure the cost of each component is compared as a weighted factor, and extended parts should have a disproportionate weight as such, to ensure the subsystem budget is adhered to. |
| SP09             | When designing the power subsystem PCB, minimize the moment arm by reducing the distance between the heaviest components and the pin header tab .   |
| SP10             | Ensure within the design decision process, trade-off analyses are conducted, which contain the number of components in stock on JLCPCB.   |
| SP11             | Download component symbol (.elibz) and footprint (.efoo) files from EasyEDA's link at the <a href="#">jlcpb.com/partdetail/</a> page and import them into KiCad.  |
| SP12             | Implement motor driver circuitry able control the speed and direction of the motors, by manipulating the PWM input signals according to the driver circuits logic table.  |
| SP13             | Ensure each micro-system does not interfere and adversely affect the operation of the other three power micro-systems.  |

## 2.3 Testing Procedures

A summary of the testing procedures designed to ensure the Functional Requirements of [Table 2.1](#) and their derived specifications from [Table 2.2](#) are quantifiable is given below in [Table 2.3](#).

Table 2.3: Acceptance testing for the micro-mouse power subsystem

| Acceptance Test ID | Description  |
|--------------------|--|
| AT01               | Visually inspect that component placement, footprints, and traces are correct, according to the power subsystem PCB's production files.  |
| AT02               | Conduct continuity testing with a multimeter between test points on the PCB, and detect short circuit faults before any voltage is applied to the power subsystem.   |
| AT03               | Measure the power supply charging micro-systems constant output current using a multimeter, to verify the data-sheet specifications.   |
| AT04               | Record the quiescent current drawn by the power subsystem using a multimeter in series.  |
| AT05               | Measure the current drawn from the battery when the system is switched off, and the voltage drop across the switch when the system is switched on using an oscilloscope.   |
| AT06               | Measure the power availability micro-systems output voltage over the 1S1P battery's voltage range with a multimeter.   |
| AT07               | Calculate the on-state resistance of the motor driver circuitry, by measuring the voltage across and current into the circuit using a multimeter, to calculate the thermal power dissipation.  |
| AT08               | Measure with a ruler the dimensions of the pin header tab, and the overall PCB size.   |
| AT09               | Upload production (Gerber, BOM, and Position) files to JLCPCB to ensure the subsystem budget is adhered to, and that the production files are JLCPCB compliant while also verifying JLCPCB has enough stock of the chosen components before submitting the files to the client.  |
| AT10               | Measure the center of mass to be within half of the PCB's total protruding length, using an axial fulcrum.   |
| AT11               | Measure with an oscilloscope the analog SoC output signal's AC RMS value to quantify the interference of the motor driver's PWM input on the sensitive analog SoC signal.  |
| AT12               | Testing the driver circuit's ability to operate and control the brushed DC motors involves varying the duty cycle of the input PWM wave, where the change in the speed of the motor is recorded. Additionally, the directional control of the motors is verified by applying the PWM signals corresponding with the driver circuits logic table, where the change in direction of the motor is recorded. Both procedures provide an indirect method of gauging acceptable performance from the driver circuit. |

## 2.4 Traceability Analysis

This section of paramount importance establishes how the functional requirements, specifications, and testing procedures are intra-connected within the power subsystem and inter-connected across the micro-mouse system in totality, which is summarized in Table 1.4 below, where each Traceability Analysis is given a unique ID (T\_A##), and expounded upon individually below.

Table 2.4: Requirements Traceability Matrix

| T_A## | Requirements       | Specifications | Acceptance Test |
|-------|--------------------|----------------|-----------------|
| T_A01 | FR01               | SP03           | AT05            |
| T_A02 | FR02               | SP04           | AT03            |
| T_A03 | FR03               | SP05           | AT06            |
| T_A04 | FR04               | SP06           | AT07            |
| T_A05 | FR05               | SP02           | AT02            |
| T_A06 | FR05 & FR07 & FR08 |                | AT01            |
| T_A07 | FR06               | SP08           | AT09            |
| T_A08 | FR09               |                | AT08            |
| T_A09 | FR10               | SP09           | AT10            |
| T_A10 | FR11               | SP10 & SP11    | AT09            |
| T_A11 |                    | SP01 & SP13    | AT11            |
| T_A12 |                    | SP07           | AT04            |
| T_A13 | FR04               | SP12           | AT12            |

- **T\_A01:** To achieve the switching described in **FR01**, with  $I_{BATT_{out}} \leq 500 \mu\text{A}$ , the specification **SP03** of a latching switch with low contact resistance is stated to ensure mechanical isolation of the electrical connection while ensuring the maximum output current retained. This is tested in **AT05**, using an oscilloscope to improve the resolution of the acceptance test measurement.
- **T\_A02:** Ensuring that **FR02** is met, requires the charging of the battery to be conducted safely as outlined in **SP04** which specifies the maximum charge current of 800mA. This is tested in **AT03** to verify that a safe and effective Battery Management System (BMS) is implemented.
- **T\_A03:** **FR03**'s requirement of sending an analog SoC signal to the  $\mu\text{C}$  resulted in **SP05**, which is specified to ensure the ADC on the  $\mu\text{C}$  is not damaged by a voltage from the power availability micro-system exceeding its maximum rated input voltage of 3.6V. The acceptance test of **AT06** was guided by FR03 and SP05, to ensure the ADC is not damaged.
- **T\_A04:** Meeting the driver circuit requirements presented in **FR04** necessitated the internal power dissipation capacity specified in **SP06**. Which is tested in **AT07** to verify the component's data-sheet parameters.
- **T\_A05:** To meet the provisions of **FR05** in supplying the motherboard with the battery voltage and the systems ground reference, **SP02** is derived to include test points at locations of interest on the power-subsystem PCB, which is verified by **AT02** which ensures the traces are correctly connected and additionally detects if there is a short circuit between the battery voltage and ground.
- **T\_A06:** The functional requirements of; **FR05**, concerning the supply of battery voltage and the systems ground reference, and **FR07 & FR08**, regarding the crucial footprints for the subsystems compatibility are qualitatively evaluated in **AT01** by visual inspection.

- **T\_A07:** Ensuring that the power subsystem budget designated under **FR06** is adhered to, facilitated the implementation of **SP08**, which details the condition that; component price and extended components, should be considered as weighted factors when design decisions on specific components are made. Confirmation that the budget is adhered to is achieved with **AT09**, before submission of the production files.
- **T\_A08:** To ensure the interoperability of the power subsystem PCB with the motherboard outlined in **FR09**, **AT08** is conducted to measure and confirm the subsystems are physically compatible.
- **T\_A09:** **FR10** details the requirements for the micro-mouse to be able to turn effectively. This is refined in **SP09**, stating that the moment arm of the heaviest components should be minimized, which is tested in **AT10** confirming that the center of mass lies within half of the power subsystem PCB's total length.
- **T\_A10:** KiCad is the software designated by **FR11** which implements; KiCad JLCPCB Tools to generate the production files and further stipulates that only JLCPCB parts can be used in the design. **FR11** provides for **SP10**, which describes how the number of JLCPCB components in stock must be a consideration within a component's trade-off analysis. Additionally, **SP11** describes where the component-specific symbols and footprints can be obtained. **AT09** confirms the aforementioned, verifying the files generated are JLCPCB compliant, and that there are sufficient components in stock.
- **T\_A11:** To ensure the power subsystem's concepts of operation are achievable without simulation testing, **SP01** specifies that the use of integrated circuits in the power subsystem design must contain comprehensive and accurate documentation, supplied by Texas Instruments. This is associated with **SP13**, which states that each micro-system should not interfere with the operational concepts of the subsystem as a whole. These specifications are confirmed by conducting **AT11**, where the interference between the power distribution and power availability microsystems are quantitatively evaluated.
- **T\_A12:** To maximize the discharge time of the battery **SP07**, states that 10mA is the maximum current to be drawn from the battery when the power subsystem is on, but not in operation. This is verified in **AT04**, which determines the quiescent current drawn by the power subsystem.
- **T\_A13:** Ensuring the driver circuits can operate the brushed DC motors as outlined in **FR04**, the specification **SP12** outlines the control features that the driver circuitry must exert on the motors, using the supplied input PWM signals. This is tested and verified in **AT12**, by gauging the acceptable performance of the driver circuit in verifying the exhibited speed and directional control.

# Chapter 3

## Subsystem Design

### 3.1 Design Decisions

#### 3.1.1 Final Design

##### α) Power Distribution Micro-system

The design procedure shown below is initiated with a trade-off analysis of the various proposed solutions that achieve the functionality outlined in traceability analyses; **T\_A04**, **T\_A05** and **T\_A13**, which is shown below in [Table 3.1](#), thereafter the justification for the design decision is stated, and its implementation is described.

| Parameters    | $r_{DS_{on}}$ (mΩ) | PWM compatible | Price(\$) | Extended? | JLCPCB stock | $I_Q$ (mA) |
|---------------|--------------------|----------------|-----------|-----------|--------------|------------|
| Components    |                    |                |           |           |              |            |
| DRV8837       | 280                | Yes            | 0.1235    | Yes       | 277802       | 0.6        |
| DRV8833       | 360                | Yes            | 0.6660    | Yes       | 9436         | 3          |
| Weight factor | 1                  | 1              | 2         | 3         | 2            | 1          |

Table 3.1: Comparison of Motor Driver Integrated Circuits for the Power Distribution Micro-system

[Table 3.1](#) above was populated using the component's respective; data-sheet values [\[3, 4\]](#) and JLCPCB/partdetail webpage. Noting that the DRV8833 has two driver circuits and the DRV3388 only has one, the following component price calculation is conducted, where the extended component fee of approximately \$3 is only paid once. The price point comparison is shown below:

DRV8833 costs:  $\$0.666 + \$3 = \$3.666$  whereas, DRV8837 costs:  $2 \times \$0.1235 + \$3 = \$3.247$ .

The internal MOSFET (high and low side) on-state resistance of the driver circuits, compared above are similar but non-negligible, such that the DRV8833 would negatively impact the efficiency of the micro-system. Furthermore, the efficiency of the micro-mouse would be impacted by the large quiescence current drawn from the DRV8833. Lastly, the number of JLCPCB components in stock is large for both driver circuits and does not affect the design decision. With the deterministic factors presented above and the weighting factors prescribed from [Table 2.2](#) the selection of **DRV8837** as the functional IC was made to execute the power distribution micro-systems operation.

##### β) Power Availability Micro-system

This micro-systems design was guided by traceability analysis **T\_A03**. Initially, an idealized design was considered, and research [\[1\]](#) was conducted into implementing a Sigma-Point Kalman filter for SoC estimation. This proved to be; outside the scope of an undergraduate course, and outside the scope of this micro-system as it supplies a digital SoC estimation. Thereafter, consideration was given to designing circuitry implementing coulomb counting through the use of a current sensor with a sense resistor whose output is fed into an op-amp integrator and supplied to the ADC of the  $\mu$ C. This design was not implemented due to the limited knowledge of Control Theory required to correctly implement the op-amp integrator. The specification that the analog SoC voltage signal supplied to the  $\mu$ C's ADC must be less than 3.6V [\[2\]](#), is achieved by considering the largest input voltage this micro-system can receive from the 3.7V LiPo battery is, 4.2V. Therefore, the desired attenuation is calculated as  $\frac{3.7}{4.2} \approx 0.881$ , and by modeling this attenuation as a voltage divider circuit the resistance ratio is calculated with a margin of error included to be  $\frac{1.2}{1.2+0.3} \frac{M\Omega}{M\Omega} = 0.8$ . These resistor values are chosen in the  $M\Omega$  range to reduce the current drawn by the subcircuit and are comprised of standard E24 resistors in series.

A passive low pass filter is implemented at the output of the voltage divider with  $R = 10k\Omega$  and  $C = 2.2\mu F$ , providing a cutoff frequency of  $f_c = (2\pi \times 10 \times 10^3 \times 2.2 \times 10^{-6})^{-1} \approx 7.23 \text{ Hz}$  which refines the SoC signal by removing high-frequency noise and interference.

However for the voltage divider to be a stable attenuation circuit, the current output should be zero. This warrants the inclusion of an operational amplifier (op-amp) in a non-inverting voltage follower configuration whose input impedance is high enough to consider the current flowing out of the voltage divider to be approximately zero. The added benefit of the op-amp is that it buffers the sensitive analog SoC signal source from the  $\mu\text{C}$ 's ADC. Below in [Table 3.2](#), the three op-amps that were considered are compared, thereafter the justification for the design decision is stated, and its implementation is described.

| Parameters           | single supply voltage <sub>min</sub> [V] | $Z_{in}(M\Omega)$ | Price(\$) | Extended? | JLCPCB stock | $I_Q(\text{mA})$ |
|----------------------|--|-------------------|-----------|-----------|--------------|------------------|
| <b>Components</b>    |  |                   |           |           |              |                  |
| LM321                | 2.7                                      | 35                | 0.1067    | Yes       | 57175        | 0.13             |
| LM2904               | 3.0                                      | 10                | 0.0893    | Yes       | 102761       | 0.46             |
| OP07                 | 6.0                                      | 30                | 0.1473    | No        | 128499       | 1.65             |
| <b>Weight factor</b> | <b>1</b>                                 | <b>1</b>          | <b>2</b>  | <b>3</b>  | <b>2</b>     | <b>1</b>         |

Table 3.2: Comparison of OPAMPS the Power Availability Micro-system

[Table 3.2](#) above was populated using the component's respective; data-sheet values [\[5, 6, 7\]](#) and JLCPCB/-partdetail webpage. The budget of the subsystem was initially the chief concern and thus, the best option was the OP07, as it is not an extended part. OP07's data-sheet states the component has a minimum supply voltage of  $\pm 3\text{V}$ . This was glossed over and assumed to be the single supply rail minimum voltage, due to expediency valued higher than meticulousity, as described in the limitations of [section 1.2](#). When this error was discerned, the comparison [Table 3.2](#), was utilized to find a replacement. In contrasting the LM321 and LM2904, the difference in cost and the number of components in stock at JLCPCB was considered negligible. The differential factors between these two opamps are their input impedance  $Z_{in}$  and quiescence current  $I_Q$ ; of which the LM321's higher input impedance is valued to improve the sensitivity of the SoC signal fulfilling the core requirement of this micro-system. The low quiescent current drawn by the LM321 is also favorable, improving the efficiency of the micro-system, which led to the design decision to implement **LM321** as the operational amplifier fulfilling the operational concepts of the power availability micro-system.

### $\gamma$ Power Supply Charging Micro-system

The design procedure shown below is initiated with a trade-off analysis of the various proposed solutions that achieve the performance criterion outlined in traceability analysis **T\_A02**, which is shown below in [Table 3.3](#), thereafter the justification for the design decision is stated, and its implementation is described.

| Parameters           | $I_{prog\max}(A)$ | ESD ( $V_{rated}$ ) | Protection | Price(\$) | Extended? | JLCPCB stock | $I_Q$ (mA) |
|----------------------|-------------------|---------------------|------------|-----------|-----------|--------------|------------|
| <b>Components</b>    |                   |                     |            |           |           |              |            |
| MCP73831             | 0.5               | $\pm 400$           | High       | 0.7590    | Yes       | 8101         | 1.5        |
| TP4056               | 1.0               | -                   | low        | 0.1724    | No        | 100891       | 0.5        |
| BQ24092              | 1.0               | $\pm 1500$          | High       | 0.7605    | Yes       | 1485         | 1.0        |
| <b>Weight factor</b> | <b>1</b>          | <b>1</b>            | <b>2</b>   | <b>2</b>  | <b>3</b>  | <b>2</b>     | <b>1</b>   |

Table 3.3: Comparison of Integrated Circuits for the Power Supply Charging Micro-system

[Table 3.3](#) above was populated using the component's respective; data-sheet values [\[8, 9, 10\]](#) and JLCPCB/part-detail webpage. In accordance with the limited budget, the TP4056 appeared initially to be the ideal choice for the micro-systems charging IC, as it is not an extended part. However, due to the limited documentation and the low protection features other solutions were considered.

The difference in the price point and quiescence current drawn between the BQ24092 and the MCP73831 is reasonably unimportant concerning their functional capabilities. These ICs have robust protection features, including; input overvoltage protection, thermal regulation and shutdown protection, and output short circuit protection. Empirically, the CDM Electrostatic Discharge (ESD) rating, is an important differentiating parameter in this decision, as additional TVS diodes would need to be included if the ESD voltage rating is not sufficiently high, such as in the case of the MCP73831. In light of the aforementioned, and noting that the MCP73831 has a low maximum programmable output current  $I_{prog_{max}}$  of only 500mA led to the design decision of implementing the **BQ24092**, as the charging IC to fulfill this micro-systems concept of operation. The number of components in stock at JLCPCB was considered, but the ESD rating &  $I_{prog_{max}}$  parameters' importance superseded this consideration.

### δ) Power Isolation Micro-system

The design of this micro-system was synthesized in line with traceability analysis **T\_A01** and below in [Table 3.4](#) various latching switch solutions to this micro-systems design are compared and contrasted. Thereafter, the rationale for the solution implemented in the final design is explained. [Table 3.4](#) below was populated using the component's respective; data-sheet values [\[11\]](#),[\[12\]](#),[\[13\]](#), [\[14\]](#) and JLCPCB/partdetail webpage. In conducting

| Parameters           | Contact Resistance (mΩ) | Operating Life(cycles) | PCB <sub>assembly</sub> | Price(\$) | Extended? | JLCPCB stock |
|----------------------|-------------------------|------------------------|-------------------------|-----------|-----------|--------------|
| <b>Components</b>    |                         |                        |                         |           |           |              |
| SPUN192600           | 40                      | $10^4$                 | TH                      | 0.9405    | Yes       | 112          |
| SPEF110100           | 100                     | $3 \times 10^3$        | TH                      | 1.1430    | Yes       | 312          |
| 2AS3T1A1M2QES        | 20                      | $3 \times 10^3$        | TH                      | 1.4985    | Yes       | 44           |
| 2BS3T1A1MZQES        | 20                      | $3 \times 10^3$        | SMD                     | 2.0250    | Yes       | 334          |
| <b>Weight factor</b> | <b>2</b>                | <b>1</b>               | <b>3</b>                | <b>3</b>  | <b>2</b>  | <b>3</b>     |

Table 3.4: Comparison of Switches for the Power Isolation Micro-system

**AT09**, it was observed that any Through-Hole (TH) components incur a hand soldering fee of around 3\$ when JLCPCB is assembling the PCB. This removed most of the options in [Table 3.4](#) above due to the budget constraint. Thereafter, consideration was given to constructing a soft-latching power switch circuit [\[15\]](#), which was ultimately abandoned due to the added complexity and uncertainty it introduced. Ultimately, given that the 2BS3T1A1MZQES is assembled as a Surface Mount Device (SMD) and is additionally a SPST (on-off-on) latching switch with very low contact resistance. It can ensure zero current is drawn from the battery when switched off, and that the voltage drop across the series contact resistance is minimized. For these reasons, the **2BS3T1A1MZQES** was chosen to achieve the functionality of this micro-system. There are several concerns regarding this design decision. Firstly, The total component cost is exorbitant placing pressure on the power subsystem budget. Additionally, the number of components JLCPCB has in stock is unsettling, which may result in the client receiving the assembled PCB that is unable to meet the user's requirements. Lastly, the component weight is a very specific limitation of this design decision however, the PCB placement of this component may mitigate the effect this drawback has, on the micro-mouse's ability to turn effectively.

The final design of the power subsystem is displayed below in schematic form in [Figure 3.1](#), and the front and back PCB are shown in [Figure 3.1a](#) and [Figure 3.1b](#). Additionally, a 3d rendering of the PCB is shown in [Figure 3.1c](#) below.

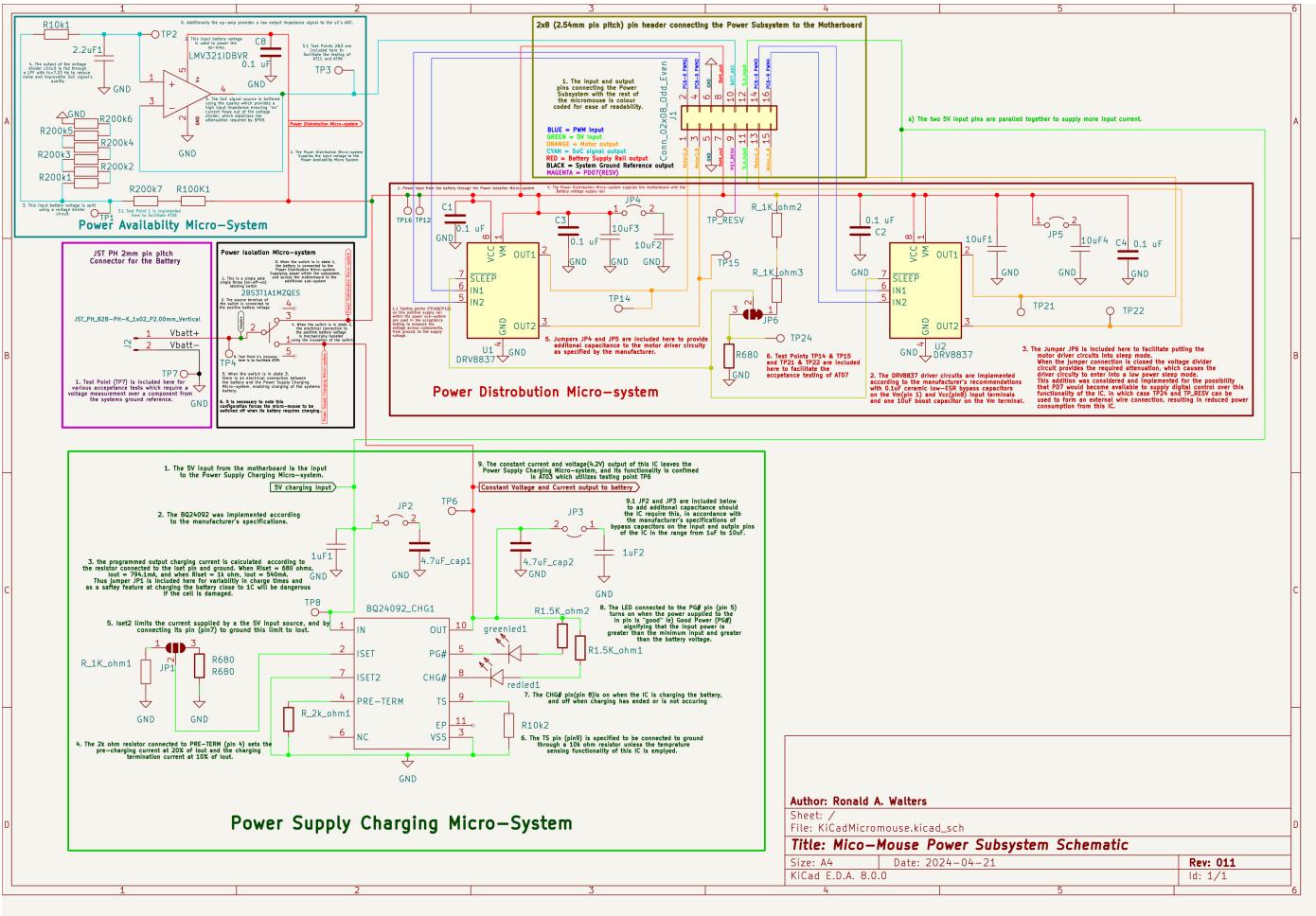


Figure 3.1: Schematic

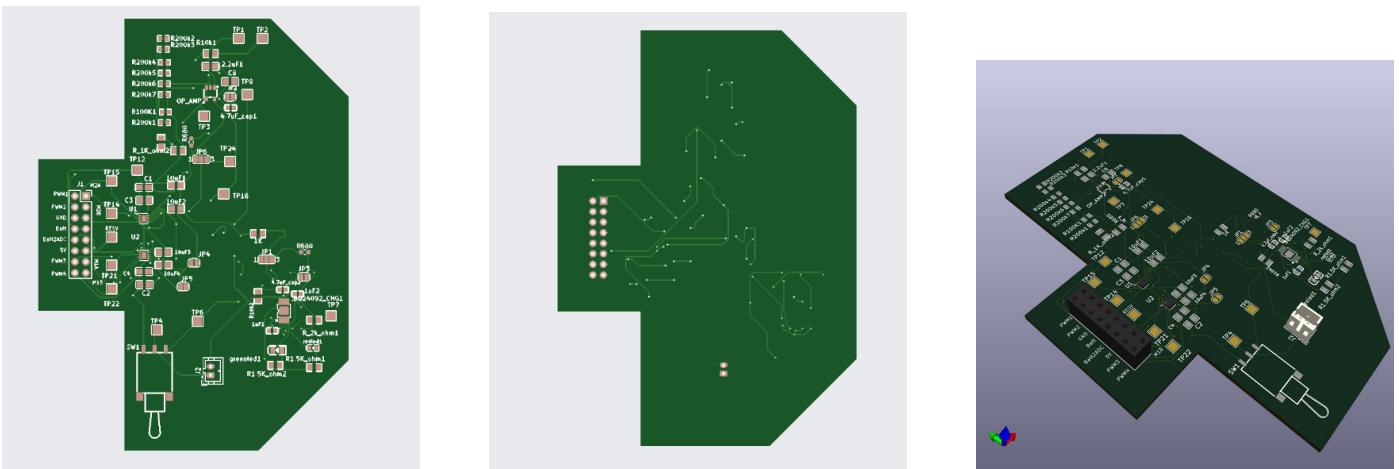


Figure 3.2: PCB

## 3.2 Failure Management

Below in table [Table 3.5](#), the failure management strategies implemented are discussed.

Table 3.5: Failure Management Strategies

| Name                         | Description   |
|------------------------------|---|
| 4mm <sup>2</sup> Test Points | The size of these test points facilitates a failure management strategy that increases the accessibility to the circuitry within the PCB, allowing for external wire placement to contravene faulty components.   |
| signal interference          | Ensuring that the high-frequency switching signals' electromagnetic radiation does not interfere with the sensitive analog signals meant running their respective traces in a manner, ensuring that at no point do they cross over each other while ensuring the trace spacing between signal lines was maintained. |
| Thermal Considerations       | The multiple IC's on the power sub-system PCB, facilitated the implementation of thermal management. This was achieved through the use of space on the PCB, ensuring that the components which would heat up, would be able to operate without the additional heat of nearby components.                            |
| ERC & DRC                    | These functionalities in KiCad were utilized in accordance with the JCLPCB's manufacturing and assembly capabilities <a href="#">[16]</a> .   |

## 3.3 System Integration and Interfacing

To integrate the power subsystem with the rest of the system the [Table 3.6](#) below was constructed, followed by a high-level block diagram.

Table 3.6: Interfacing specifications

| Interface | Description   | Pins/Output  |
|-----------|---|--|
| I001      | Power Subsystem to Two Brushed DC motors, for speed and direction control | <ul style="list-style-type: none"> <li>• Pin 1 to Motor2_A</li> <li>• Pin 3 to Motor2_B PB15</li> <li>• Pin 13 to Motor1_A PB13</li> <li>• Pin 15 to Motor1_B</li> </ul> |
| I002      | PWM from $\mu$ C through the motherboard                                  | <ul style="list-style-type: none"> <li>• PC6 to Pin 2</li> <li>• PC7 to Pin 4</li> <li>• PC8 to Pin 14</li> <li>• PC9 to Pin 16</li> </ul>                               |
| I003      | SoC signal to $\mu$ C's ADC   | <ul style="list-style-type: none"> <li>• Pin 10 to <math>\mu</math>C</li> </ul>  |
| I004      | Battery voltage to motherboard  | <ul style="list-style-type: none"> <li>• Pin 11 to motherboard</li> <li>• Pin 12 to motherboard</li> </ul>   |
| I005      | Sysntem ground reference to motherboard                                   | <ul style="list-style-type: none"> <li>• Pin 5 to motherboard</li> <li>• Pin 6 to motherboard</li> </ul>   |

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