

# Anh Tran

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## EDUCATION

<b>University of Pennsylvania</b> , M.S.E in Electrical Engineering - GPA: 3.91/4.0	Sep 2024 – May 2026
<b>Relevant coursework:</b> System-on-a-Chip Architecture, HW/SW Co-Design for ML, General-Purpose GPU Architecture & Programming, Computer Organization & Design, Digital IC & VLSI Fundamentals, Graph Neural Networks	
<b>VinUniversity</b> , B.Sc in Electrical Engineering - GPA: 3.83/4.0	Sep 2021 – Jun 2025
<b>Relevant coursework:</b> Digital Logic & Computer Organization, Computer System Programming, Artificial Intelligence, Natural Language Processing, Digital Signal and Image Processing	

## RESEARCH EXPERIENCE

<b>Research Assistant   A Dedicated MicroBlaze SoC for Deep Neural Networks   EDABK LAB</b>	Jul 2025 – Present
<b>Supervised by:</b> Assoc. Prof. Duc Minh Nguyen	
<ul style="list-style-type: none"><li>Developed a custom System-on-Chip (SoC) on the UltraScale+ ZCU104 featuring a MicroBlaze soft processor, with full support for DDR4, UART, and GPIO interfaces.</li><li>Actively working on deploying convolutional neural network (CNN) models on FPGA and integrating the accelerator into the custom SoC architecture.</li></ul>	
<b>Research Assistant   Federated Learning for Graph-based ICD auto coding   VinUniversity</b>	Jul 2025 – Present
<b>Supervised by:</b> Assistant Prof. Danh Cuong Do	
<ul style="list-style-type: none"><li>Leveraged Graph Neural Networks to enhance the diagnosis of International Classification of Diseases (ICD) codes in language models.</li><li>Ongoing effort to develop a federated learning architecture that supports collaborative training across multiple hospital clients while preserving data privacy and training efficiency.</li></ul>	
<b>Research Assistant   Implicit Deep Learning   VinUniversity</b>	May 2024 – Oct 2024
<b>Supervised by:</b> Prof. Laurent El Ghaoui	
<ul style="list-style-type: none"><li>Designed experiments to verify and evaluate the generalization performance of implicit models across various architectures (fully connected, residual, attention-based, RNNs), a new class of deep learning models proposed by Laurent El Ghaoui.</li><li>Explored and deployed various solvers (MOSEK, ADMM, and projected gradient descent) for fixed-point equations, a key component in training implicit models.</li><li>Examined the sparsity and representational capacity of implicit models by analyzing patterns in weight matrices.</li></ul>	
<b>Research Assistant   Satellite Imagery Super-resolution for Carbon Stocks Estimation   VinUniversity</b>	Mar 2024 – Oct 2024
<b>Supervised by:</b> Assoc. Prof. Nidal Kamel	
<ul style="list-style-type: none"><li>Utilized deep learning methods to super-resolve satellite images, incorporating dynamic high-pass filtering and channel attention to enhance image generation.</li><li>Trained an image super-resolution model using data from Vietnam's mountainous and forest regions; used quality-enhanced images as input for a carbon stock estimator, integrating neural networks to refine predictions.</li></ul>	

## PROFESSIONAL EXPERIENCE

<b>AI/Data Engineer Intern   AlphaAsimov Robotics</b>	Mar 2024 – Oct 2024
<ul style="list-style-type: none"><li>Performed data preprocessing and analysis to ensure readiness for AI model training; assessed the alignment of various modalities (camera, LIDAR, SONAR, IMU, GPS, etc.) in the dataset.</li><li>Designed tools using Python and Bash scripting, to streamline and partially automate the data verification process, incorporating anomaly detection models and descriptive visualizations.</li></ul>	

## TEACHING EXPERIENCE

<b>ESE 5060: Introduction to Optimization Theory   University of Pennsylvania</b>	Fall 2025
<ul style="list-style-type: none"><li>Responsibilities included answering students' online questions, grading homework, and grading/proctoring exams</li></ul>	
<b>CIS 5710: Computer Organization &amp; Design   University of Pennsylvania</b>	Spring 2026
<ul style="list-style-type: none"><li>Incoming responsibilities include answering students' online questions, holding office hours, and grading exams</li></ul>	

## PROJECTS

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<b>High-Performance CUDA Kernel for CSR-Dense Matrix Multiplication</b>	Oct 2025 – Present
<ul style="list-style-type: none"><li>Designed a custom Compressed Sparse Row (CSR) × dense CUDA kernel with an optimized thread layout for coalesced access and minimized bank conflicts, along with shared-memory tiling to improve data reuse.</li><li>Achieved up to <math>1.5\times</math> speedup over cuSPARSE and <math>1.39\times</math> speedup over torch.sparse baseline.</li><li>Ongoing effort to explore additional optimization strategies, including load-balancing schemes across warps/threads and alternative work partitioning to further accelerate the kernel.</li></ul>	
<b>System-on-Chip (SoC) Design for Real-Time Data Deduplication and Compression</b>	Oct 2025 – Dec 2025
<ul style="list-style-type: none"><li>Developed a comprehensive deduplication-compression pipeline integrating content-defined chunking (CDC), SHA-256-based hashing, and LZW (Lempel-Ziv-Welch) compression.</li><li>Enhanced cryptographic hashing performance through ARM NEON SIMD intrinsics and implemented a FPGA-based hardware accelerator for LZW.</li><li>Demonstrated system-level performance exceeding 800 Mb/s throughput with a 0.65 compression ratio on Ultra96-V2 platform.</li></ul>	
<b>Pipelined RISC-V Processor</b>	Jan 2024 – May 2025
<ul style="list-style-type: none"><li>Developed a custom 32-bit RISC-V core using SystemVerilog with a fully pipelined datapath, incorporating multicycle operators, direct-mapped instruction and data caches, and AXI4-Lite protocol for streamlined memory communication.</li><li>Synthesized using the Yosys toolchain and deployed on Lattice ECP5 FPGA, achieving a 31MHz maximum clock frequency with resource utilization of 30.9% LUTs and 4.1% flip-flops.</li></ul>	
<b>Fast, Compact and Efficient DNN via Pruning and Sparse Matrix Compression</b>	Oct 2024 - Dec 2024
<ul style="list-style-type: none"><li>Explored various pruning strategies (global, channel-wise, hard pruning), combined with quantization, to reduce model size while maintaining accuracy and accelerating inference.</li><li>Developed custom sparse linear layer leveraging Compressed Sparse Row (CSR) format for efficient storage and inference.</li><li>Achieved a <math>1.52\times</math> speedup in the most pruned layer and reduced the model size by 43% on VGG16 architecture.</li></ul>	
<b>Configurable Logic Block (CLB) Design and Optimization</b>	Oct 2024 - Dec 2024
<ul style="list-style-type: none"><li>Designed and verified a transistor-level 16-bit CLB circuit using 45nm Salicide CMOS technology in the Cadence environment.</li><li>Performed transistor sizing, mitigated timing hazards, and optimized the circuit for minimal delay and improved energy efficiency.</li><li>Achieved a maximum operating frequency of 1 GHz and an average power consumption of <math>134.9\mu\text{W}</math>.</li></ul>	

## SKILLS & INTERESTS

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**Programming Languages:** C/C++, Python, Verilog/SystemVerilog, CUDA, MATLAB, Shell Scripting

**Hardware Platforms:** Avnet Ultra96-V2, Xilinx PYNQ-Z2, Xilinx ZCU104, ULX3S

**Hardware Design Tools:** Vitis HLS, Vivado Design Suite, Cadence Toolchain

**Frameworks:** OpenCL, PyTorch, TensorFlow, TensorRT, JAX, OpenCV, ROS2

**Software Tools:** Linux, Git, Docker, CUDA Toolkit

**Focus Areas:** Configurable Computing, GPU Computing, Hardware/Software Co-Design, ML Systems

## HONORS & ACHIEVEMENTS

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<b>Vingroup Science &amp; Technology Scholarship</b> , Full funding for Master's study at the University of Pennsylvania.	2024
<b>Excel Award for Exceptional Capability</b> , VinUniversity	2023
<b>Dean's List</b> , VinUniversity	2021 – 2024
<b>Undergraduate Merit-based Full-Tuition Scholarship</b> , VinUniversity	2021
<b>First Prize</b> , Vietnamese National Physics Competition for High School Students	2020
<b>Gold Medal</b> , Physics Competition for Specialized Students in the Northern Delta and Coastal Areas in Vietnam	2019