Abdallah Hashem

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OBJECTIVE

Experienced Electrical & Computer Engineer with a focus on RTL design, SoC, Computer Architecture, and Validation. Seeking a Design / Computer Architecture / Validation Engineer role to contribute to groundbreaking silicon chip initiatives. Skilled in Verilog, Python, and complex ASIC product development.

EDUCATION

University of California, Davis
Master of Science, Electrical & Computer Engineering
Thesis: *Hardware Security: A Comprehensive Study of Counteracting Side-Channel Attacks, SAT attacks, Reverse Engineering, and Hardware Trojans*

University of California, Davis
Bachelor of Science, Electrical Engineering | Minor Technology Management | Dean's list
Emphasis: System on Chip (SoC) Design, Computer Architecture, Layout Design

ENGINEERING EXPERIENCE

IC Validation Engineer - Audio, Qualcomm, Tempe, AZ July 2023 – Present

- Launched new Audio SoC products, **Qualcomm S7 Gen 1 and Qualcomm S5 Gen 2,** seamlessly integrated into cutting-edge premium-tier headphones
- Lead rigorous co-existence validation of various technologies including Wi-Fi, analog and digital audio, Bluetooth (BT), auxiliary, charger, I2S, PCM, and SRAM interactions on System on Chip (SoC) for usage cases
- Design and implement detailed test strategies including debugging, data collection, and analysis for comprehensive validation, expediting customer product sampling
- Automate test scripts using python to improve test coverage and enable parallel testing of multiple devices, resulting in a remarkable 91% reduction in testing time
- Validate PMU, AUX, and BT LDOs at block-level across temperature
- Collaborate with cross-functional teams, including design, system, applications, and firmware teams, to optimize device KPMs
- Skillfully collaborate across multiple geographic regions, India, US, UK, and Taiwan, ensuring efficient coordination

Audio Evaluation and Optimization Intern, Qualcomm, Tempe, AZ June 2022 – Sep 2022

- Submitted an Invention Disclose Form (IDF) for a revolutionary application of 5G technology
- Evaluated audio TXADC and HSDAC of Total Harmonic Distortion, signal to noise ratio, dynamic range, and noise
- Led a top team in 5G intern hackathon, demonstrating strong innovation and teamwork
- Automated Audio testing process and results generation with python anad R, reducing testing time by 70%

Performance Engineering Intern, Maxeon Solar Technologies, Davis, CA May 2021 – June 2022

- Modeled and simulated cracked and un-cracked cells using Griddler and AutoCAD
- Performed flash & electroluminescence testing and analysis on unreleased development products
- Characterized degradation factor of interdigitate back contact cells (IBC), and IR analysis to minimize error rates to < 5%

RESEARCH

Graduate Research Assistant, Professor Houman Homayoun, UC Davis Sep 2022 – July 2023

- Conducted in-depth research involving digital design, advanced research, and analysis techniques to protect circuits from side-channel attacks, SAT attacks, hardware trojans, and reverse engineering
- Participated in the peer review process of MWSCAS and GLSVLSI conferences hosted by IEEE and ACM

Published
2023 IEEE MWSCAS: Securing AI Hardware: Challenges in Detecting and Mitigating Hardware Trojans in ML Accelerators

LEADERSHIP

Google Developer Student Clubs at UC Davis – Founder & Lead Aug 2021 – June 2022

- Selected by Google to form a community of student developers at UC Davis as 1 of the 124 North American leads and grew community to over 100 members in 3 months
- Hosted a nation-wide Hackathon, 7 technical workshops, and 8 events with attendance ranging from 20 to 300 attendees

Space and Satellite Systems at UC Davis – Power Systems Lead Mar 2020 – June 2020

- Designed PCBs for UC Davis' first CubeSat using Eagle, Fusion 360, and KiCAD software
- Lead the power systems team of 30 members focused on solar power generation, battery circuitries, and mission power budget

SKILLS

- RTL Development**: Verilog, CDC, Timing, Logic synthesis, STA**
- Programming**: Python, C, MATLAB, UVM**
- Design**: SoC, ASIC Product Development, IO Protocols (APB,AHB,AXI), Low Power Design (DVFS, Static power reduction)**