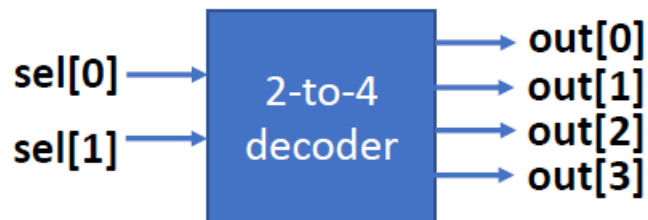


ECE-111 Advanced Digital Design Project

Homework-1:

- **For 2-to-4 decoder**, complete remainder of dataflow and behavioral model SystemVerilog code provided in Lab1 folder. Gatelevel model full code is provided. Review gatelevel model code.
- Synthesize behavioral, dataflow and gatelevel model of 2-to-4 decoder models one by one.
- Review Resource Usage Summary table under Analyze and Synthesis and see how many ALUT (Adaptive Look Up Tables are utilized and number of inputs to ALUT used to implement Boolean function)
- Simulate all three models separately using Modelsim-Altera and using same decoder testbench provided. Review simulation result.

Block Diagram and Truth Table of Decoder



Truth Table

sel[0]	sel[1]	out[3]	out[2]	out[1]	out[0]
0	0	0	0	0	1
0	1	0	0	1	0
1	0	0	1	0	0
1	1	1	0	0	0

- For Behavioral Model of Decoder :
 - See in above mentioned truth table values of sel[0] and sel[1] in each row and generate out[0], out[1], out[2], out[3] accordingly.
 - **Example** : 2'b00 : out = 4'b0001;

- For decoder dataflow model, implement using “assign” statements 4 boolean expressions for out[0], out[1], out[2], out[3] as shown below.
- Note :
 - for “.” Use logical “&&” operator
 - for use logical “!” operator
 - Example : **assign** out[0] = (!sel[0]) &&(!sel[1]);

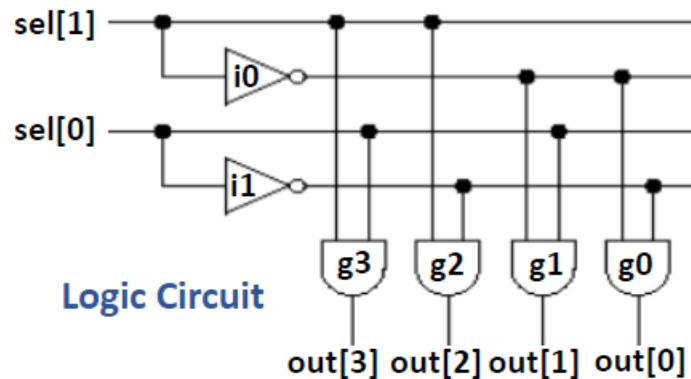
out[0] = $\overline{\text{sel[0]}}.\overline{\text{sel[1]}}$

out[1] = $\overline{\text{sel[0]}}.\text{sel[1]}$

out[2] = $\text{sel[0]}. \overline{\text{sel[1]}}$

out[3] = $\text{sel[0]}. \text{sel[1]}$

Boolean Expression



- **For 2-to-1 Mux and Full Adder**, review SystemVerilog code for behavioral level, dataflow level and gatelevel models provided in Labs1.zip folder
- Synthesize each of these representations of 2-to-1 MUX and Full Adder using Altera Quartus Prime
- Using Netlist viewer in Quartus Altera review RTL Viewer and Post technology mapping and fitting schematics.
- Review Resource Usage Summary table under Analyze and Synthesis and see how many ALUT (Adaptive Look Up Tables are utilized and number of inputs to ALUT used to implement Boolean function)
- Simulate using Modelsim-Altera any one of the models say behavioral model for Mux and FullAdder using its respective testbench provided. Review simulations waveform to confirm the behavior of multiplexer and FullAdder.
- Review resource usage summary and simulation waveform of all three implementations of MUX (gate level, dataflow and behavioral)
- Same mux_2x1_testbench.sv provided in Lab1.zip folder can be used to simulate mux_2x1_gate.sv, mux_2x1_dataflow.sv and mux_2x1_behavioral.sv implementations.

Lab1.zip folder has Mux, Fulladder full SystemVerilog code, partial code for Decoder and testbench files for all three designs.

Homework Report Submission Requirements :

Submit report on gradescope using canvas in pdf format which should include following mentioned :

- For Decoder behavioral and dataflow model provide SystemVerilog code snapshot. For MUX and FullAdder SystemVerilog code snapshot is not required in the report.
- For MUX, Decoder and FullAdder provide Snapshot of RTL and post-mapping schematics schematics generated from Altera Quartus Prime.
- Provide number ALUT's used, number of Boolean functions used for each design including number of input pins to ALUT used. Explain why 2 or 3 or N number ALUT's are used, why 2 or 3 or N number of Boolean functions implemented and why 2 or 3 or N number inputs to ALUT.
Note : For each design (MUX, decoder, FullAdder) one explanation is sufficient if gate level / behavioral and dataflow models of each design has same resource usage.
- Provide snapshot of simulation waveform generated from Modelsim, briefly explaining decoder, mux and FullAdder behavior.
Note : For each design (MUX, decoder, FullAdder) only one waveform snapshot is sufficient since gate level / behavioral and dataflow models of each design has same functional behavior.