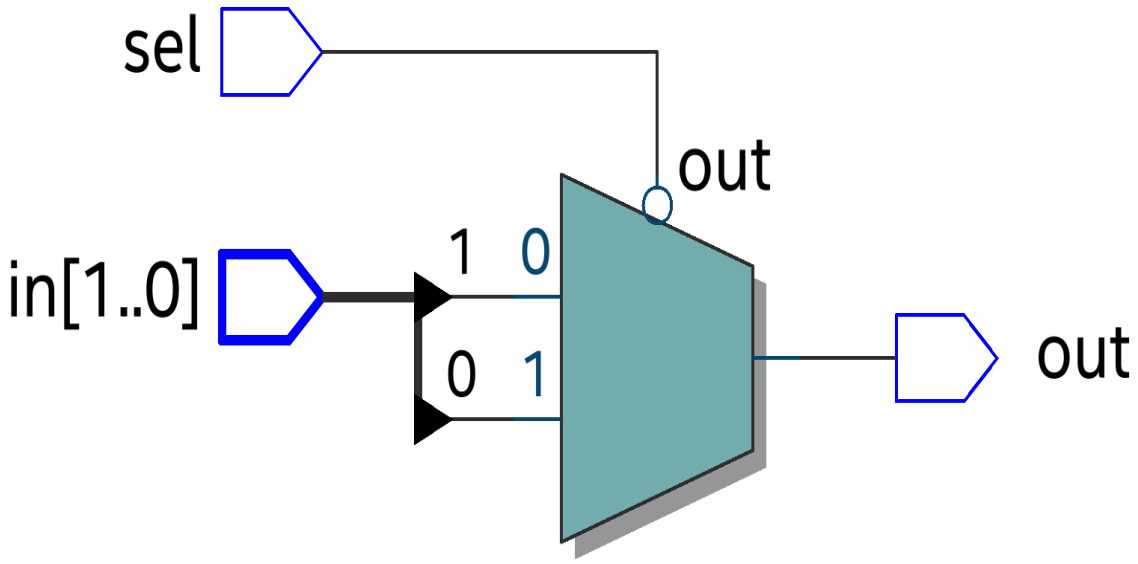
Sample Report HW0 ECE-111

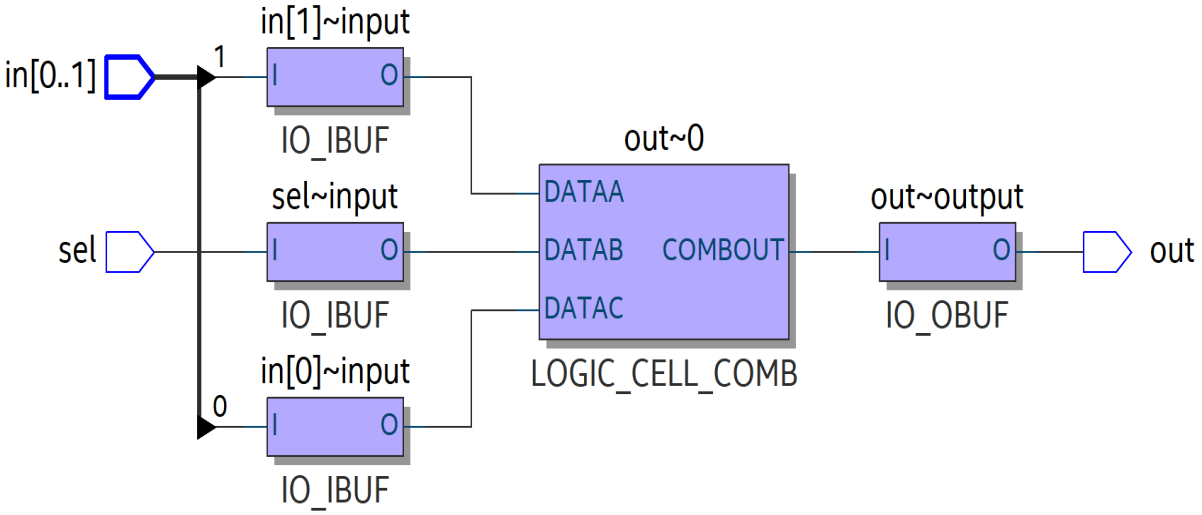
MUX 2x1

1. Behavioral level

a. RTL schematic



b. Post mapping schematic



c. Resource usage

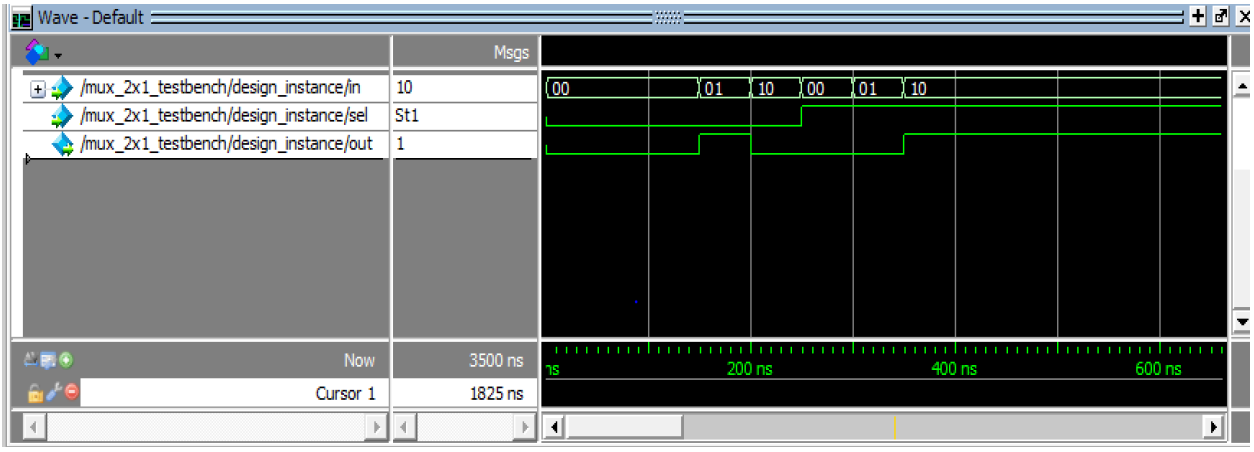
Analysis & Synthesis Resource Usage Summary

<<Filter>>

	Resource	Usage
1	Estimated ALUTs Used	1
1	-- Combinational ALUTs	1
2	-- Memory ALUTs	0
3	-- LUT_REGs	0
2	Dedicated logic registers	0
3		
4	Estimated ALUTs Unavailable	0
5		
6	Total combinational functions	1
7	Combinational ALUT ...by number of inputs	
1	-- 7 input functions	0
2	-- 6 input functions	0
3	-- 5 input functions	0
4	-- 4 input functions	0
5	-- <=3 input functions	1
8		
9	Combinational ALUTs by mode	
10		
11	Estimated ALUT/register pairs used	1
12		
13	Total registers	0
14		
15		
16	I/O pins	4
17		
18	DSP block 18-bit elements	0
19		
20	Maximum fan-out node	out~0
21	Maximum fan-out	1
22	Total fan-out	8
23	Average fan-out	0.80

Number of ALUT: 1 (4 I/O pins)
Simple 2:1 MUX design can be implemented using one ALUT
Number of Functions: 1 (3 input function)
For 2:1 MUX design, it requires only one 3 input function for implementation (2:1 MUX has 3 inputs including in_0, in_1 and sel, thus 3 inputs to ALUT)

d. Modelsim simulation results

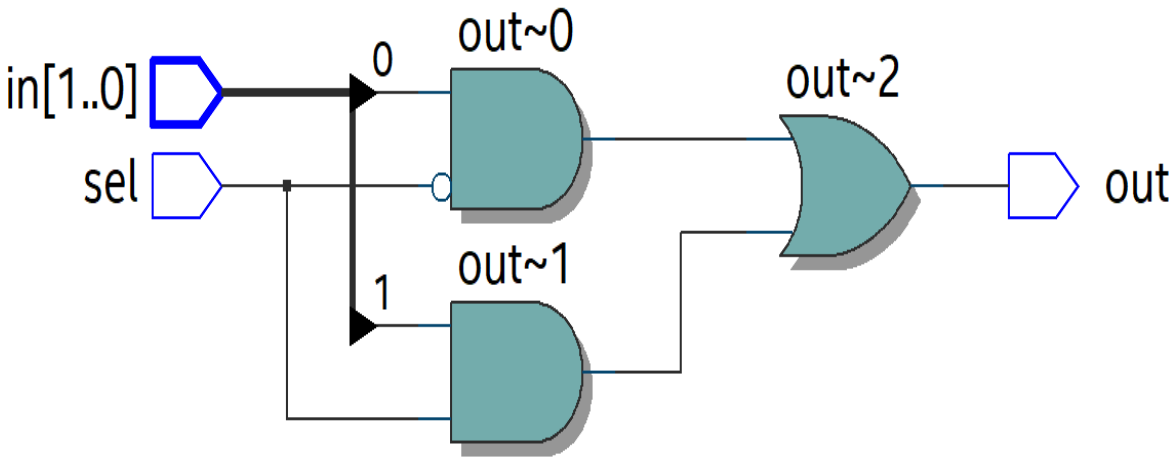


Transcript

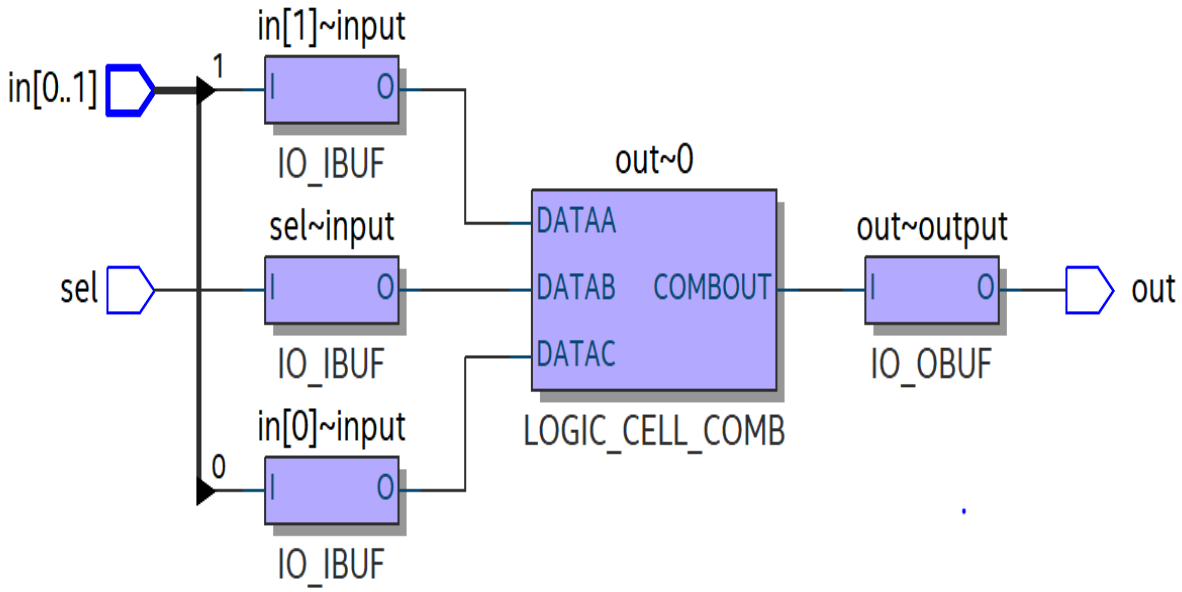
```
# End time: 21:57:26 on Oct 07,2019, Elapsed time: 0:00:00
# Errors: 0, Warnings: 0
ModelSim> vsim work.mux_2x1_testbench
# vsim work.mux_2x1_testbench
# Start time: 21:57:50 on Oct 07,2019
# Loading sv_std.std
# Loading work.mux_2x1_testbench
# Loading work.mux_2x1
add wave -position insertpoint sim:/mux_2x1_testbench/design_instance/*
VSIM 6> run
#  time=0,  in=00  sel=0  out=0
#
#  time=150,  in=01  sel=0  out=1
#
#  time=200,  in=10  sel=0  out=0
#
#  time=250,  in=00  sel=1  out=0
#
#  time=300,  in=01  sel=1  out=0
#
#  time=350,  in=10  sel=1  out=1
#
```

2. Dataflow level

a. RTL schematic



b. Post mapping schematic



c. **Resource usage**

Analysis & Synthesis Resource Usage Summary

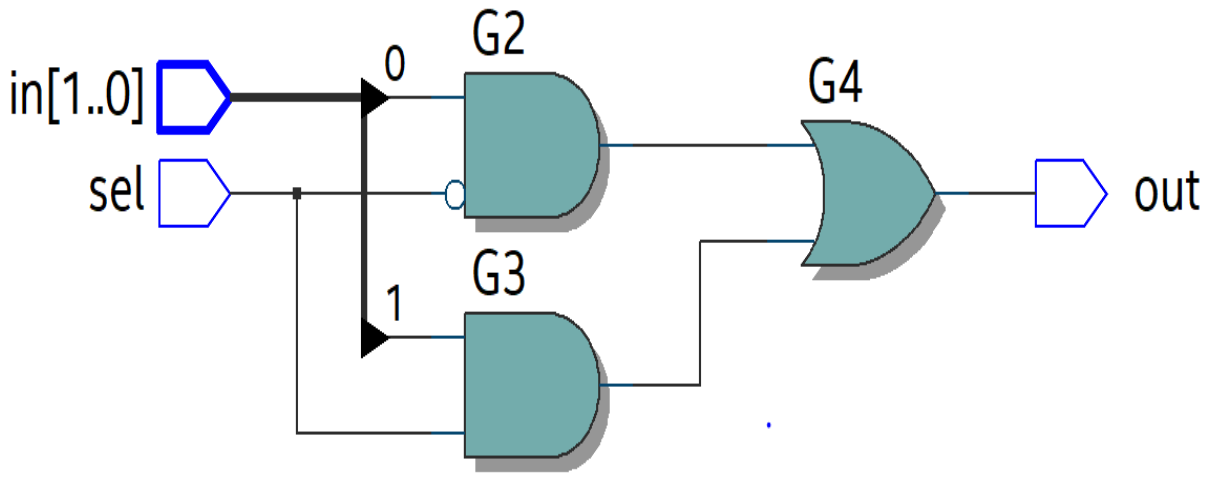
<<Filter>>

	Resource	Usage
1	Estimated ALUTs Used	1
1	-- Combinational ALUTs	1
2	-- Memory ALUTs	0
3	-- LUT_REGs	0
2	Dedicated logic registers	0
3		
4	Estimated ALUTs Unavailable	0
5		
6	Total combinational functions	1
7	Combinational ALUT ...by number of inputs	
1	-- 7 input functions	0
2	-- 6 input functions	0
3	-- 5 input functions	0
4	-- 4 input functions	0
5	-- <=3 input functions	1
8		
9	Combinational ALUTs by mode	
10		
11	Estimated ALUT/register pairs used	1
12		
13	Total registers	0
1	-- Dedicated logic registers	0
2	-- I/O registers	0
3	-- LUT_REGs	0
14		
15		
16	I/O pins	4
17		
18	DSP block 18-bit elements	0
19		
20	Maximum fan-out node	out~0

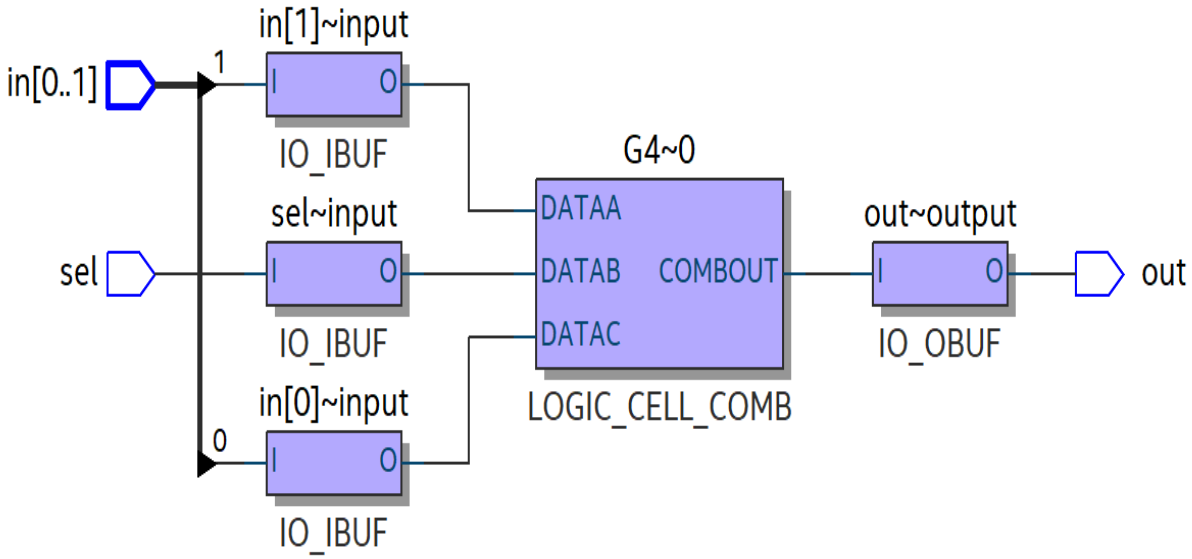
d. **Modelsim simulation result (same as behavioral level simulation result)**

3. Gatelevel

a. RTL schematic



b. Post mapping schematic



c. **Resource usage**

Analysis & Synthesis Resource Usage Summary

<<Filter>>

	Resource	Usage
1	Estimated ALUTs Used	1
1	-- Combinational ALUTs	1
2	-- Memory ALUTs	0
3	-- LUT_REGs	0
2	Dedicated logic registers	0
3		
4	Estimated ALUTs Unavailable	0
5		
6	Total combinational functions	1
7	Combinational ALUT ...by number of inputs	
1	-- 7 input functions	0
2	-- 6 input functions	0
3	-- 5 input functions	0
4	-- 4 input functions	0
5	-- <=3 input functions	1
8		
9	Combinational ALUTs by mode	
10		
11	Estimated ALUT/register pairs used	1
12		
13	Total registers	0
14		
15		
16	I/O pins	4
17		
18	DSP block 18-bit elements	0
19		
20	Maximum fan-out node	G4~0
21	Maximum fan-out	1
22	Total fan-out	8

d. **Modelsim simulation result (same as behavioral level simulation result)**