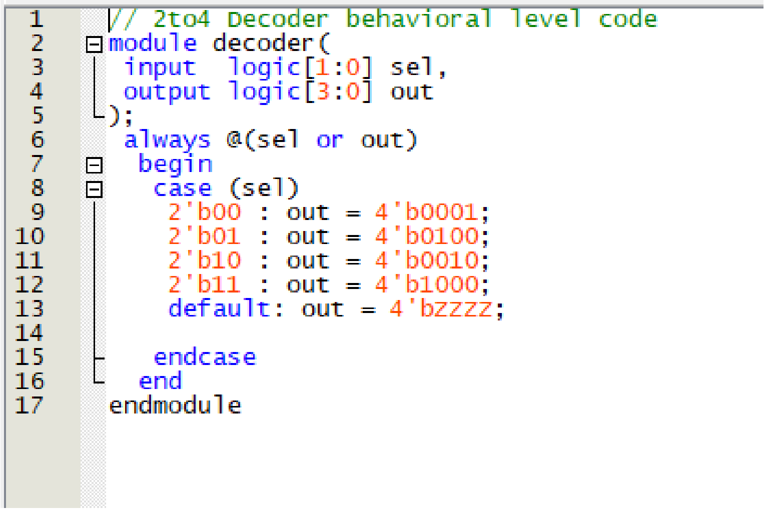
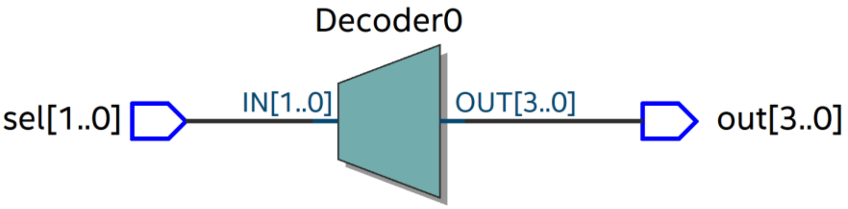
ECE 111 Winter 2022
HW1
Hao Le A15547504

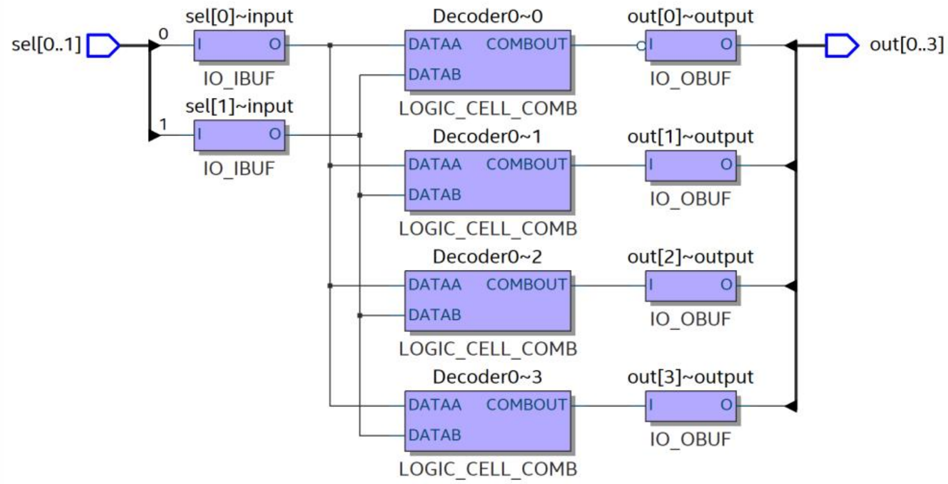
2-to-4 Decoder

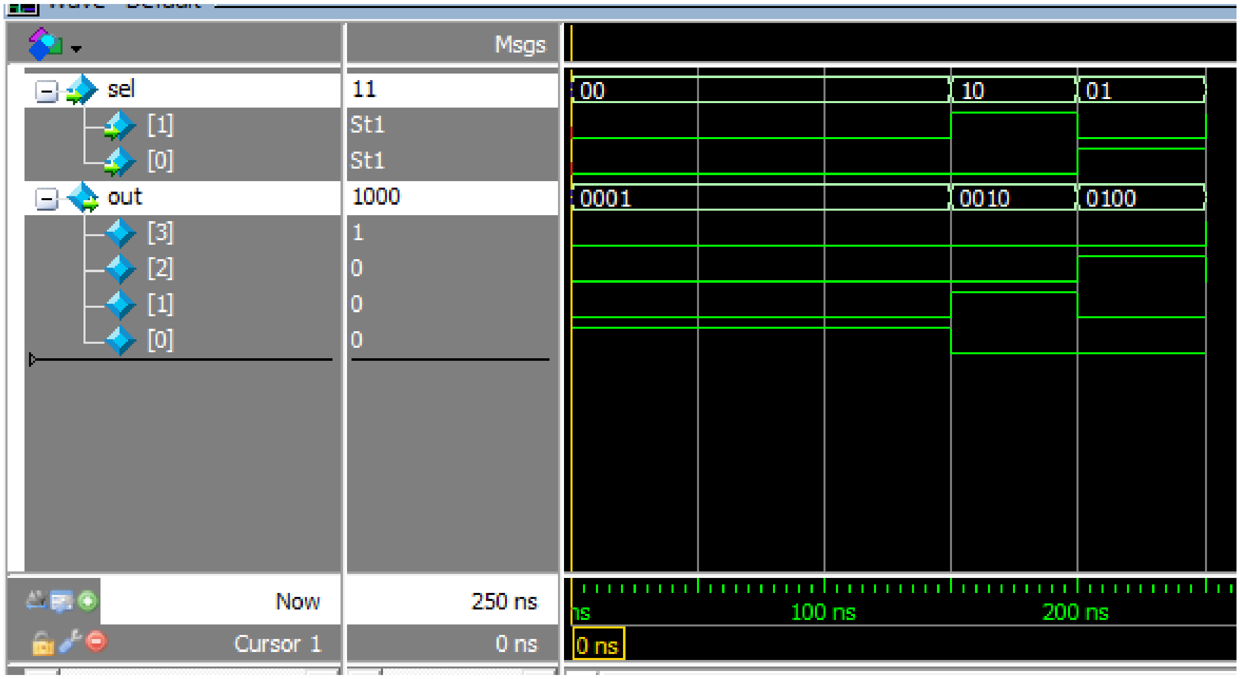
Behavioral Level



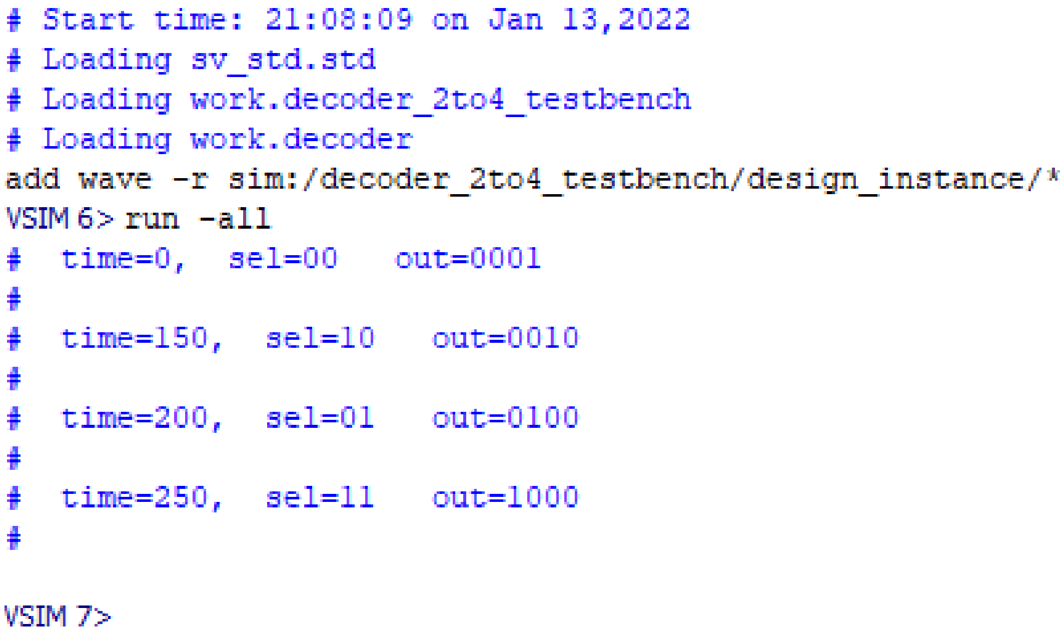
```
// 2to4 Decoder behavioral level code
module decoder(
 input  logic[1:0] sel,
 output logic[3:0] out
);
 always @(sel or out)
  begin
   case (sel)
    2'b00 : out = 4'b0001;
    2'b01 : out = 4'b0100;
    2'b10 : out = 4'b0010;
    2'b11 : out = 4'b1000;
    default: out = 4'bzzzz;

   endcase
  end
endmodule
```



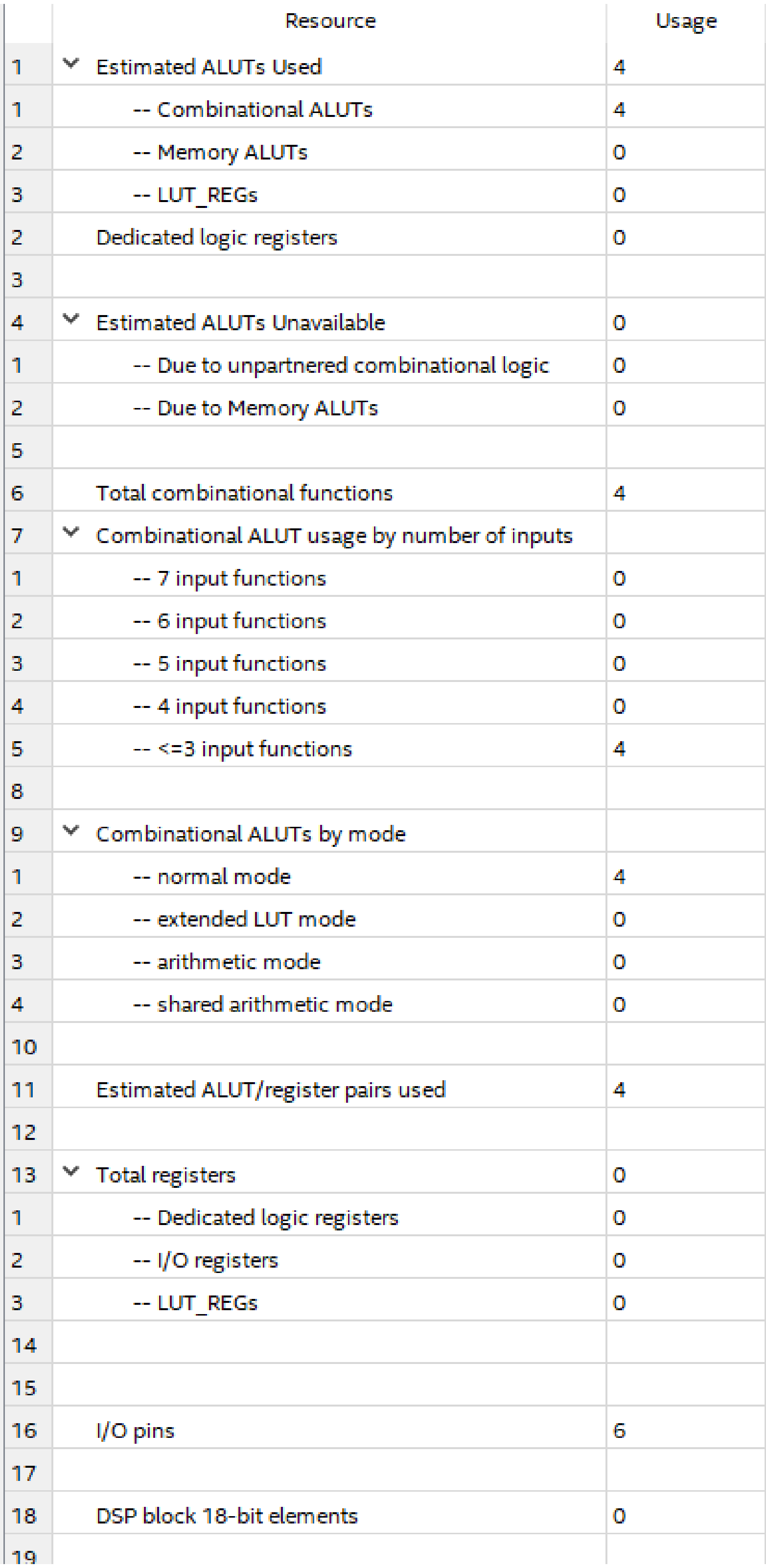




	Msgs
sel	11
[1]	St1
[0]	St1
out	1000
[3]	1
[2]	0
[1]	0
[0]	0
Now	250 ns
Cursor 1	0 ns

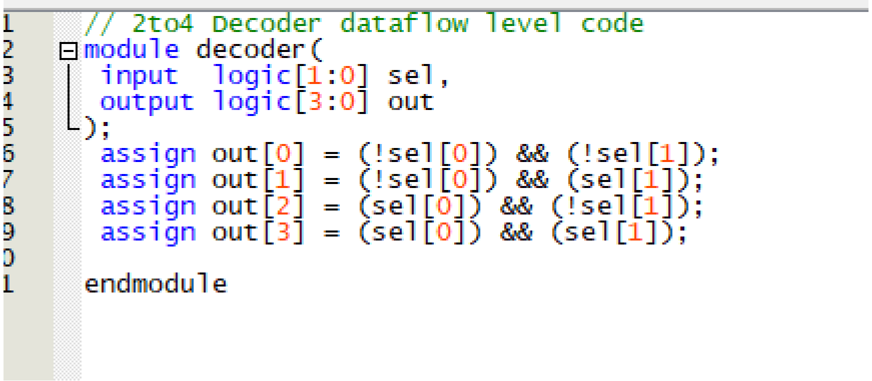


```
# Start time: 21:08:09 on Jan 13,2022
# Loading sv_std.std
# Loading work.decoder_2to4_testbench
# Loading work.decoder
add wave -r sim:/decoder_2to4_testbench/design_instance/*
VSIM 6> run -all
#  time=0,  sel=00   out=0001
#
#  time=150,  sel=10   out=0010
#
#  time=200,  sel=01   out=0100
#
#  time=250,  sel=11   out=1000
#

VSIM 7>
```

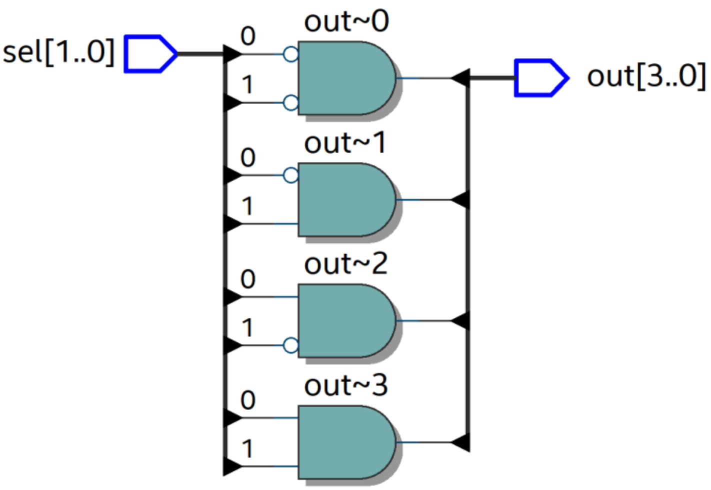


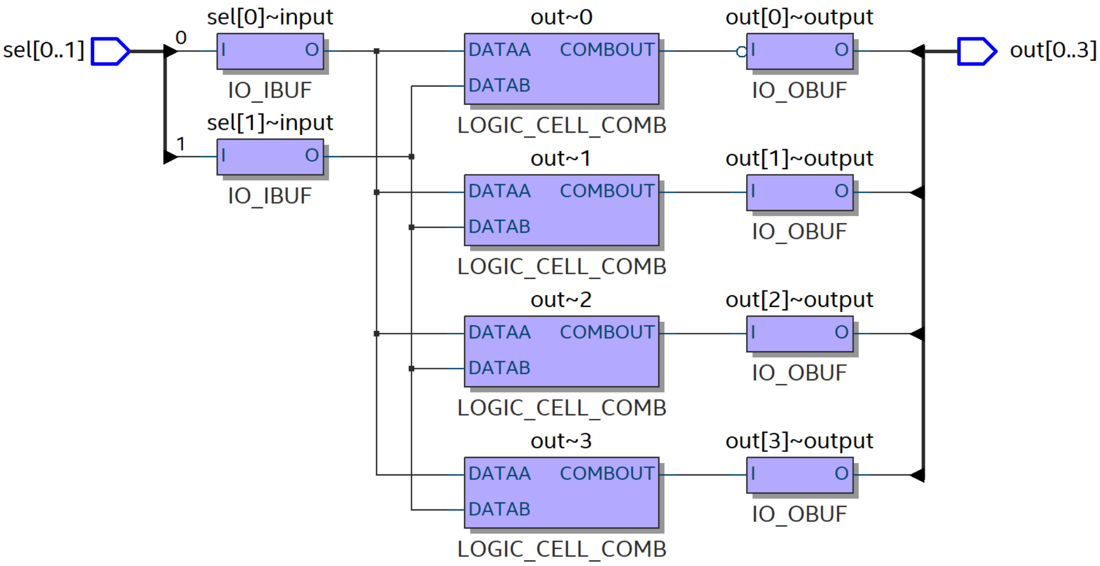
	Resource	Usage
1	Estimated ALUTs Used	4
1	-- Combinational ALUTs	4
2	-- Memory ALUTs	0
3	-- LUT_REGs	0
2	Dedicated logic registers	0
3		
4	Estimated ALUTs Unavailable	0
1	-- Due to unpartnered combinational logic	0
2	-- Due to Memory ALUTs	0
5		
6	Total combinational functions	4
7	Combinational ALUT usage by number of inputs	
1	-- 7 input functions	0
2	-- 6 input functions	0
3	-- 5 input functions	0
4	-- 4 input functions	0
5	-- <=3 input functions	4
8		
9	Combinational ALUTs by mode	
1	-- normal mode	4
2	-- extended LUT mode	0
3	-- arithmetic mode	0
4	-- shared arithmetic mode	0
10		
11	Estimated ALUT/register pairs used	4
12		
13	Total registers	0
1	-- Dedicated logic registers	0
2	-- I/O registers	0
3	-- LUT_REGs	0
14		
15		
16	I/O pins	6
17		
18	DSP block 18-bit elements	0
19		

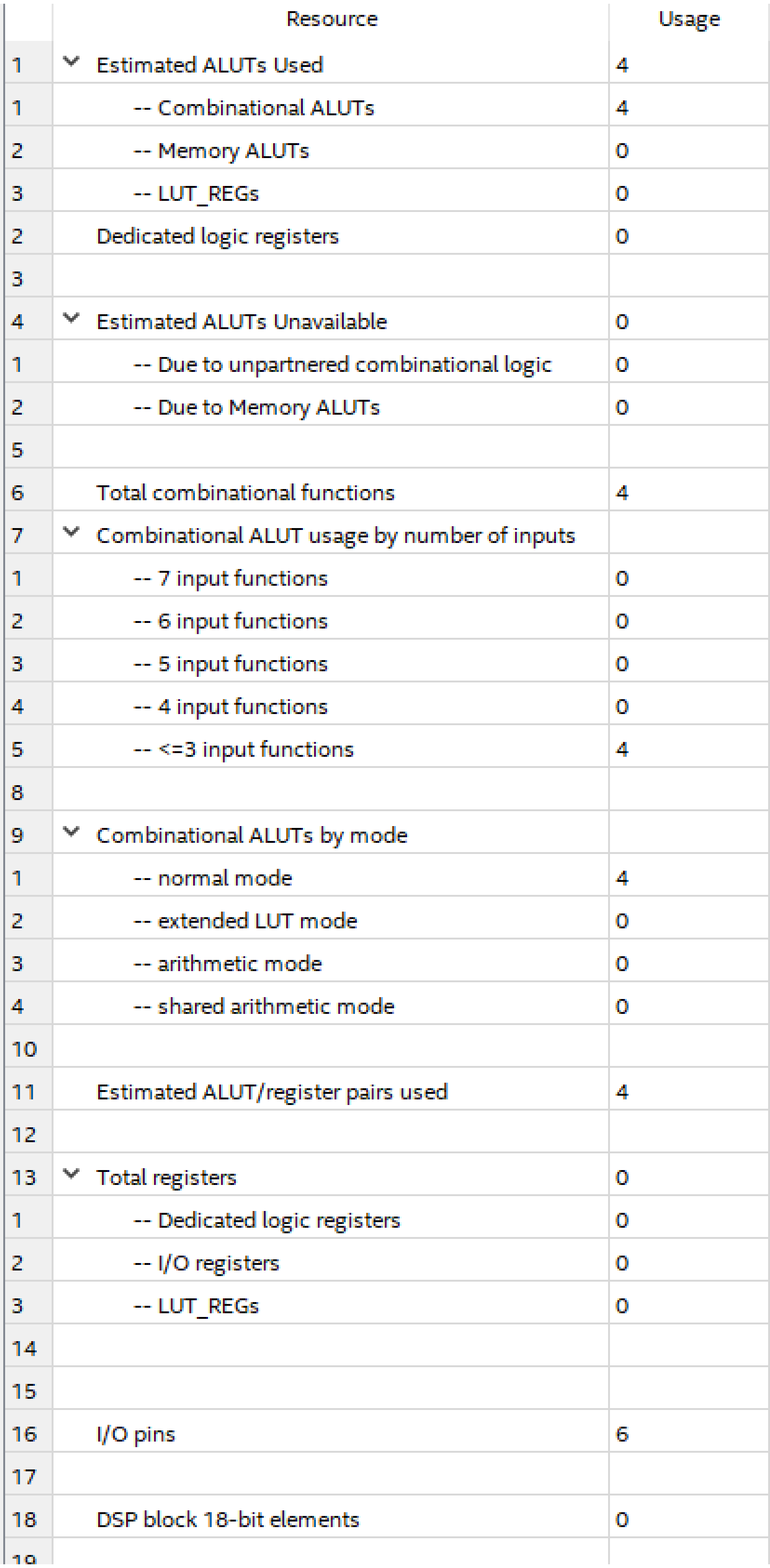
Dataflow Level



```
// 2to4 Decoder dataflow level code
module decoder(
  input  logic[1:0] sel,
  output logic[3:0] out
);
  assign out[0] = (!sel[0]) && (!sel[1]);
  assign out[1] = (!sel[0]) && (sel[1]);
  assign out[2] = (sel[0]) && (!sel[1]);
  assign out[3] = (sel[0]) && (sel[1]);

endmodule
```

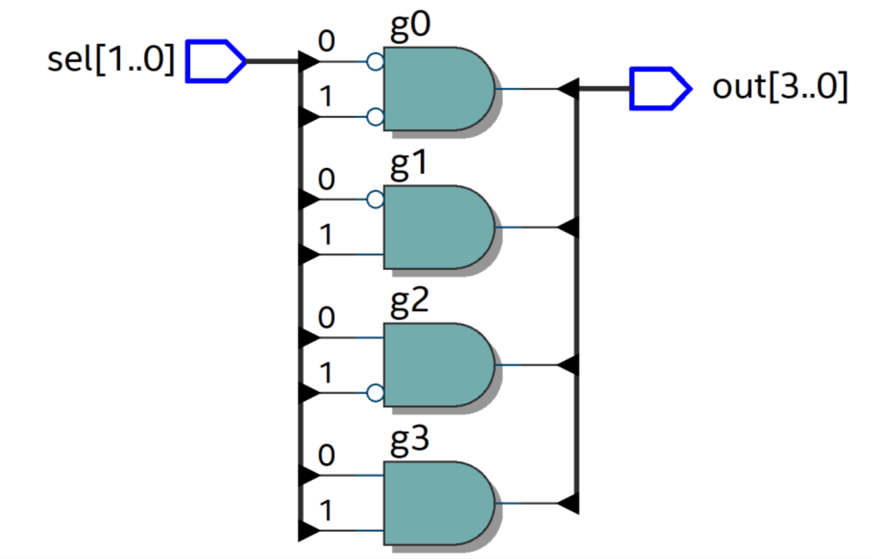


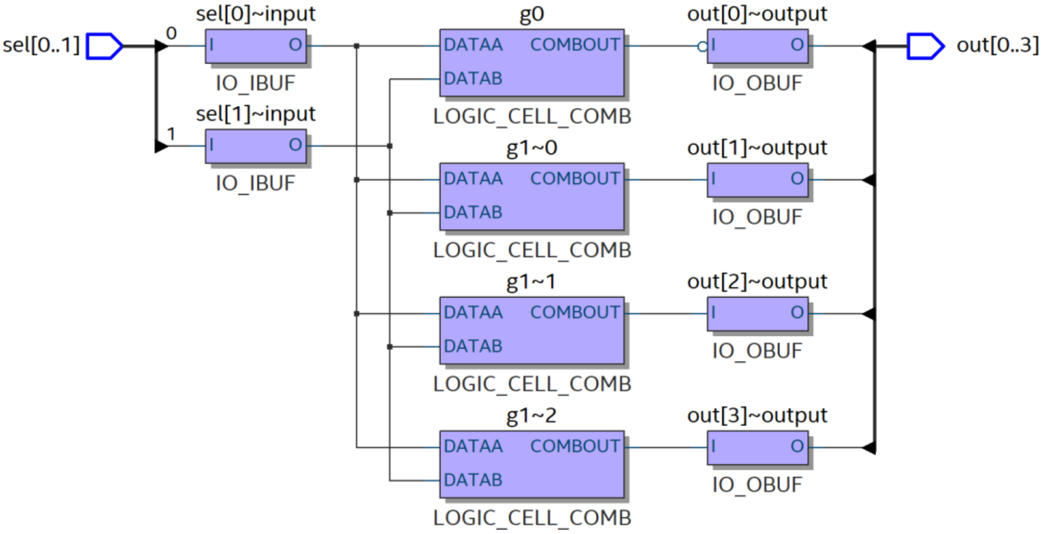


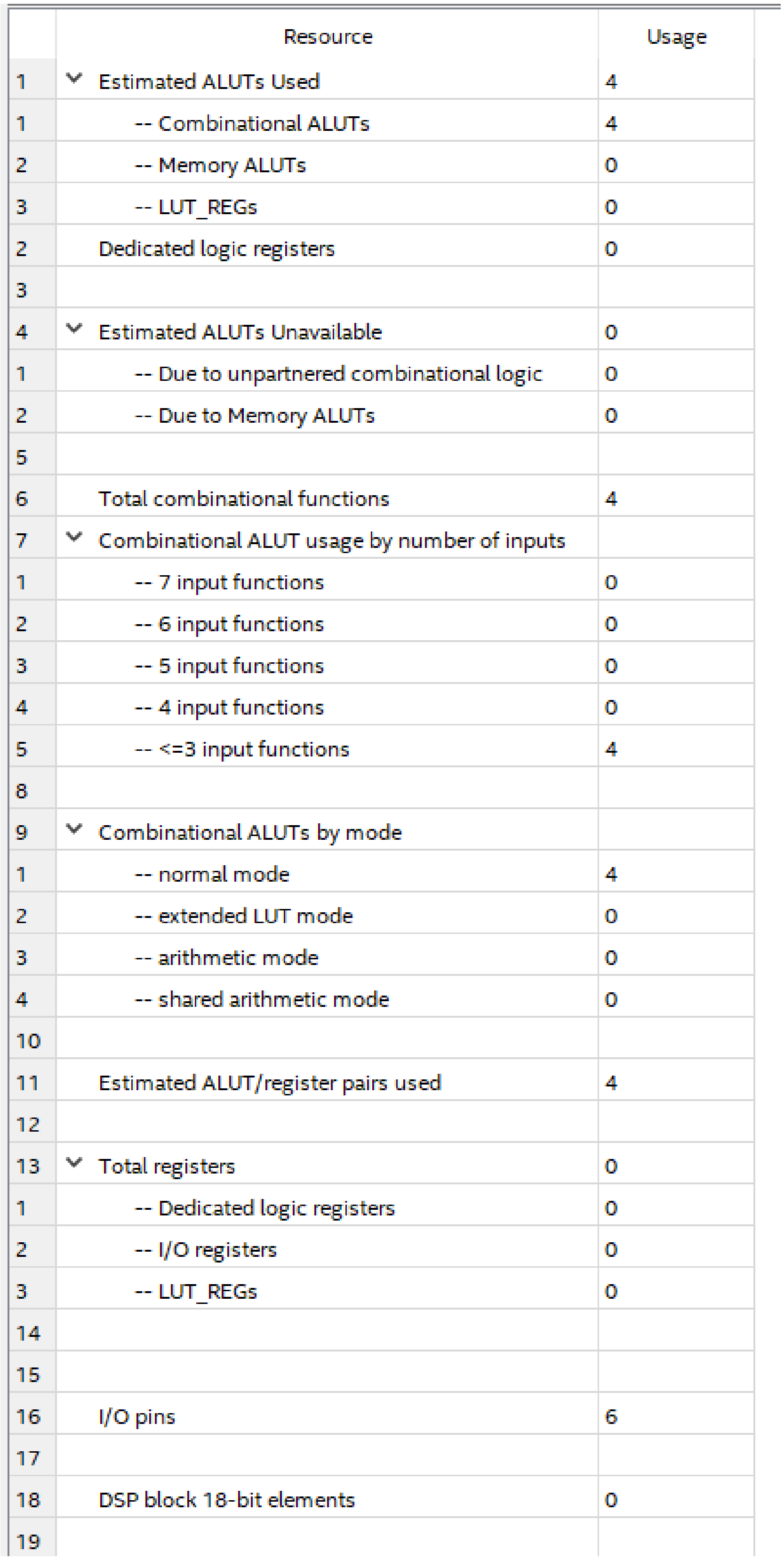


	Resource	Usage
1	Estimated ALUTs Used	4
1	-- Combinational ALUTs	4
2	-- Memory ALUTs	0
3	-- LUT_REGs	0
2	Dedicated logic registers	0
3		
4	Estimated ALUTs Unavailable	0
1	-- Due to unpartnered combinational logic	0
2	-- Due to Memory ALUTs	0
5		
6	Total combinational functions	4
7	Combinational ALUT usage by number of inputs	
1	-- 7 input functions	0
2	-- 6 input functions	0
3	-- 5 input functions	0
4	-- 4 input functions	0
5	-- <=3 input functions	4
8		
9	Combinational ALUTs by mode	
1	-- normal mode	4
2	-- extended LUT mode	0
3	-- arithmetic mode	0
4	-- shared arithmetic mode	0
10		
11	Estimated ALUT/register pairs used	4
12		
13	Total registers	0
1	-- Dedicated logic registers	0
2	-- I/O registers	0
3	-- LUT_REGs	0
14		
15		
16	I/O pins	6
17		
18	DSP block 18-bit elements	0
19		

Gate Level


sel[1..0]
0
1
g0
0
1
g1
0
1
g2
0
1
g3
out[3..0]


sel[0..1]
0
sel[0]~input
I
O
IO_IBUF
1
sel[1]~input
I
O
IO_IBUF
g0
DATAA
COMBOUT
DATAB
LOGIC_CELL_COMB
g1~0
DATAA
COMBOUT
DATAB
LOGIC_CELL_COMB
g1~1
DATAA
COMBOUT
DATAB
LOGIC_CELL_COMB
g1~2
DATAA
COMBOUT
DATAB
LOGIC_CELL_COMB
out[0]~output
I
O
IO_OBUF
out[1]~output
I
O
IO_OBUF
out[2]~output
I
O
IO_OBUF
out[3]~output
I
O
IO_OBUF
out[0..3]



	Resource	Usage
1	⌄ Estimated ALUTs Used	4
1	-- Combinational ALUTs	4
2	-- Memory ALUTs	0
3	-- LUT_REGs	0
2	Dedicated logic registers	0
3		
4	⌄ Estimated ALUTs Unavailable	0
1	-- Due to unpartnered combinational logic	0
2	-- Due to Memory ALUTs	0
5		
6	Total combinational functions	4
7	⌄ Combinational ALUT usage by number of inputs	
1	-- 7 input functions	0
2	-- 6 input functions	0
3	-- 5 input functions	0
4	-- 4 input functions	0
5	-- <=3 input functions	4
8		
9	⌄ Combinational ALUTs by mode	
1	-- normal mode	4
2	-- extended LUT mode	0
3	-- arithmetic mode	0
4	-- shared arithmetic mode	0
10		
11	Estimated ALUT/register pairs used	4
12		
13	⌄ Total registers	0
1	-- Dedicated logic registers	0
2	-- I/O registers	0
3	-- LUT_REGs	0
14		
15		
16	I/O pins	6
17		
18	DSP block 18-bit elements	0
19		

Function of 2-to-4 decoder: Converts a 2-bit binary number into a 4-bit one-hot encoded representation, where the logical 1’s index is representative of the input decimal number.

Number of ALUTs: 4 (6 I/O pins)

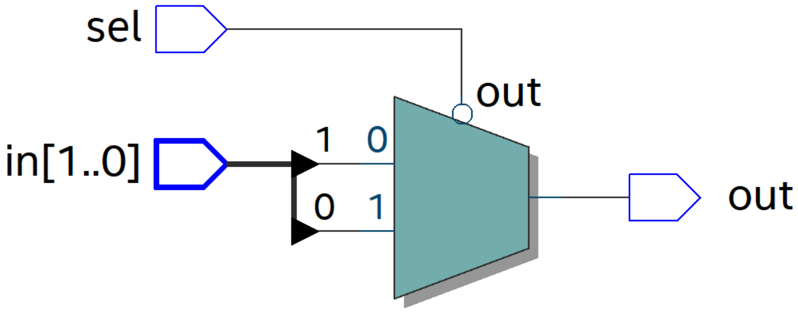
A 2-to-4 decoder can be implemented using 4 ALUTs because the 2-bit input has 4 unique states that is one hot encoded into a 4-bit output. Each bit of the output is tied to the output of one ALUT, thus four are needed in total.

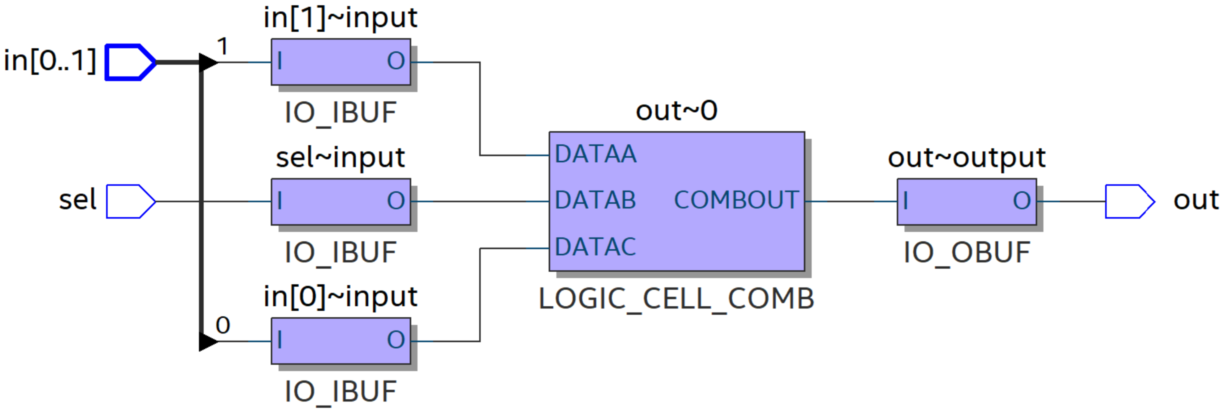
Number of Functions: 4 (2 input, 1 output)

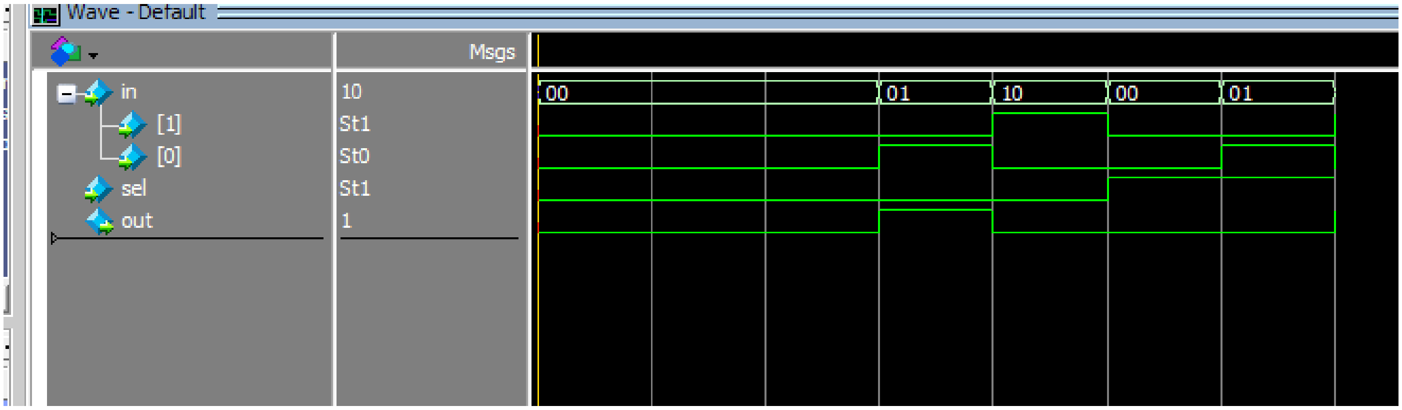
Each ALUT takes in the 2-bit input that can take on four unique states that represent 0-3 in decimal. The ALUT’s memory is programmed in a way that will only output a logical 1 if the 2-bit input’s state matches its predesignated output bit index. Since the same 2-bit input is fed into four ALUT’s, and each ALUT outputs a bit, there are six I/O’s.

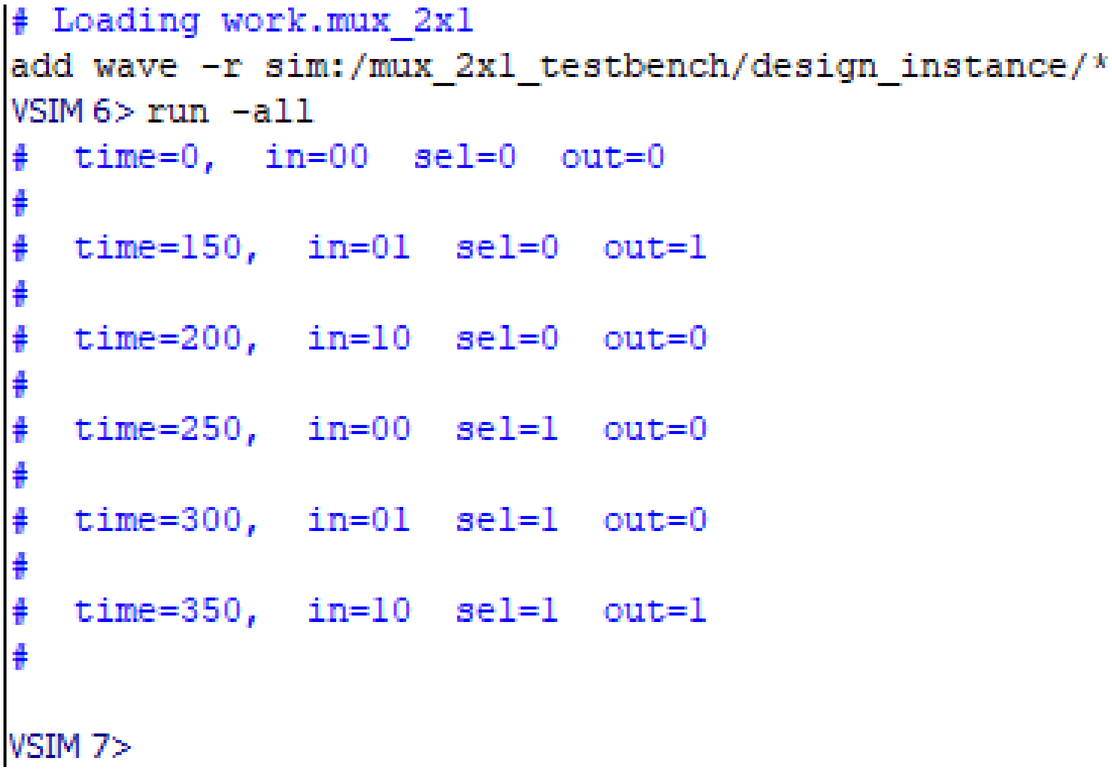
MUX

Behavioral Level

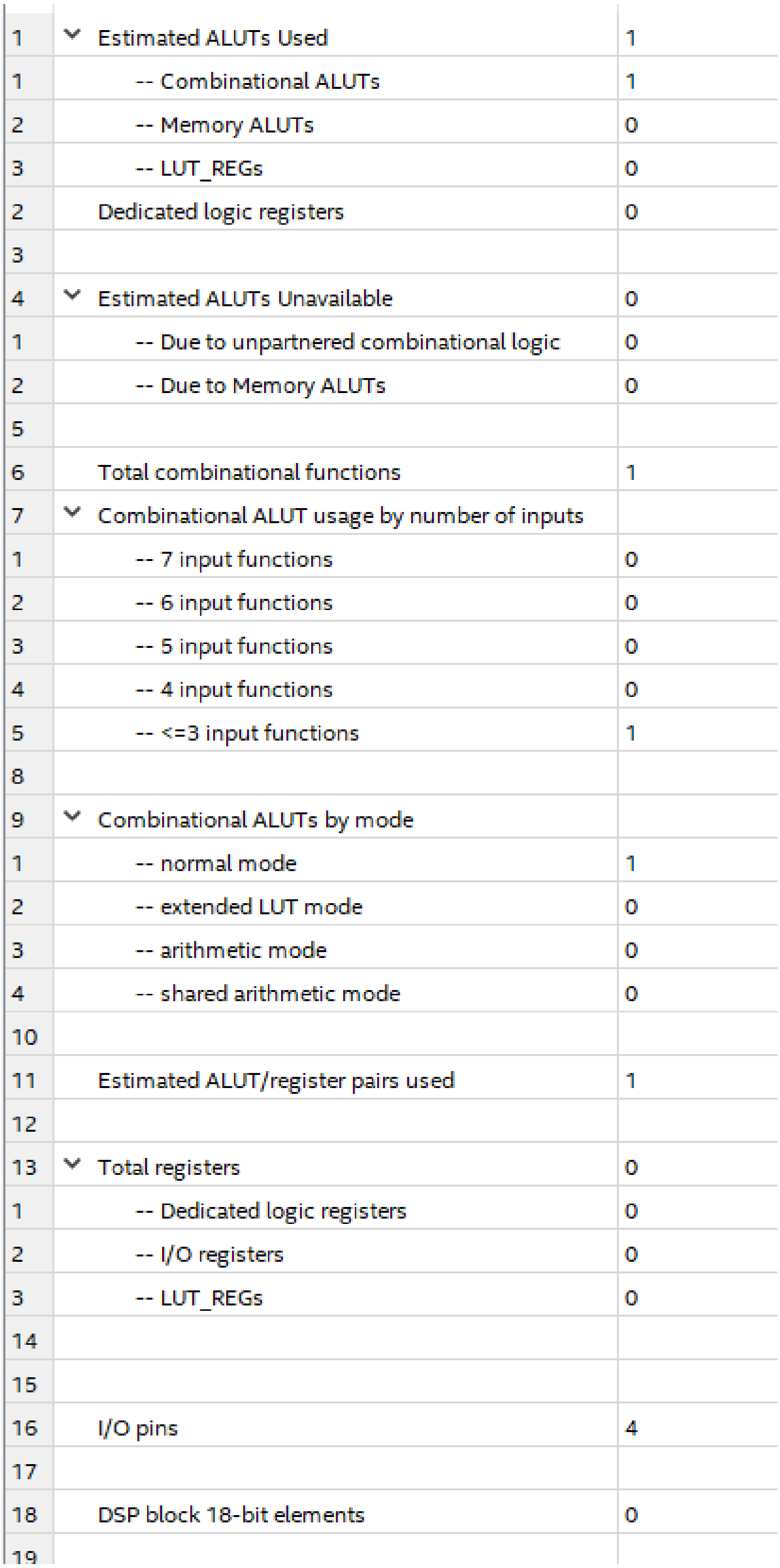






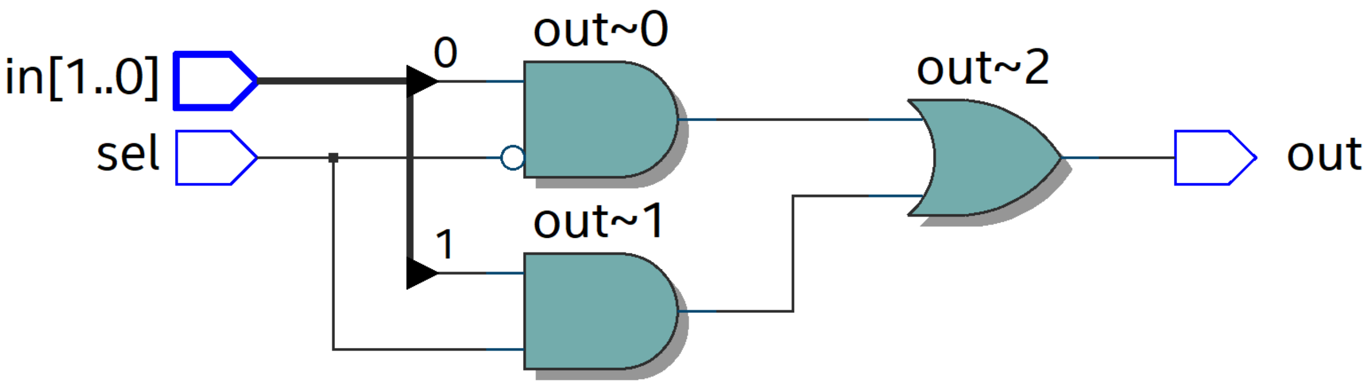


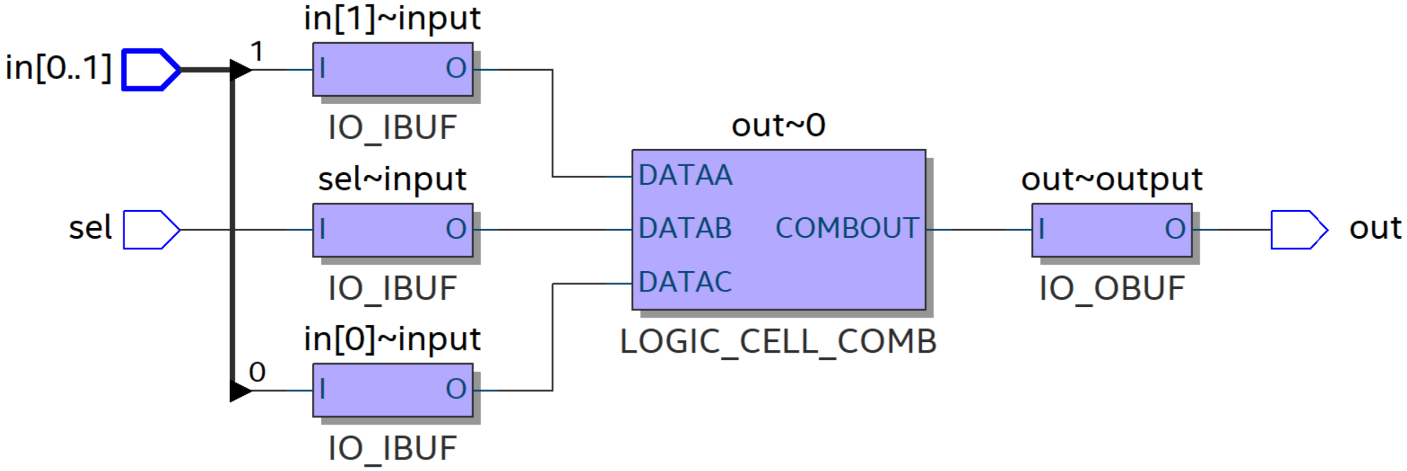
```
# Loading work.mux_2x1
add wave -r sim:/mux_2x1_testbench/design_instance/*
VSIM 6> run -all
#  time=0,  in=00  sel=0  out=0
#
#  time=150,  in=01  sel=0  out=1
#
#  time=200,  in=10  sel=0  out=0
#
#  time=250,  in=00  sel=1  out=0
#
#  time=300,  in=01  sel=1  out=0
#
#  time=350,  in=10  sel=1  out=1
#

VSIM 7>
```

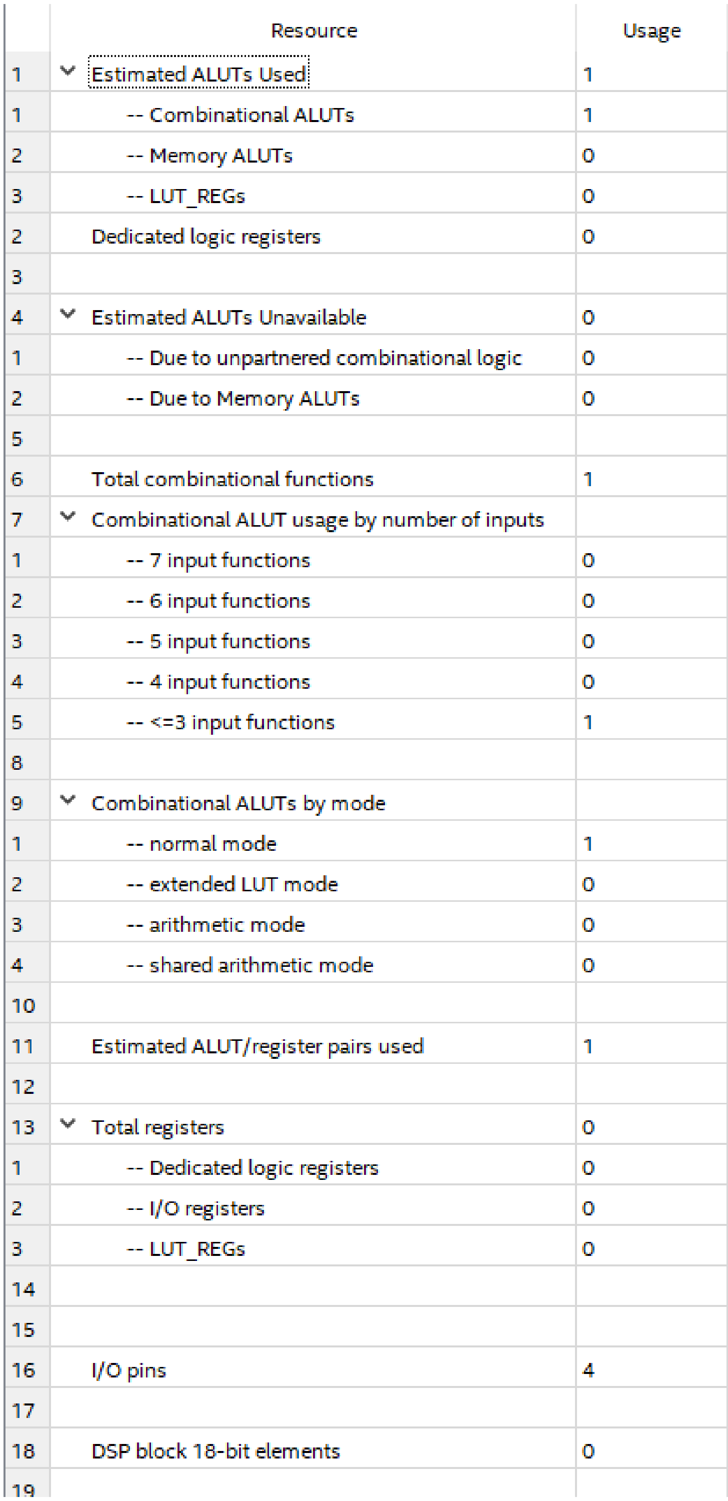


1	⌄	Estimated ALUTs Used	1
1		-- Combinational ALUTs	1
2		-- Memory ALUTs	0
3		-- LUT_REGs	0
2		Dedicated logic registers	0
3			
4	⌄	Estimated ALUTs Unavailable	0
1		-- Due to unpartnered combinational logic	0
2		-- Due to Memory ALUTs	0
5			
6		Total combinational functions	1
7	⌄	Combinational ALUT usage by number of inputs	
1		-- 7 input functions	0
2		-- 6 input functions	0
3		-- 5 input functions	0
4		-- 4 input functions	0
5		-- <=3 input functions	1
8			
9	⌄	Combinational ALUTs by mode	
1		-- normal mode	1
2		-- extended LUT mode	0
3		-- arithmetic mode	0
4		-- shared arithmetic mode	0
10			
11		Estimated ALUT/register pairs used	1
12			
13	⌄	Total registers	0
1		-- Dedicated logic registers	0
2		-- I/O registers	0
3		-- LUT_REGs	0
14			
15			
16		I/O pins	4
17			
18		DSP block 18-bit elements	0
19			

Dataflow Level

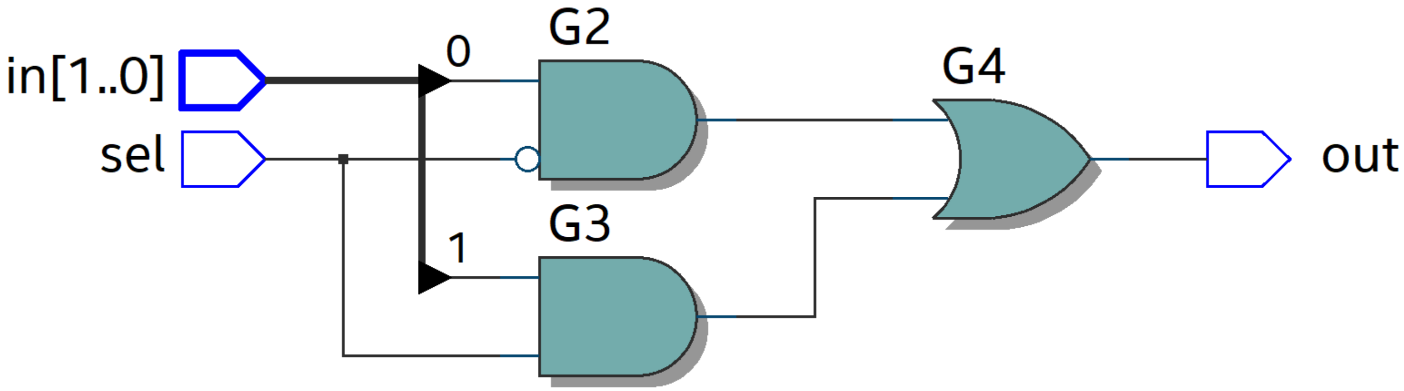


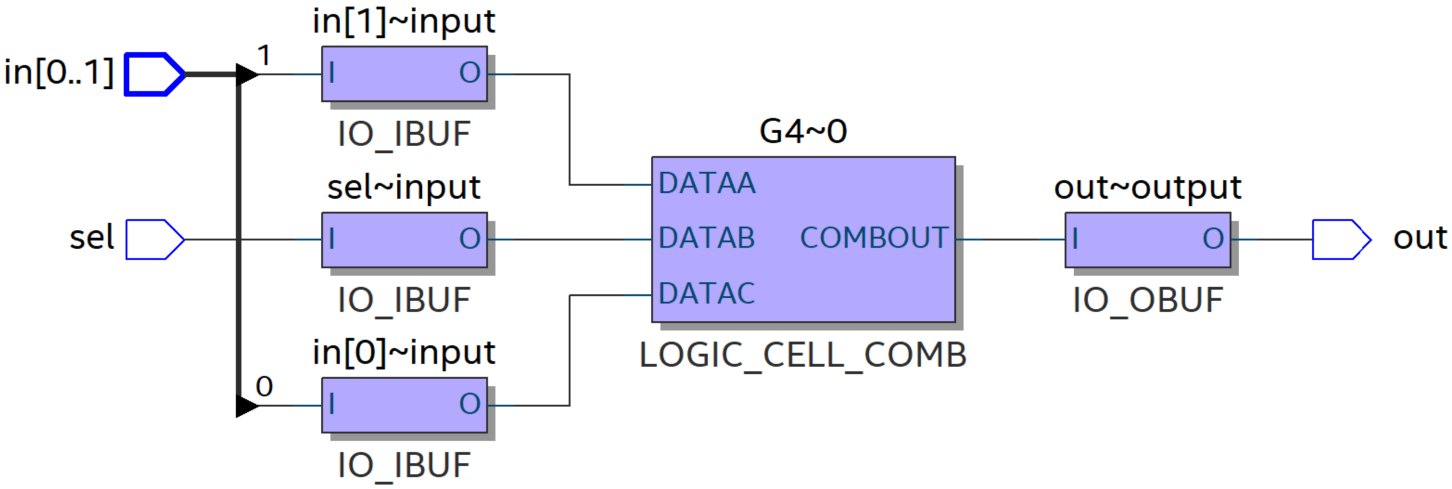


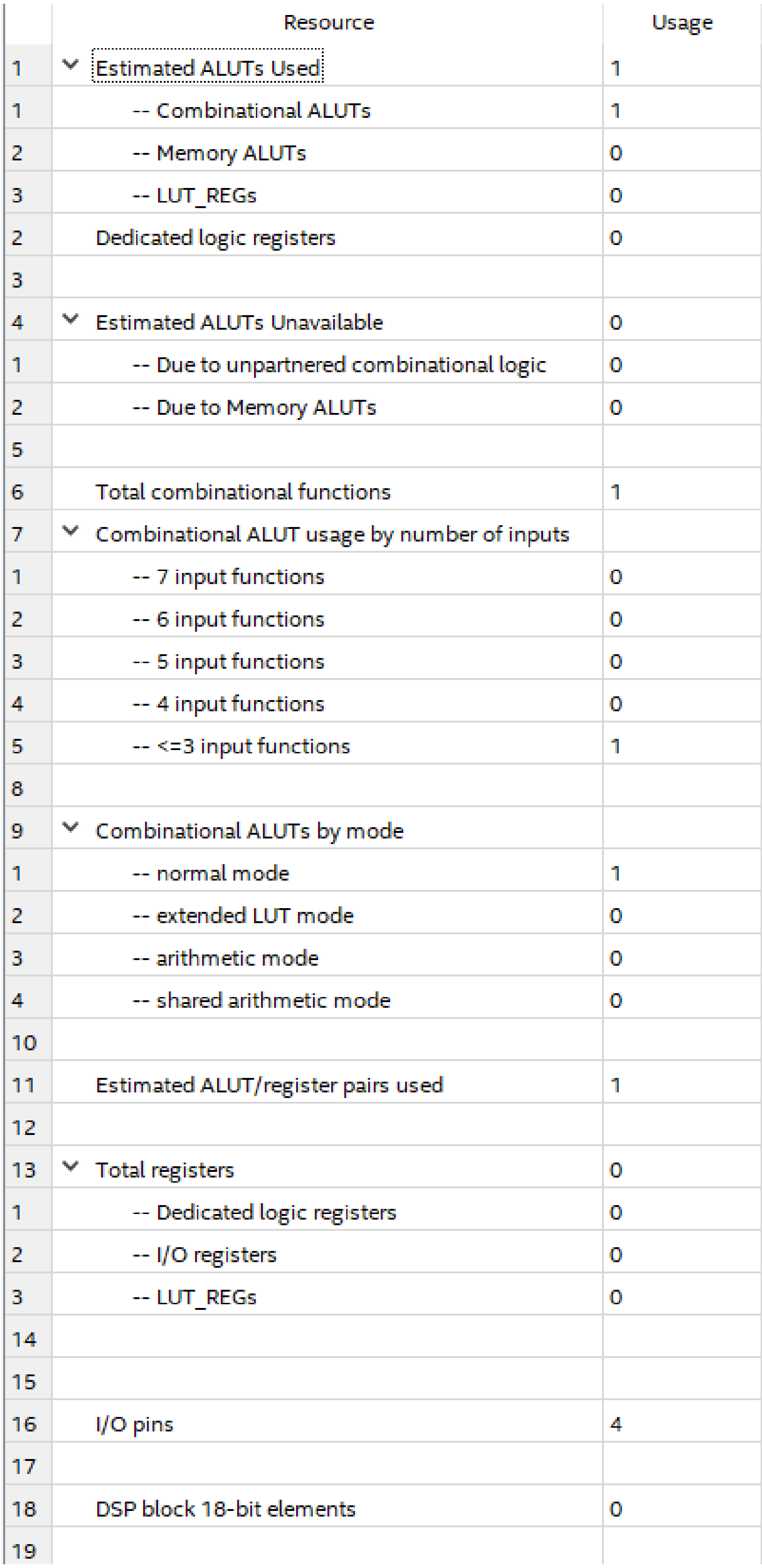


	Resource	Usage
1	⌄ Estimated ALUTs Used	1
1	-- Combinational ALUTs	1
2	-- Memory ALUTs	0
3	-- LUT_REGs	0
2	Dedicated logic registers	0
3		
4	⌄ Estimated ALUTs Unavailable	0
1	-- Due to unpartnered combinational logic	0
2	-- Due to Memory ALUTs	0
5		
6	Total combinational functions	1
7	⌄ Combinational ALUT usage by number of inputs	
1	-- 7 input functions	0
2	-- 6 input functions	0
3	-- 5 input functions	0
4	-- 4 input functions	0
5	-- <=3 input functions	1
8		
9	⌄ Combinational ALUTs by mode	
1	-- normal mode	1
2	-- extended LUT mode	0
3	-- arithmetic mode	0
4	-- shared arithmetic mode	0
10		
11	Estimated ALUT/register pairs used	1
12		
13	⌄ Total registers	0
1	-- Dedicated logic registers	0
2	-- I/O registers	0
3	-- LUT_REGs	0
14		
15		
16	I/O pins	4
17		
18	DSP block 18-bit elements	0
19		

Gate Level


in[1..0]
sel
0
1
G2
G3
G4
out


in[0..1]
sel
1
0
in[1]~input
I
O
IO_IBUF
sel~input
I
O
IO_IBUF
in[0]~input
I
O
IO_IBUF
G4~0
DATAA
DATAB
DATAC
COMBOUT
LOGIC_CELL_COMB
out~output
I
O
IO_OBUF
out



	Resource	Usage
1	⌄ Estimated ALUTs Used	1
1	-- Combinational ALUTs	1
2	-- Memory ALUTs	0
3	-- LUT_REGs	0
2	Dedicated logic registers	0
3		
4	⌄ Estimated ALUTs Unavailable	0
1	-- Due to unpartnered combinational logic	0
2	-- Due to Memory ALUTs	0
5		
6	Total combinational functions	1
7	⌄ Combinational ALUT usage by number of inputs	
1	-- 7 input functions	0
2	-- 6 input functions	0
3	-- 5 input functions	0
4	-- 4 input functions	0
5	-- <=3 input functions	1
8		
9	⌄ Combinational ALUTs by mode	
1	-- normal mode	1
2	-- extended LUT mode	0
3	-- arithmetic mode	0
4	-- shared arithmetic mode	0
10		
11	Estimated ALUT/register pairs used	1
12		
13	⌄ Total registers	0
1	-- Dedicated logic registers	0
2	-- I/O registers	0
3	-- LUT_REGs	0
14		
15		
16	I/O pins	4
17		
18	DSP block 18-bit elements	0
19		

Function of 1-bit MUX: A two-line selector based on a 1-bt binary input. The 1-bit input's state changes which input line is to be selected and ported to the output i.e. 0 is first line and 1 is second line.

Number of ALUTs: 1 (4 I/O pins)

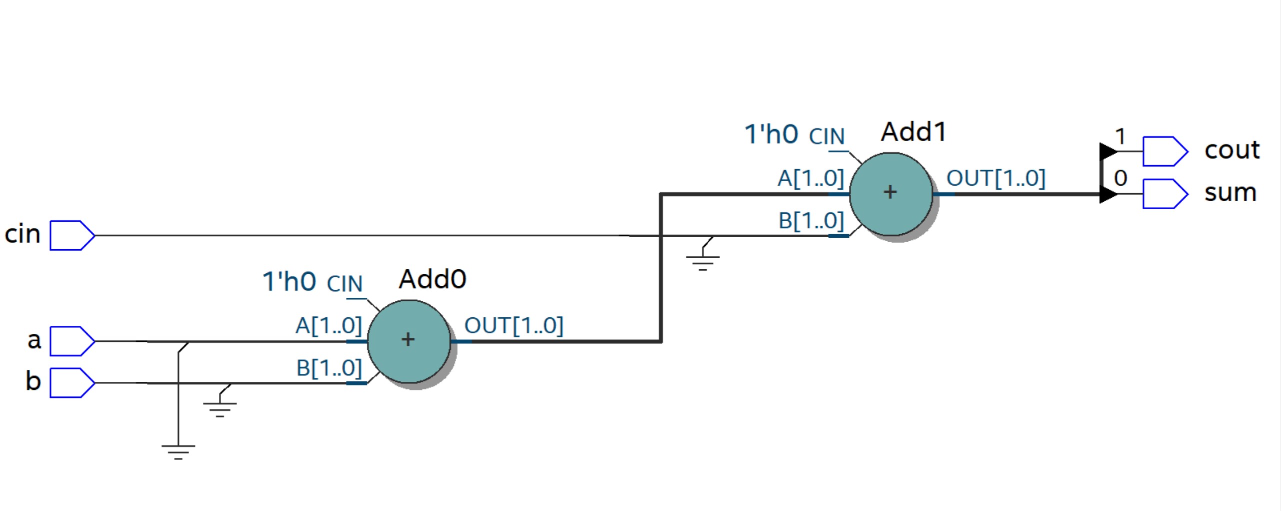
Since the MUX outputs only one bit, this can be accomplished with one ALUT with three inputs.

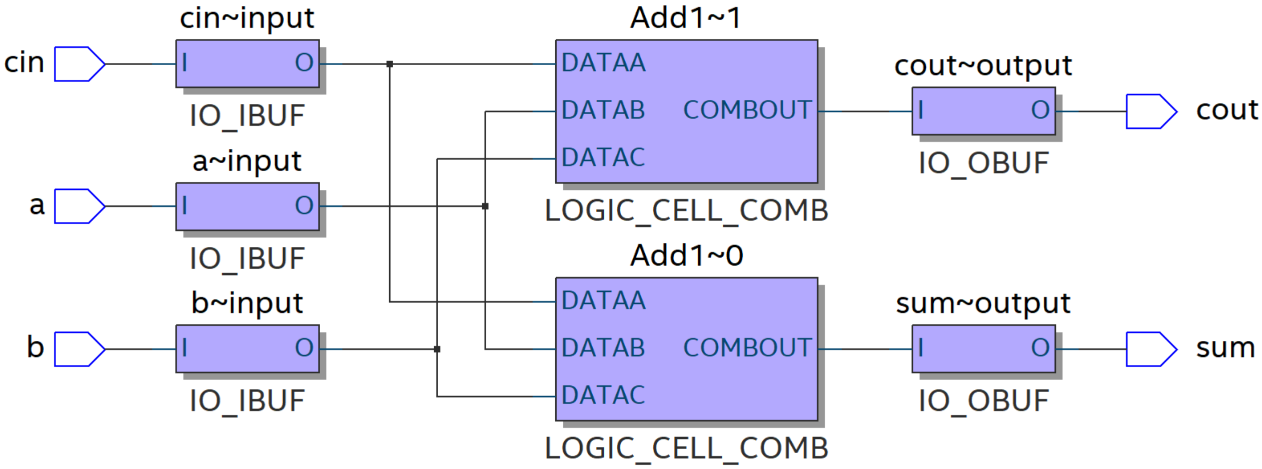
Number of Functions: 1 (3 input, 1 output)

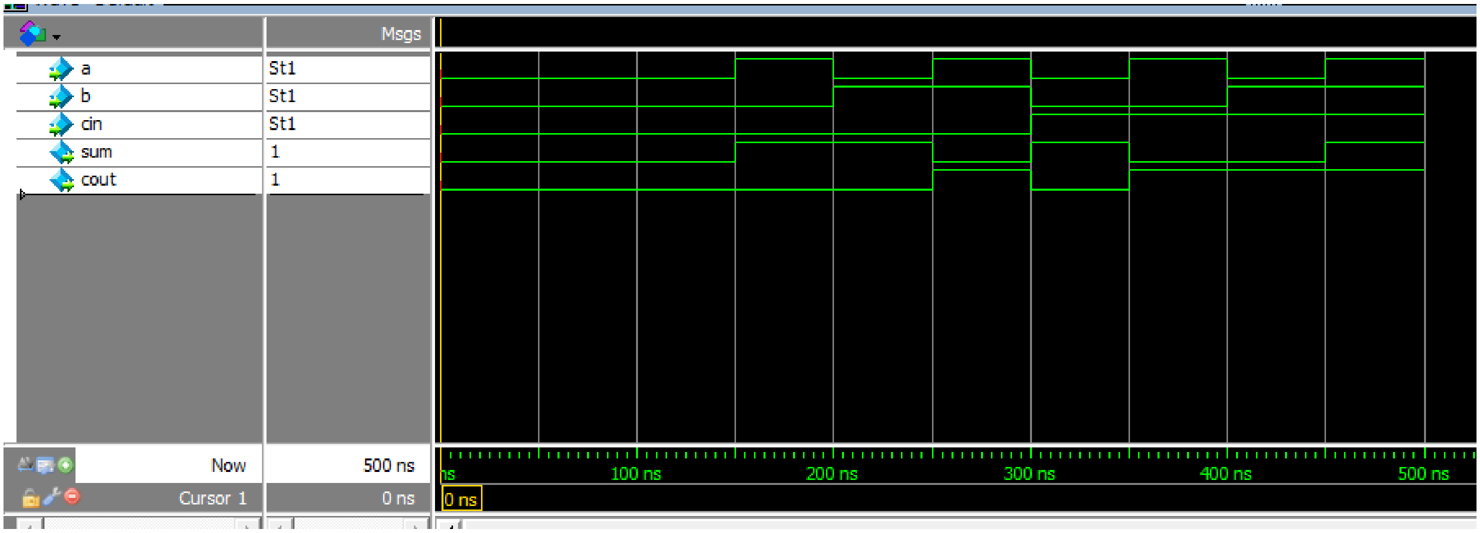
2-bit input and 1-bit selector input equates to a 3-bit input Boolean expression. This can be one function that has one output. Overall, only one function is needed.

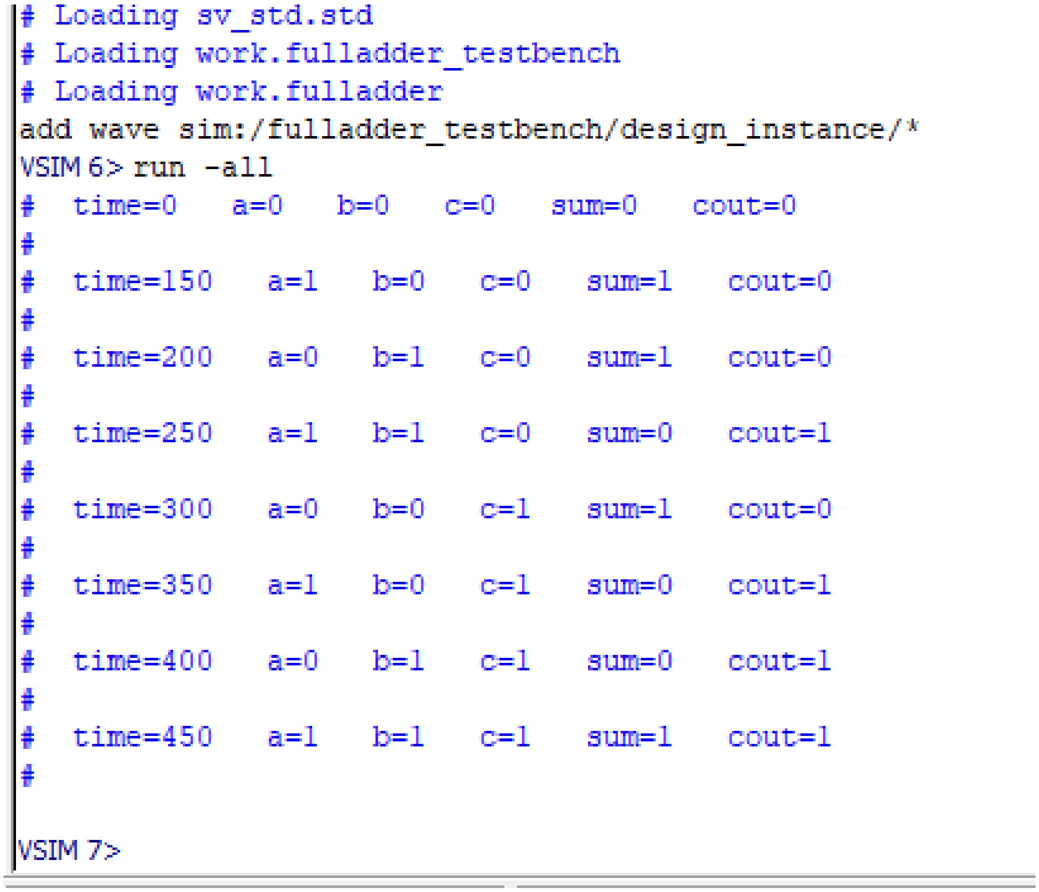
Full Adder

Behavioral Level

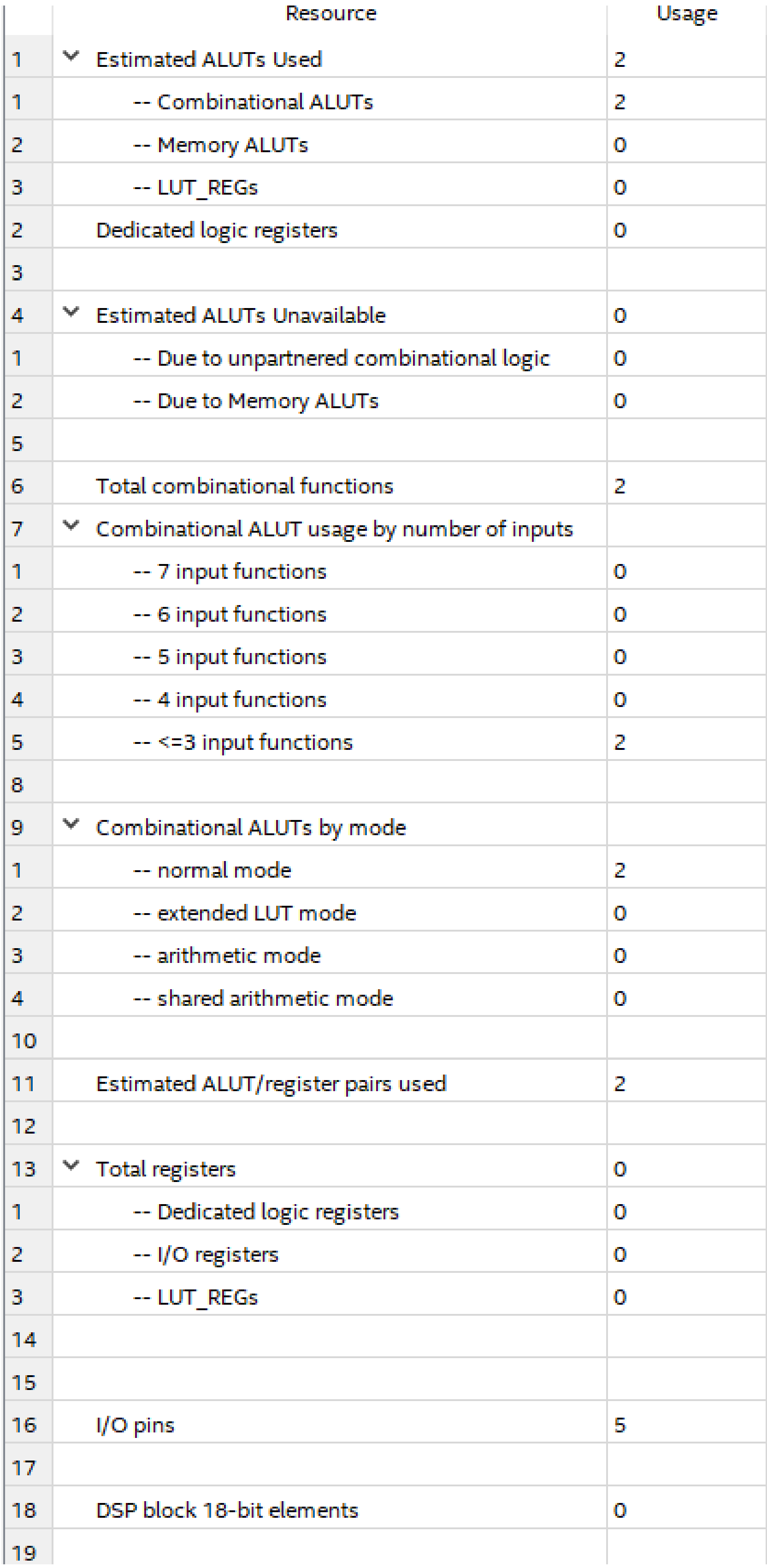






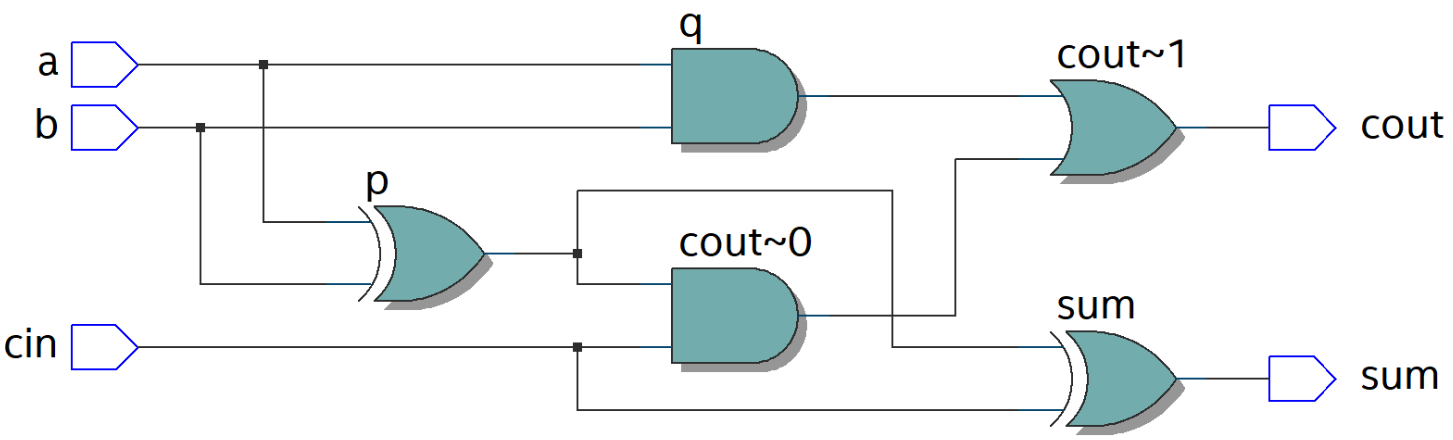


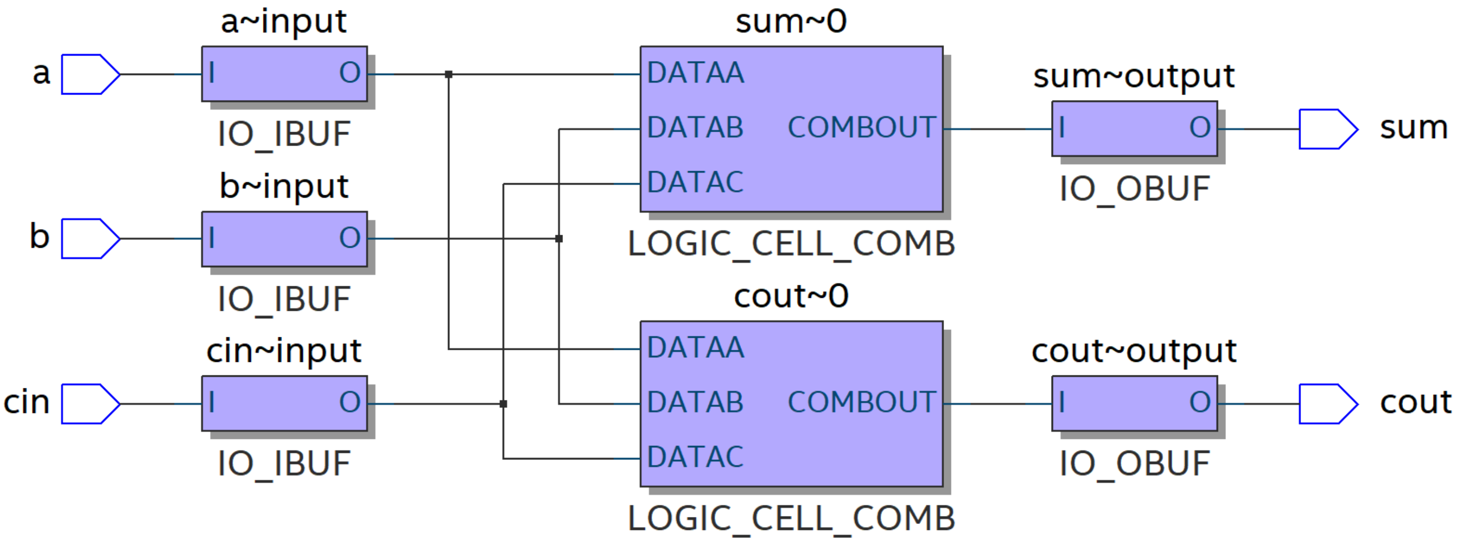
```
# Loading sv_std.std
# Loading work.fulladder_testbench
# Loading work.fulladder
add wave sim:/fulladder_testbench/design_instance/*
VSIM 6> run -all
#  time=0    a=0   b=0   c=0   sum=0   cout=0
#
#  time=150   a=1   b=0   c=0   sum=1   cout=0
#
#  time=200   a=0   b=1   c=0   sum=1   cout=0
#
#  time=250   a=1   b=1   c=0   sum=0   cout=1
#
#  time=300   a=0   b=0   c=1   sum=1   cout=0
#
#  time=350   a=1   b=0   c=1   sum=0   cout=1
#
#  time=400   a=0   b=1   c=1   sum=0   cout=1
#
#  time=450   a=1   b=1   c=1   sum=1   cout=1
#

VSIM 7>
```

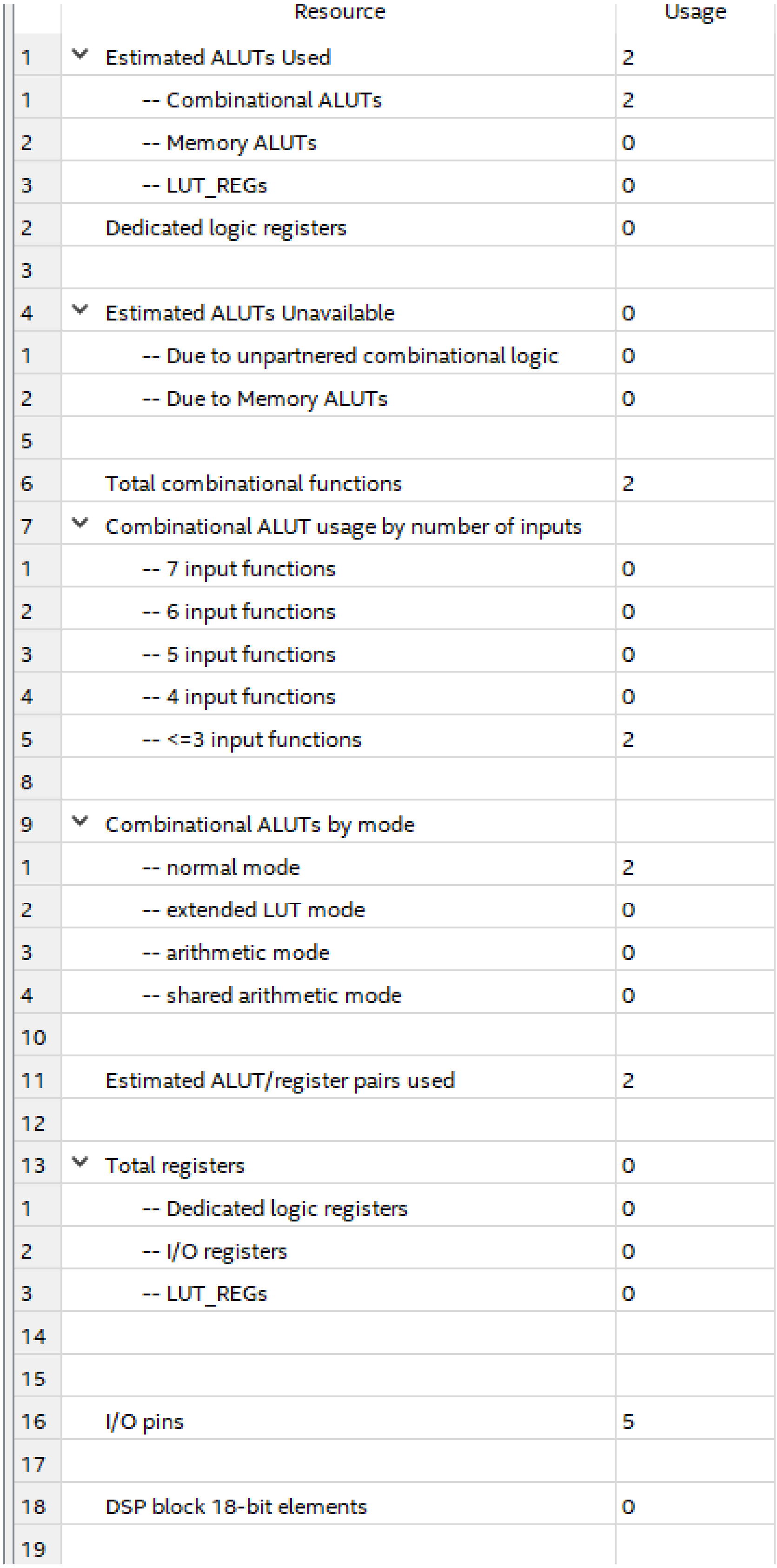


	Resource	Usage
1	⌄ Estimated ALUTs Used	2
1	-- Combinational ALUTs	2
2	-- Memory ALUTs	0
3	-- LUT_REGs	0
2	Dedicated logic registers	0
3		
4	⌄ Estimated ALUTs Unavailable	0
1	-- Due to unpartnered combinational logic	0
2	-- Due to Memory ALUTs	0
5		
6	Total combinational functions	2
7	⌄ Combinational ALUT usage by number of inputs	
1	-- 7 input functions	0
2	-- 6 input functions	0
3	-- 5 input functions	0
4	-- 4 input functions	0
5	-- <=3 input functions	2
8		
9	⌄ Combinational ALUTs by mode	
1	-- normal mode	2
2	-- extended LUT mode	0
3	-- arithmetic mode	0
4	-- shared arithmetic mode	0
10		
11	Estimated ALUT/register pairs used	2
12		
13	⌄ Total registers	0
1	-- Dedicated logic registers	0
2	-- I/O registers	0
3	-- LUT_REGs	0
14		
15		
16	I/O pins	5
17		
18	DSP block 18-bit elements	0
19		

Dataflow Level

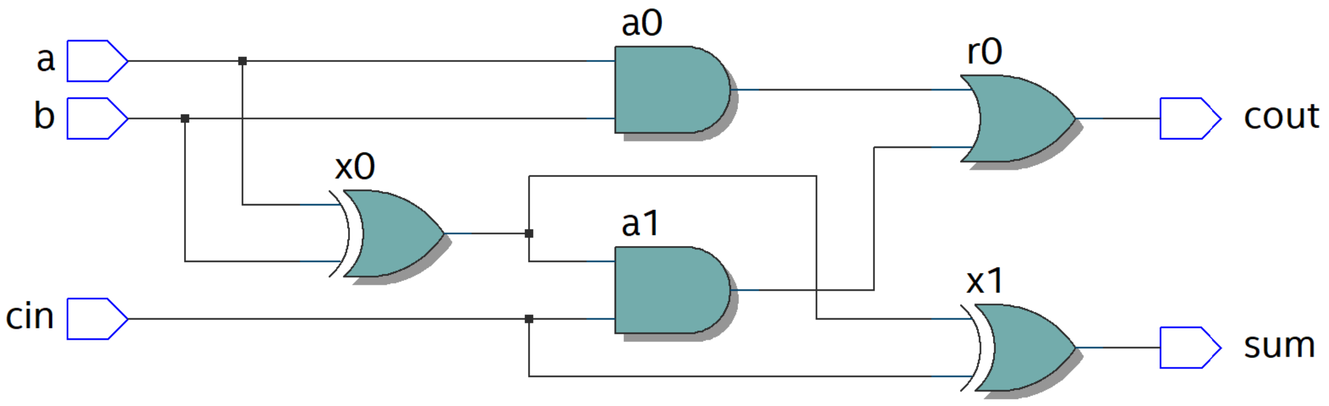


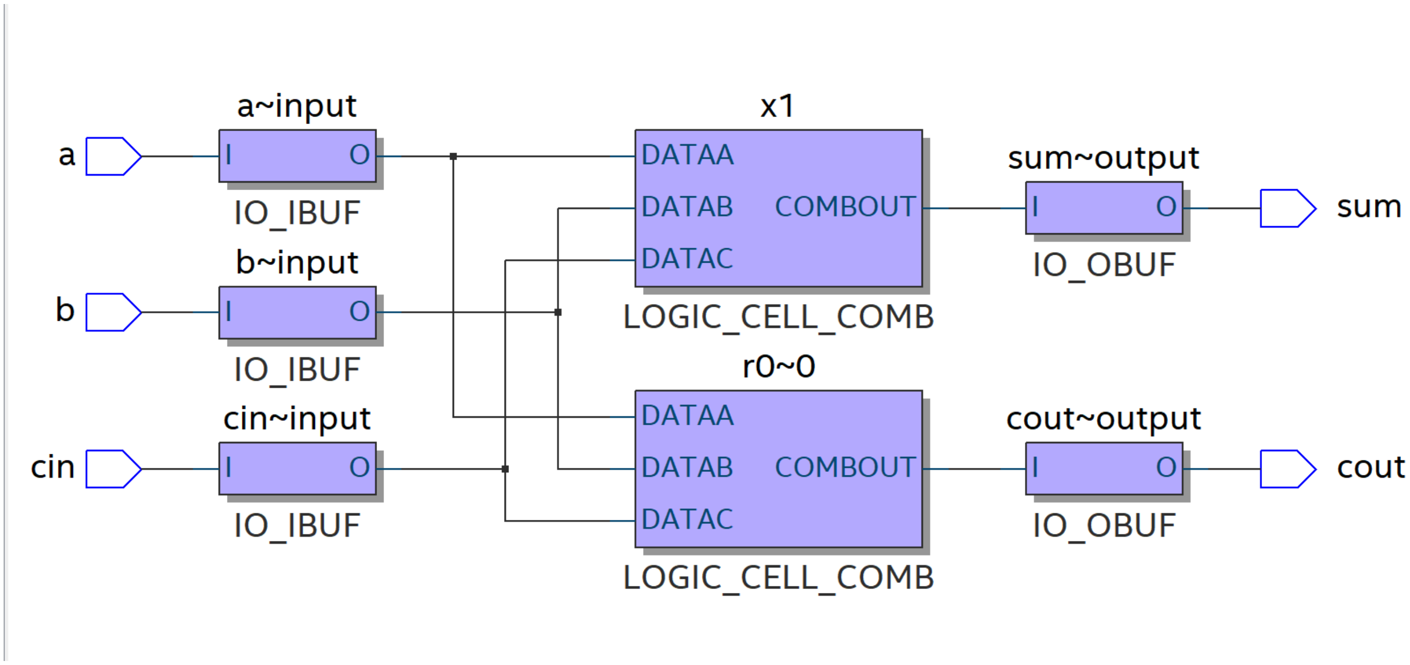


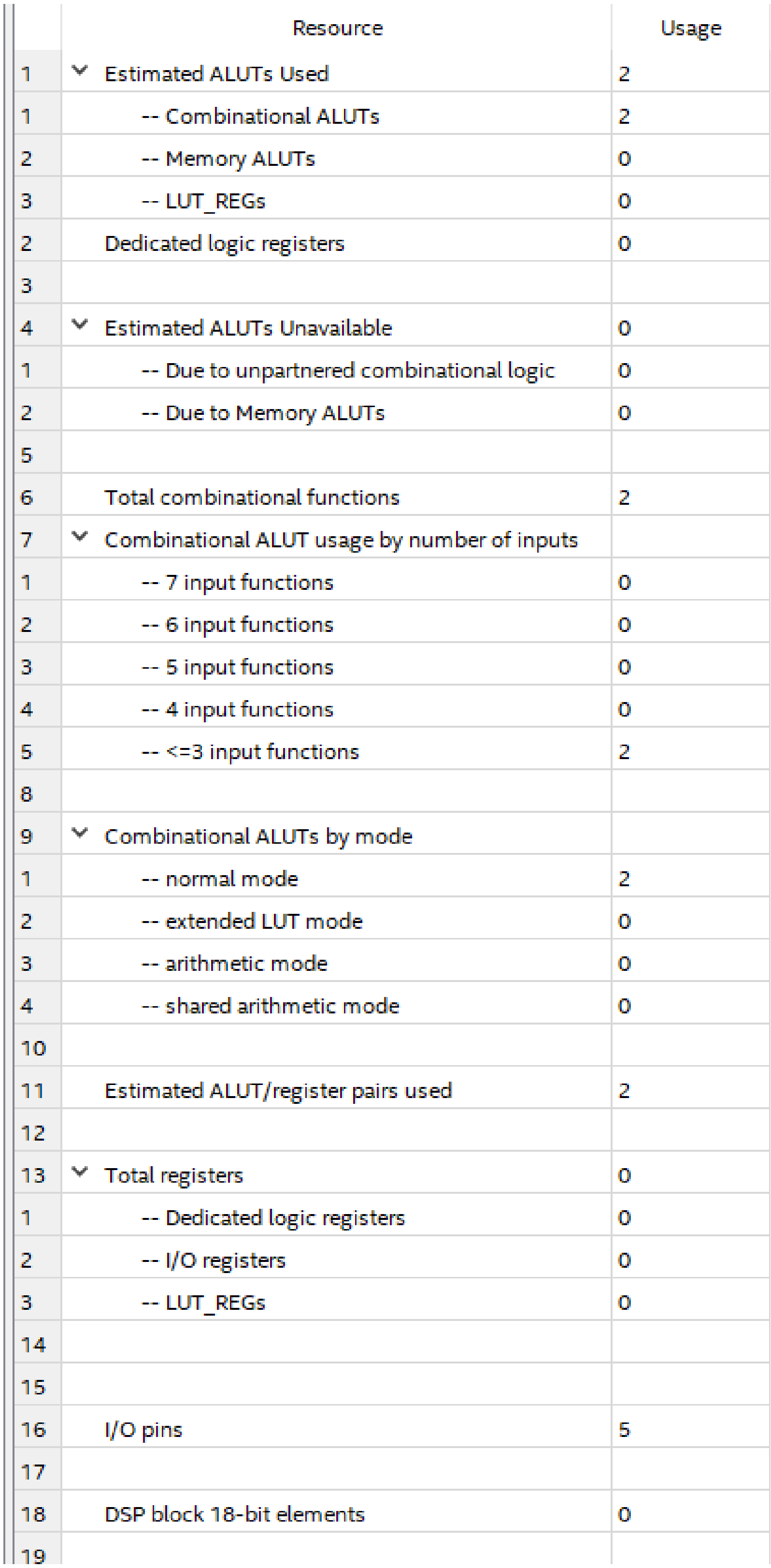


	Resource	Usage
1	Estimated ALUTs Used	2
1	-- Combinational ALUTs	2
2	-- Memory ALUTs	0
3	-- LUT_REGs	0
2	Dedicated logic registers	0
3		
4	Estimated ALUTs Unavailable	0
1	-- Due to unpartnered combinational logic	0
2	-- Due to Memory ALUTs	0
5		
6	Total combinational functions	2
7	Combinational ALUT usage by number of inputs	
1	-- 7 input functions	0
2	-- 6 input functions	0
3	-- 5 input functions	0
4	-- 4 input functions	0
5	-- <=3 input functions	2
8		
9	Combinational ALUTs by mode	
1	-- normal mode	2
2	-- extended LUT mode	0
3	-- arithmetic mode	0
4	-- shared arithmetic mode	0
10		
11	Estimated ALUT/register pairs used	2
12		
13	Total registers	0
1	-- Dedicated logic registers	0
2	-- I/O registers	0
3	-- LUT_REGs	0
14		
15		
16	I/O pins	5
17		
18	DSP block 18-bit elements	0
19		

Gate Level


a0
r0
a
b
cout
x0
a1
x1
cin
sum


a~input
x1
a
I
O
IO_IBUF
DATAA
DATAB
COMBOUT
DATAC
sum~output
I
O
IO_OBUF
sum
b~input
b
I
O
IO_IBUF
LOGIC_CELL_COMB
r0~0
cin~input
DATAA
cout~output
cin
I
O
DATAB
COMBOUT
I
O
cout
DATAC
IO_IBUF
IO_OBUF
LOGIC_CELL_COMB



	Resource	Usage
1	Estimated ALUTs Used	2
1	-- Combinational ALUTs	2
2	-- Memory ALUTs	0
3	-- LUT_REGs	0
2	Dedicated logic registers	0
3		
4	Estimated ALUTs Unavailable	0
1	-- Due to unpartnered combinational logic	0
2	-- Due to Memory ALUTs	0
5		
6	Total combinational functions	2
7	Combinational ALUT usage by number of inputs	
1	-- 7 input functions	0
2	-- 6 input functions	0
3	-- 5 input functions	0
4	-- 4 input functions	0
5	-- <=3 input functions	2
8		
9	Combinational ALUTs by mode	
1	-- normal mode	2
2	-- extended LUT mode	0
3	-- arithmetic mode	0
4	-- shared arithmetic mode	0
10		
11	Estimated ALUT/register pairs used	2
12		
13	Total registers	0
1	-- Dedicated logic registers	0
2	-- I/O registers	0
3	-- LUT_REGs	0
14		
15		
16	I/O pins	5
17		
18	DSP block 18-bit elements	0
19		

Function of full adder: Adds two 1-bit operands and also takes in a 1-bit carry in. The result is two bits, one being the sum, and the other being the carry out. The sum and carry out represent the 2-bit result when the decimal result is larger than 1 that causes a bit overflow in sum.

Number of ALUTs: 2 (5 I/O pins)

Two distinct outputs are required: first between inputs a and b, second between a + b and carry in. This means a total of two ALUTs are needed.

Number of Functions: 2 (2 input, 1 output)

Two functions are needed – these are essentially half adders. Each half adder takes in two 1-bit inputs. The first half-adder's output is ported to the first input of the second half-adder. This is added to carry in. Overall, there are three inputs and 2 outputs, sum and carry out. A total of 5 I/O's are present.