ECE 111 Winter 2022  
HW1  
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**2-to-4 Decoder**

Text

Description automatically generated**Behavioral Level**

Chart

Description automatically generated

Diagram

Description automatically generated

A picture containing chart

Description automatically generated

Graphical user interface, text, application

Description automatically generated

Graphical user interface

Description automatically generated with medium confidence

**Dataflow Level**

Text

Description automatically generated

Diagram, schematic

Description automatically generated

Diagram

Description automatically generated

Graphical user interface, application

Description automatically generated

**Gate Level**

Diagram, schematic

Description automatically generated

Diagram

Description automatically generated

A picture containing graphical user interface

Description automatically generated

**Function of 2-to-4 decoder:** Converts a 2-bit binary number into a 4-bit one-hot encoded representation, where the logical 1’s index is representative of the input decimal number.

**Number of ALUTs:** 4 (6 I/O pins)

A 2-to-4 decoder can be implemented using 4 ALUTs because the 2-bit input has 4 unique states that is one hot encoded into a 4-bit output. Each bit of the output is tied to the output of one ALUT, thus four are needed in total.

**Number of Functions:** 4 (2 input, 1 output)

Each ALUT takes in the 2-bit input that can take on four unique states that represent 0-3 in decimal. The ALUT’s memory is programmed in a way that will only output a logical 1 if the 2-bit input’s state matches its predesignated output bit index. Since the same 2-bit input is fed into four ALUT’s, and each ALUT outputs a bit, there are six I/O’s.

**MUX**

**Behavioral Level**

Diagram, schematic

Description automatically generated

Diagram

Description automatically generated

Graphical user interface

Description automatically generated

Text

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Graphical user interface

Description automatically generated with medium confidence

**Dataflow Level**

Diagram, schematic

Description automatically generated

Diagram

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**Gate Level**

Diagram, schematic

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Diagram

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Graphical user interface

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**Function of 1-bit MUX:** A two-line selector based on a 1-bt binary input. The 1-bit input’s state changes which input line is to be selected and ported to the output i.e. 0 is first line and 1 is second line.

**Number of ALUTs:** 1 (4 I/O pins)

Since the MUX outputs only one bit, this can be accomplished with one ALUT with three inputs.

**Number of Functions:** 1 (3 input, 1 output)

2-bit input and 1-bit selector input equates to a 3-bit input Boolean expression. This can be one function that has one output. Overall, only one function is needed.

**Full Adder**

**Behavioral Level**

Diagram

Description automatically generated

Diagram

Description automatically generated

Graphical user interface

Description automatically generated with medium confidence

Text

Description automatically generated

Graphical user interface

Description automatically generated with medium confidence

**Dataflow Level**

Diagram, schematic

Description automatically generated

Diagram

Description automatically generated

Graphical user interface

Description automatically generated with medium confidence

**Gate Level**

Diagram, schematic

Description automatically generated

Diagram

Description automatically generated

Graphical user interface

Description automatically generated with medium confidence

**Function of full adder:** Adds two 1-bit operands and also takes in a 1-bit carry in. The result is two bits, one being the sum, and the other being the carry out. The sum and carry out represent the 2-bit result when the decimal result is larger than 1 that causes a bit overflow in sum.

**Number of ALUTs:** 2 (5 I/O pins)

Two distinct outputs are required: first between inputs a and b, second between a + b and carry in. This means a total of two ALUTs are needed.

**Number of Functions:** 2 (2 input, 1 output)

Two functions are needed – these are essentially half adders. Each half adder takes in two 1-bit inputs. The first half-adder’s output is ported to the first input of the second half-adder. This is added to carry in. Overall, there are three inputs and 2 outputs, sum and carry out. A total of 5 I/O’s are present.