ECE 111 Winter 2022  
HW2  
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**ALU**

ALU module

Text

Description automatically generated

ALU top module

Text

Description automatically generated

Text

Description automatically generated

RTL netlist (ALU top)

Diagram, schematic

Description automatically generated

Post-mapping netlist (ALU top)

Diagram, schematic

Description automatically generated

Resource usage (ALU top)

Graphical user interface

Description automatically generated with low confidence

113 ALUTs were used.

Table

Description automatically generatedTestbench simulation waveform

The simulation waveform shows the ALU performing all 16 operations correctly on the given operands, as follows:

1. 2 + 1 = 3
2. 9 – 5 = 4
3. 12 \* 10 = 120
4. 7 % 4 = 3. This is because the remainder to 7 / 4 is 3.
5. 12 / 6 = 2
6. 9 & 8 = 1001 & 1000 = 1000 = 8 in decimal.
7. 5 | 10 = 0101 & 1010 = 1111 = 15 in decimal.
8. 1 ^ 3 = 0001 XOR 0011 = 0010 = 2 in decimal.
9. 9 && 8 = 1, because both operands are larger than 1, so this is a boolean True. Thus, True AND True make True, 1 in decimal.
10. 5 || 10 = 1, because 5 (True) OR 10 (True) is True, 1 in decimal.
11. 4 << 1 = 8, because 0100 shifted 1 to the left is 1000 which is 8 in decimal; this is equivalent to multiplying by 2.
12. 4 >> 1 = 2, because a logical shift to the right by 1 is equivalent to dividing by 2.
13. 5 == 5 = 1, because the equality is true.
14. 3 != 8 = 1, because the inequality is true.
15. 9 < 7 = 0, because 9 is not less than 7.
16. 13 < 10 = 1, because 13 is greater than 10.

**Up-down Counter**

Up counter module

Text

Description automatically generated

Down counter module

Text

Description automatically generated

Mux 2x1 module

Text

Description automatically generated

Up-down counter module

Text

Description automatically generated

Diagram, schematic

Description automatically generatedRTL netlist (Up-down counter)

Chart

Description automatically generatedPost-mapping netlist (Up-down counter)

Resource usage (Up-down counter)

Graphical user interface

Description automatically generated with medium confidence

10 ALUTs were used.

Graphical user interface

Description automatically generatedTestbench simulation waveform

The simulation shows that the up-down counter works. The first half of the simulation shows the counting up phase, indicated by the constant 0 input of the select line. The clear pulse sets the up counter back to 0, and on every positive edge of the clock, the output count\_value increments, until it reaches 15 and wraps back to 0 due to the 4-bit width limitation. The second half of the simulation is the count down phase, indicated by the select line going to 1. The clear pulse now resets the count down to 15, which is followed by a decrement on every positive clock – when the count\_value reaches 0, it wraps back to 15 because of the discussed bit width limitation.