ECE 111 Winter 2022  
HW4  
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**Barrel Shifter**

Code

Text

Description automatically generated with low confidence

Graphical user interface, text, application

Description automatically generated

RTL netlist

Diagram, schematic

Description automatically generated

Resource usage

Graphical user interface

Description automatically generated with medium confidence

Testbench simulation waveform

Graphical user interface

Description automatically generated

* The testbench in this case was for a 4-bit LFSR, but will work widths 2-8. We see that the seed is 1111, and upon the positive edge of clock when load\_seed was high, the output data of the LFSR takes on 1111, with lfsr\_done going high to signify the start of the pattern. Then, for every positive edge of the clock after, lfsr\_data takes on all the other 14 state patterns in a pseudorandom manner before going back to 1111, upon which lfsr\_done goes high for one clock period to signify the repetition of the pattern. This is the expected and correct behavior

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* The first half of the simulation is in right direction mode since direction input is low. From 0 to 400 ns, select is low meaning it is in shift mode. 1000 is loaded in, and shift value is incremented from 1 to 3. We subsequently see the loaded in data shifted to the right by the specified shift value, with a 0 being appended to the trailing end at dout e.g. 1000 to 0100. This is the correct behavior of right shift mode. After 400ns, select goes high, and now the module is in right rotate mode, so now the trailing end is appended with the overflow bit. We see this is the behavior observed e.g. 1101 loaded in becomes 1101 after being rotated to the right by 1.

Graphical user interface

Description automatically generated

* The second half of the simulation is in left direction mode since direction goes high. Thus we can observe the correct behaviors of left shift and rotation by 1, 2, and 3 bits.