Anh Tran

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EDUCATION

University of Pennsylvania, M.S.E in Electrical Engineering – GPA: 3.88/4.0 Sep 2024 – May 2026

Relevant coursework: HW/SW co-design for ML, Digital IC & VLSI Fundamentals, Computer Organization & Design, Modern Convex Optimization, F1/10 Autonomous Racing Cars, System-on-a-Chip Architecture (upcoming), General-Purpose GPU Architecture and Programming (upcoming), Graph Neural Network (upcoming)

VinUniversity, B.Sc in Electrical Engineering – GPA: 3.82/4.0 Sep 2021 – Jun 2025

Relevant coursework: Digital Logic & Computer Organization, Computer System Programming, Digital Signal and Image Processing, Artificial Intelligence, Natural Language Processing

SKILLS

Focus Areas: Computer Architecture, HW/SW co-design, VLSI, Deep Learning, Convex Optimization

Programming Languages: Python, C/C++, Verilog/System Verilog, MATLAB, Bash Script

Tools & Platforms: Linux, CUDA, Docker, Git, Cadence, Vivado Design Suite

Frameworks & Libraries: PyTorch, Jax, TensorFlow, TensorRT, OpenCV, ROS2

RESEARCH EXPERIENCE

Research Assistant | Implicit Deep Learning | VinUniversity Oct 2024

Supervised by: Professor Laurent El Ghaoui

- Designed experiments to verify and evaluate the generalization ability to various architectures (fully connected, residual, attention layer, RNN, etc.) of the implicit model, a new class of deep learning model proposed by Laurent El Ghaoui.
- Explored and deployed various solvers to solve fix-point equations, a key component in training the implicit model.
- Examined the sparsity and representational capacity of the implicit model by analyzing patterns in weight matrices.

Research Assistant | Satellite Imagery Super-resolution for Carbon Stocks Estimation | VinUniversity Oct 2024

Supervised by: Professor Nidal Kamel

- Utilized deep learning methods to super-resolve satellite images, incorporating dynamic high-pass filtering and channel attention to enhance image generation.
- Trained image-superesolution model using data from Vietnam's mountainous and forest regions.
- Used enhanced images as input for the carbon stock estimator, integrating neural networks to refine predictions.

PROFESSIONAL EXPERIENCE

AI/Data Engineer Intern | AlphaAsimov Robotics Sep 2024

- Performed data preprocessing and analysis to ensure readiness for AI model training; assesses the alignment of various modalities (camera, LIDAR, SOLAR, IMU, GPS, etc.) in the dataset.
- Designed tools, using Python and Bash Scripting, to streamline and partially automate the data verification process, incorporating descriptive visualizations and anomaly detection techniques.

PROJECTS

Pipelined RISC-V Processor May 2025

- Developed a custom 32-bit RISC-V core using SystemVerilog with a fully pipelined datapath, incorporating multicycle operators, direct-mapped instruction and data caches, and AXI4-Lite protocol for streamlined memory communication.
- Synthesizeed using the Yosys toolchain and deploy on a Lattice ECP5 FPGA, achieving a 31MHz maximum clock frequency with resource utilization of 30.9% LUTs and 4.1% flip-flops.

Autonomous Driving Systems for F1/10 Racing Car May 2025

- Developed autonomous driving modules on F1/10 car platform, including SLAM, particle filtering, reactive control, Pure Pursuit, and RRT-based planning.

- Integrated computer vision and deep learning models for perception tasks using the NVIDIA Jetson Orin, leveraging deep compression techniques and TensorRT framework to enhance real-time performance.

Fast, Compact and Efficient DNN via Pruning and Sparse Matrix Compression Dec 2024

- Implemented various pruning strategies (global, channel-wise, hard pruning), combined with quantization, to reduce model size while maintaining accuracy and accelerating inference.
- Developed custom linear layer leveraging Compressed Sparse Row format for efficient storage and inference in pruned networks.
- Achieved a 1.52× speed-up in the most pruned layer and reduce the overall model size by 43% on VGG16.

Configurable Logic Block (CLB) Design and Optimization Dec 2024

- Designed and verified a 16-bit CLB leveraging advanced 45nm Salicide CMOS technology within the Cadence environment.
- Performed transistor sizing, mitigate timing hazards, and optimized circuit for minimal delay and enhanced energy efficiency.
- Achieved a maximum operating frequency of 1GHz with an average power consumption of 134.9μW.

Greatest Common Divisor (GCD) and Multiply-and-Accumulate (MAC) design and optimization Jan 2024

- Developed a Finite State Machine (FSM)-based implementation of the Euclidean algorithm for computing the greatest common divisor (GCD).
- Designed a Multiply-and-Accumulate (MAC) unit.
- Wrote testbenches and perform simulation, synthesis, and timing analysis using Verilog and the Vivado Design Suite to evaluate and optimize resource utilization and clock frequency.

VeriFace - Instant, Low-Resource Face Verification System Jun 2023

- Developed a face recognition and verification app using OpenCV and C++.
- Combined pretrained SFace and YuNet models with Siamese network architecture, enabling recognition with minimal input images.
- Achieved 95% accuracy using a lightweight network and optimized data flow, without the need for computationally intensive training, making it suitable for deployment on edge devices.

LC-3 Virtual Machine on C Mar 2023

- Implemented an LC-3 microprocessor architecture simulator in C, including instruction set, registers, control unit, and a 3-stage working cycle.
- Verified the functionality of the LC-3 machine with LC-3 Assembly games including 2048, Hangman, and Rogue.

HONNORS & ACHIEVEMENTS

Vingroup Science and Technology Scholarship (for master study at the University of Pennsylvania) 2024

Excel Award for Exceptional Capability, VinUniversity 2023

Dean's List, VinUniversity 2021 – 2024

100% Merit-based Scholarship, VinUniversity 2021

First Prize, Vietnamese National Physics Competition for High School Students 2020

Gold Medal, Physics Competition for Specialized Students in the Northern Delta and Coastal Areas in Vietnam 2019