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**CECS 361 Fall 2019**

**Project 2: VGA Synchronization Design**

**Requirements Testing**

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| **Reset brings the VGA Synchronization circuit to a known state with all outputs inactiveA screenshot of a computer  Description automatically generated** |
| **The Synchronization Logic shall be updated at the 25Mhz**  **A screenshot of a computer  Description automatically generated** |
| **The Horizontal Scan Count shall be updated at the 25MHz**  **A screenshot of a computer  Description automatically generated** |
| **The Horizontal Scan Count shall range from 0 to 799**  **A screenshot of a computer  Description automatically generated** |
| **The Horizontal Sync signal shall be LOW ACTIVE and shall be active from Horizontal Scan Count 656-751**  **A screenshot of a computer  Description automatically generated** |
| **A screenshot of a computer  Description automatically generated** |
| **The Horizontal Video On signal shall be HIGH ACTIVE and shall be active from Horizontal Scan Count 0-639**  **A screenshot of a computer  Description automatically generated** |
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| **The Vertical Scan Count shall be updated at the completion of a Horizontal Scan**  **A screenshot of a computer  Description automatically generated** |
| **The Vertical Scan Count shall range from 0-524**  **A screenshot of a computer  Description automatically generated** |
| **The Vertical Sync signal shall be LOW ACTIVE and shall be active from Vertical Scan Count 490-491**  **A screenshot of a computer  Description automatically generated** |
| **The Vertical Video On signal shall be HIGH ACTIVE and shall be active from Vertical Scan Count 0-479**  **A close up of a computer  Description automatically generated** |
| **A screenshot of a computer  Description automatically generated** |

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| **The Video On signal shall be HIGH ACTIVE and shall be active when Horizontal Video On and Vertical Video On are active at the same time**  **A close up of a device  Description automatically generated** |

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| **The RGB signals shall be driven while the Video On signal is ACTIVE. When the Video On signal is INACTIVE the RGB signals shall be held at 0**  **A screenshot of a computer  Description automatically generated** |