T.Y.B.Tech (CSE)

System Software and Compilers(SSC)

Theory Assignment - 1

Name: Aniruddha Shende

Roll number: PD-05

Batch: D1

Panel: D

Batch:- D1

ASSIGNMENT / TEST BOOKLET

Student's Name : Aniruddha   Arun   Shende

Class : T· Y· Btech   Division : D   Roll No : PD-05   Academic Year : 2021-2022

Subject : SSC   Theory Assignment / Test No : 1   Date :

PLEDGE

I solemnly affirm that I have written this Assignment/Test based on my own preparation. I have neither copied it from others nor given it to others for coping. I know that this is to be submitted as a part of my submission at the end of the term.

Shende.
Signature of the student

Q. No.	1	2	3	4	5	6	7	8	9	10	Total	
Marks/Grade												

Name & Sign of the faculty Member

(Please start writing assignment/ test from here)

T· Y· BTech CSE

Subject :- System Software & Compiler (CS331)

Theory Assignment - 1

Batch :- D1

Q·1· Show the contents of the symbol table, Literal table, Pool table, & Intermediate code generated at the end of Pass 1 of an Assembler.

```
START 200
READ A
MULT AREG, B
MOVER AREG, = '2'
MOVEM AREG, C
```

mitwpu.edu.in

```
ADD   BREG, ='2'
LTORG
MOVER  AREG, ='7'
MOVEM  AREG, B
MULT   CREG, D
STOP
C  DS  5
D  DS  1
A  DC  3
B  DS  4
END
```

Ans.1. At the end of the Pass-I :-
@ Intermediate code

ALP	LC	Mnemonic	Op1	Op2
			I/C Code	
START 200	−	(AD,01)	−	(C,200)
READ A	200	(IS,09)	−	(S,01)
MULT AREG,B	201	(IS,03)	1	(S,02)
MOVER AREG,='2'	202	(IS,04)	1	(L,01)
MOVEM AREG,C	203	(IS,05)	1	(S,03)
ADD BREG,='2'	204	(IS,01)	2	(L,01)
LTORG	205	(AD,05)	−	002
MOVER AREG,='7'	206	(IS,04)	1	(L,02)
MOVEM AREG,B	207	(IS,05)	1	(S,02)
MULT CREG,D	208	(IS,03)	3	(S,04)
STOP	209	(IS,00)	−	−
C DS 5	210	(IS,	−	(C,05)
		(DL,02)		

ASSIGNMENT /
TEST Page No.

D	DS 1	215	(DL,02)	—	(C,1)
A	DC 3	216	(DL,01)	—	(C,3)
B	DS 4	217	(DL,02)	—	(C,4)
END		221	(AD,02)	—	007

ⓑ Symbol Table:-

Sym-id	Sym-name	Sym-addr	Length	
1	A	216	1	
2	B	217	1	
3	C	210	1	
4	D	215	1	

ⓒ Literal Table:-

Lit-no	Literal	Addr	
1	='2'	205	
2	='7'	221	

ⓓ Pool Table:-

POOLTAB[1] = 1

POOLTAB[2] = 2

4

Q.2. With respect to the design of TWO PASS ASSEMBLER, state whether following statements are true or false. Justify your answer for each case.

(i.) Literals are processed in Pass II.

⇒ False

Literals are processed in Pass I.

(ii.) Undefined Symbols are detected in Pass I.

⇒ True.

Undefined symbols are detected in Pass I and are added to the Symbol Table.