CODE:

Top Module

```
1 —LIBRARIES TO USE
2 library IEEE;
3 use IEEE.STD_LOGIC_1164.ALL;
4 use IEEE.NUMERIC_STD.ALL;
  --ENTITY OF 8 bit Floating Point Multiplier top module
  entity floating_point_mul is
7
    port( num1 : in unsigned(7 downto 0);
8
         num2 : in unsigned(7 downto 0);
9
        output: out unsigned (7 downto 0);
10
        op_flag:out std_logic);
11
12 end floating_point_mul;
13
14 ——ARCHTECTURE
15 architecture Behavioral of floating_point_mul is
16
17
  ---COMPONENT OF MULTIPLIER
18
19 component mul_8bit is
      Port ( a : in unsigned (7 downto 0);
20
                     unsigned (7 downto 0);
21
             b: in
             prod : out unsigned(7 downto 0);
22
             sflag : out std_logic);
23
24
25 end component;
27 ---MAIN BODY
28 begin
29
30 —FLOATING POINT MULTIPLIER
31 FLT_MUL_INS: mul_8bit port map(a=>num1,b=>num2,prod=>output,sflag=>op_flag);
33 —END OF ARCHITECTURE
34 end Behavioral;
```

Multipler

```
-Floating Point Multiplier
3 library IEEE;
4 use IEEE.STD_LOGIC_1164.ALL;
  use IEEE.NUMERIC_STD.ALL;
5
6
7
  entity mul_8bit is
8
      Port (a: in unsigned (7 downto 0);
             b: in unsigned (7 downto 0);
9
10
              prod : out unsigned (7 downto 0);
              sflag : out std_logic);
11
12 end mul_8bit;
13
14 architecture Behavioral of mul-8bit is
15
```

```
16 begin
17
     process (a,b)
       -declaring variable for each part of the floating point number
18
      variable sign_a , sign_b , sign_z , svar: std_logic;
19
      variable exp_a, exp_b, exp_z: unsigned(3 downto 0);
20
21
      variable man_a, man_b: unsigned(4 downto 0);
      variable man_z: unsigned(9 downto 0);
22
23
24
     --1) checking infinite value in inputs
     if (a(6 downto 4)="111" or b(6 downto 4)="111") then
25
26
     sflag \le 0';
     prod<="01110000";
27
      else
28
29
           2) assigning value to each variable
30
           sign_a := a(7);
31
           \operatorname{sign}_{-b} := b(7);
32
           \exp_a(2 \text{ downto } 0) := a(6 \text{ downto } 4);
33
           \exp_{a}(3) := 0;
34
           \exp_b(2 \text{ downto } 0) := b(6 \text{ downto } 4);
35
           \exp_{-b}(3) := '0';
36
           man_a(3 \text{ downto } 0) := a(3 \text{ downto } 0);
37
           man_b(3 \quad downto \quad 0) := b(3 \quad downto \quad 0);
38
39
           man_a(4) := '1';
           man_b(4) := '1';
40
          -3) success if nothing lowers success flag
41
42
           svar := '1';
43
44
        --4) adding exponents
           \exp_z := \exp_a + \exp_b;
45
          - subtracting bias
46
           \exp_z := \exp_z - 0011";
47
        --5) checking overflow
48
           if \exp_z(3) = 1, then
49
             \operatorname{svar} := '0';
50
           end if;
51
52
53
        --6) multiplying mantissas
           man_z := resize(man_a*man_b, 10);
54
55
        --7) normalising and shifting exp
56
57
           if (\max_{z}(9) = '1') then
             man_z := man_z srl 1;
58
             \exp_z := \exp_z + 0001";
59
60
           end if;
61
        --8) raising overflow flag and lowering sucess flag
62
           if (\exp_{z}(3) = 1) then
63
             svar := '0';
64
           end if;
65
66
        -- 9) calculating sign of product
67
           sign_z := sign_a xor sign_b;
68
69
        -- 10) Assigning final values to prod
70
           \operatorname{prod}(3 \operatorname{downto} 0) \leq \operatorname{man}_{z}(7 \operatorname{downto} 4);
71
           \operatorname{prod}(6 \operatorname{downto} 4) \leq \exp_{z}(2 \operatorname{downto} 0);
72
           \operatorname{prod}(7) \leq \operatorname{sign}_{z};
73
           sflag \le svar;
74
75
        end if;
        end process;
76
77 end Behavioral;
```

Hardware Description Language (ECL-302)							