The Application of MUX in the Realming of Domino Logic, Dynamic Consequently, and Transmission Gates: A Case Study with Performance Calculation.

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***Abstract*— Multiplexers (MUX) are one of the most important components of communication systems. To increase data transmission efficiency, utilize the vast memory space of a computer in an effective way, and convert parallel data into serial form in telecommunication networks, an efficient design of low power-delay MUX is required. Thus, a basic 4:1 MUX is created in this study employing a variety of CMOS logic families, including static CMOS logic, pseudo-NMOS logic, Domino logic, dynamic logic, mux using a transmission gate, and dual-rail Domino logic, to determine the best suitable logic family for creating higher levels of MUX. The implementation is done in VLSI technology, as it has features like small size, low cost, high operating speed, and low power. The performance analysis of the MUX using various CMOS logic families is conducted using a VLSI back-hand tool: Cadence VIRTUOSO SCHEMATIC EDITOR 6.1 at 180nm. Based on the results obtained, it is determined that a Domino logic based 4:1 MUX is the most efficient. Its average power consumption is 20.06%, and its PDP (power delay product) is 20.1% lower than other logic families. But trade-offs are inferred between Domino logic and static CMOS logic, which can be neglected when considering overall performance. This work suggests that any higher-level MUX with low power-delay and PDP can be achieved using Domino logic since it outperforms the other logic families**

***Keywords*—** MUX, domino logic, dynamic logic, power analysis

I. INTRODUCTION

A multiplexer, sometimes known as a "MUX," is a digital circuit that selects one of numerous input signals and sends it to a single output line. Digital communication systems, such as data transmission, often employ it to enhance data transmission efficiency by allowing the transmission of many signals on a single communication channel. Multiplexers can also be used to reduce the cost of a system, as fewer communication channels are required. They are also used to route signals from different sources to the same destination

In the following circuit level description, domino logic is used to construct a 4:1 MUX, using two main components/phase.

Precharge phase: A precharge transistor and a precharge node make up the precharge network.

The precharge transistor is an NMOS transistor with a clock signal (CLK) linked to its gate.

The output of the MUX is connected to the precharge node, which is precharged to VDD throughout the precharge period.The gate terminals of the pass transistors are connected to the input signals.

Two pass transistors plus an evaluation node make up the evaluate network.

The evaluation node is precharged to VDD initially during the precharge phase and connected to the MUX's output.

The evaluation node and the input are connected by the first pass transistor (T1). if the select signal (S) is low, and disconnects it if it is high, during the assess phase.

If the select signal is high, the second pass transistor (T2) links the evaluation node to the input during the evaluate phase. If the select signal is low, it disconnects it.

The voltage level at the evaluation node following the evaluation phase controls the MUX's output.

The 4:1 MUX using domino logic can be implemented with fewer transistors than static logic implementations. Nevertheless, it requires a clock signal to operate and may suffer from dynamic hazards This can lead to increased power consumption and greater circuit complexity. Additionally, as the clock frequency increases, the circuit becomes more susceptible to noise and reliability issues.

II. DESIGN AND IMPLEMENTATION

A. DEMUX 1:4

The data splitter, also known as a demultiplexer, or demultiplexer for short, is the exact opposite of a multiplexer. The demultiplexer takes a single line of input data and switches it sequentially to any number of output lines. The demultiplexer converts a serial data signal on its input to a parallel data signal on its output lines, as shown below. The Demultiplexer switches one common data input line to any one of the 4 output data lines A to D in our example above. As with the multiplexer the individual solid state switches are

selected by the binary input address code on the output select pins “a” and “b” as shown. The demultiplexer is used to process signals that are encoded in parallel form, such as digital computers. It is also used in applications that require a high data transfer rate.

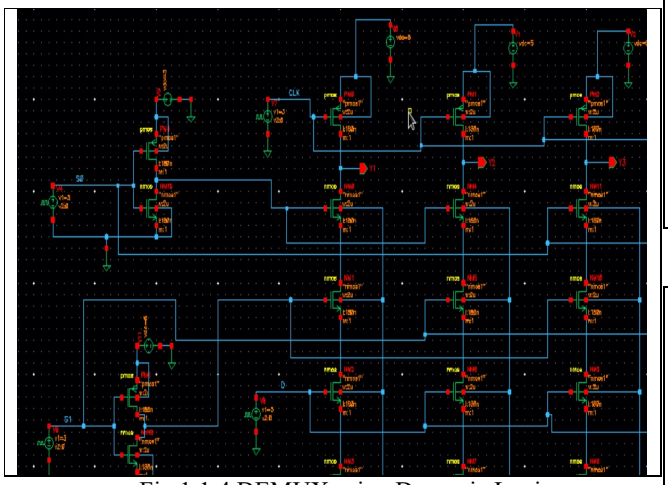

Fig 1:1:4 DEMUX using Dynamic Logic

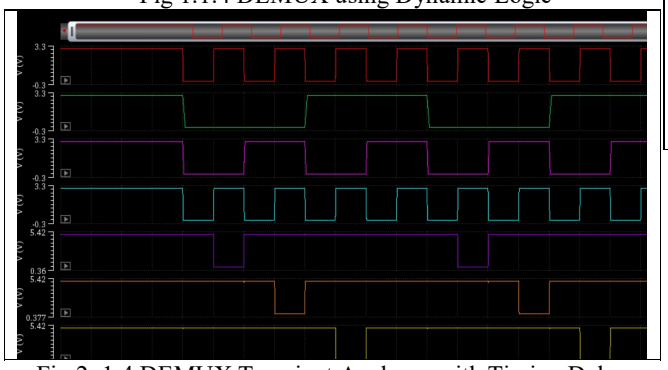

Fig 2: 1:4 DEMUX Transient Analyses with Timing Delay

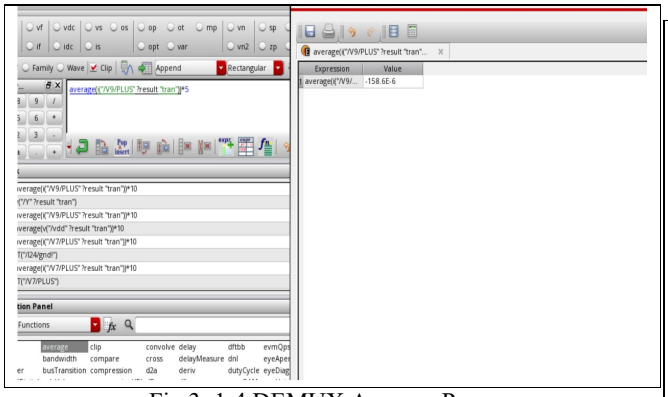

Fig 3: 1:4 DEMUX Average Powers

B MUX 4:1

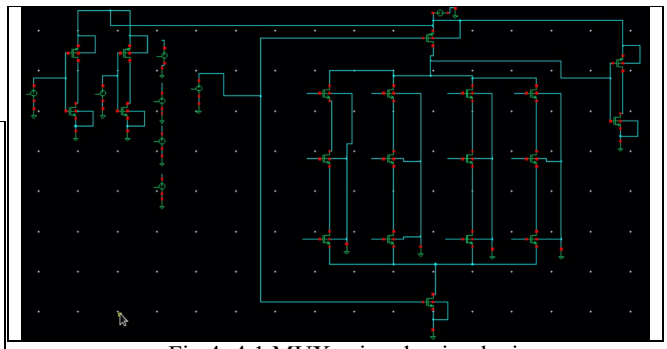

Fig 4: 4:1 MUX using domino logic

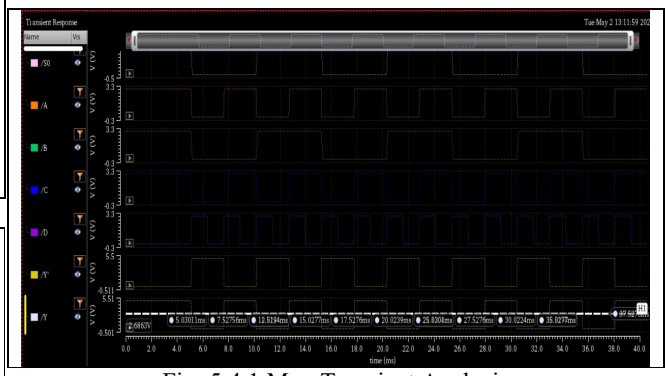

Fig: 5:4:1 Mux Transient Analysis

III. Application Level Implementation

A. Using Transmission Gates

Transmission gates are electronic components that pass electrical signals from one circuit to another. They are used in digital systems to control the flow of data and information.

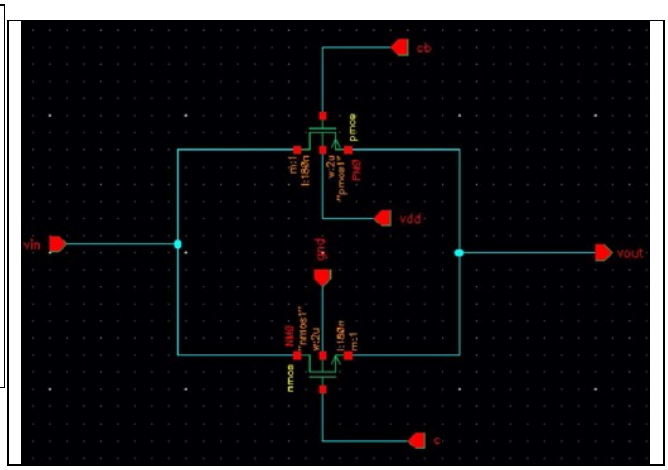

Fig 6: schematic -Transmission Gate

They are key components of computers and other digital systems. Block electrical signals in a circuit. Transmission gates can be used as analog switches or pass gates. The advantage of using transmission gates over other types of switches is their ability to switch signals with low resistance and minimal distortion; they also require less power to operate and are capable of switching faster than other types of switches. Additionally, they are less prone to errors due to noise or other interference

In Figure 6 the drain of PMOS and source of NMOS serve as switches that control the flow of current from one transistor to another. The drain and source of the transistors act to turn the current on or off, depending on the gate voltage applied. This allows for a controlled flow of current for specific applications. inputs while the output is measured across the source of PMOS and drain of NMOS. In NMOS, the body is connected to ground, while in PMOS, the body is connected to VDD.The NMOS transistor Vds and Vgs

- VDS=VDD-Vout
- VGS=VDD-Vout

Therefore the operation of NMOS is

- Turn off when Vgs<Vtn
- Operational mode when VGS>=Vtn

Operates in saturation when Vout > Vgs —lVtpl

The PMOS transistor Vds and Vgs

- VDS=Vout- VDD
- VGS=-Vout

Therefore the operation of NMOS is

- Turn off when VGS>lVtpl
- Operational mode when Vgs<=lVtpl

Operates in saturation when Vout<Vgs —lVtpl

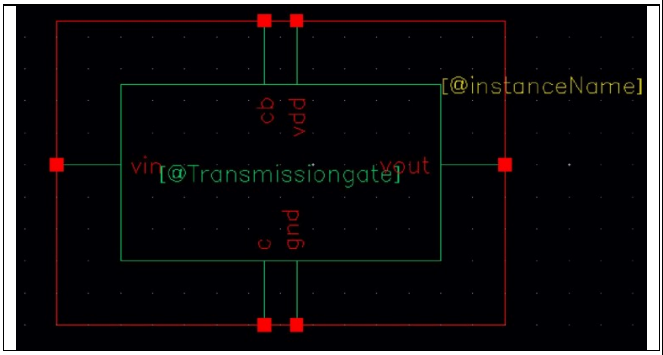

Fig 7: symbol generated for Transmission Gate to use as standard cell for next level implementation

Here the transmission gate is converted into a black box, so that it can be used repeatedly as per requirement. A black box is a system, whose inputs and outputs are clearly visible, but not the internal structure and working. By converting the transmission gate into a black box, it can be used for multiple applications without needing to understand the underlying internal structure and working of the system. This makes it easier to use and more efficient in terms of cost and time. Furthermore, it simplifies the process of troubleshooting, as it is not necessary to understand the underlying system in order to fix any issues. This also makes it easier to upgrade and modify the system in the future.

In figure 10 The three signals are represented by the blue, green, and yellow lines. They are used to control the operation of the system. The x-axis is the time and the y-axis is the amplitude of each signal.

a. S2: Time period- 40ns Voltage range - 0 to 4V
b. SI: Time period- 20ns Voltage range - 0 to 4V
c. S0: Time period- 10ns Voltage range - 0 to 4V

This transient analysis helps to measure the accuracy of the system's response. The response is analysed based on its time domain parameters such as rise time, settling time, peak time and peak value. The results are then compared to the expected values to determine the system's performance.

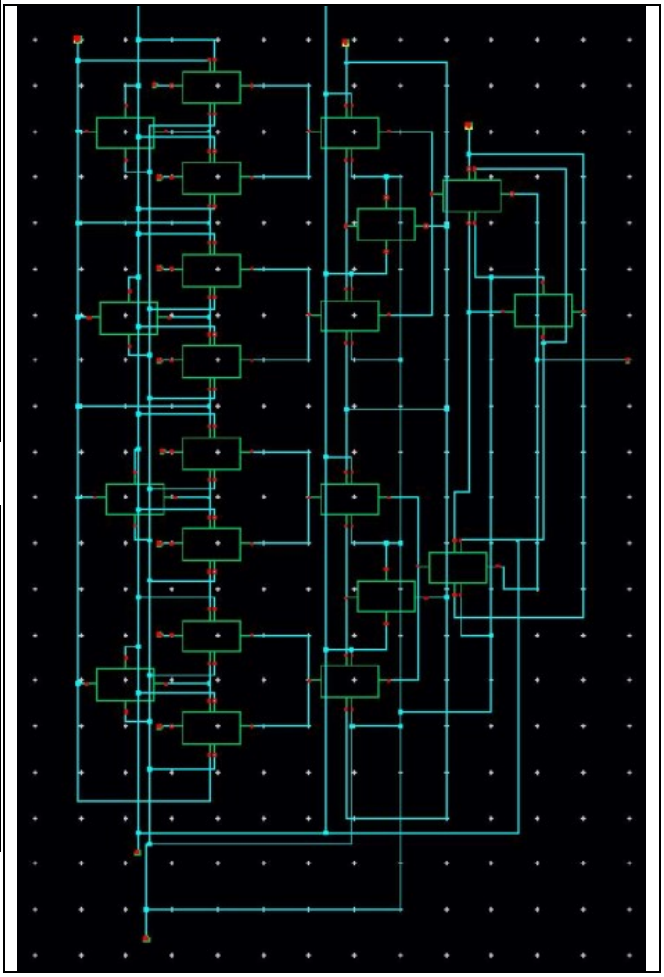

Fig 8: transmission gates and inverters are used to build an 8:1 MUX

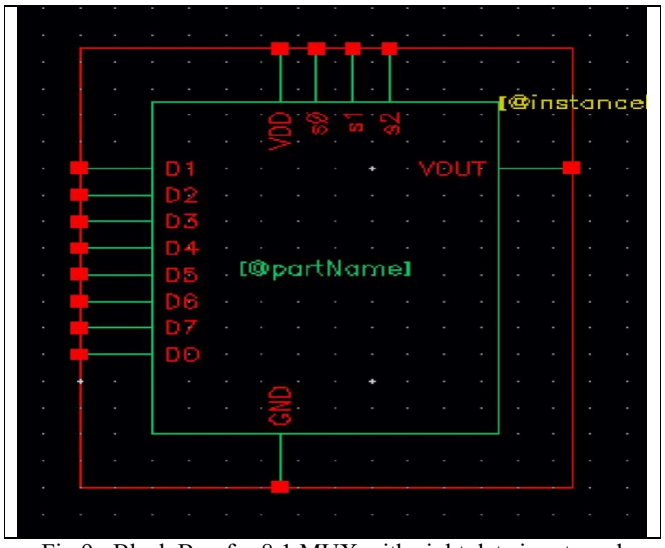

Fig 9 : Black Box for 8:1 MUX with eight data inputs and three control signals and one output port along with default pins Ground and VDD

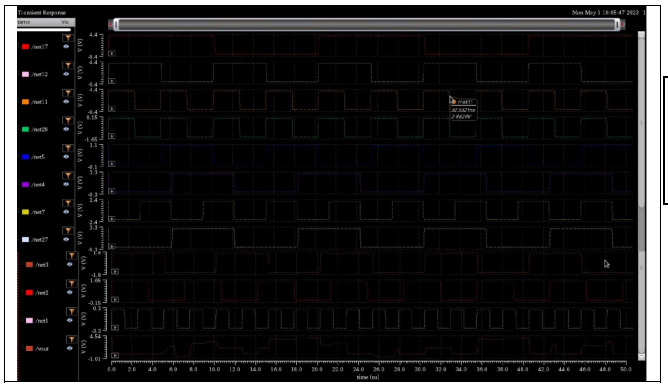

Fig 10: Transient Response covering all the possible test samples of data inputs and control signals.

B. Power calculations

Power calculations are needed to determine the sample size needed for a study to have the desired statistical power. They are significant in determining study reliability. Power calculations can help ensure that the study can detect a real effect if one is present.

1. Battery life: Many portable devices that rely on batteries use VLSI circuits. High power usage can quickly deplete the battery, reducing device operating time. VLSI circuits are designed to be very efficient, but they can still consume a lot of power. This is especially true when the device is performing computationally demanding tasks. Over time, the power usage of these circuits can cause the battery to deplete; reducing the device's operating time.
2. Energy efficiency: As worries about energy use and the environment grow, so does the demand for energy-efficient technology. A system's overall energy consumption can be decreased by optimizing power consumption. This is a key factor in determining a device's energy efficiency. By producing devices with lower power consumption, energy waste can be minimized. This can reduce the amount of energy consumed and contribute to a more sustainable future. Manufacturers should design products to require the least amount of energy possible. Additionally, users should ensure that their devices are set up for optimal energy efficiency and are not using more energy than necessary. Finally, recycling and repurposing electronics can also reduce energy waste.
3. Cost: High power consumption may result in higher costs because the circuit may need more expensive cooling systems or power supplies to handle the heat additionally, higher power consumption could lead to reduced reliability of the circuit due to thermal stress. This may lead to additional maintenance costs in the long run.

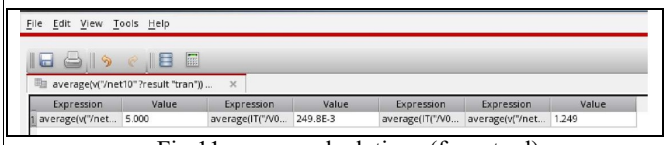

Fig 11: power calculations (from tool)

The current is 249.8 e-3 and the voltage is VDD 5 volts, so using the equation P=VI to calculate the power of an 8:1 MUX using TG, the average power is 1.249 watts.

IV. CONCLUSIONS

A 4:1 MUX and DEMUX is a digital circuit that selects one of four input signals and passes it to the output based on a control signal. It can be implemented using various logic gates like AND, OR, NAND, NOT, etc. The selection of input signals is based on the control signal value. Input signal selection is controlled by logic gate connections and input values. The 4:1 MUX is widely used in digital systems to switch between varieties of data inputs and multiplex them. It is also used to select one of several data paths within a digital system. The 4:1 MUX can be utilized for various applications, such as switching between multiple data sources or selecting between various data path

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technologies and products for diverse applications.' The research center provides a range of resources and facilities for students to explore and innovate in electronics and communications

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