

Summer School – 2024

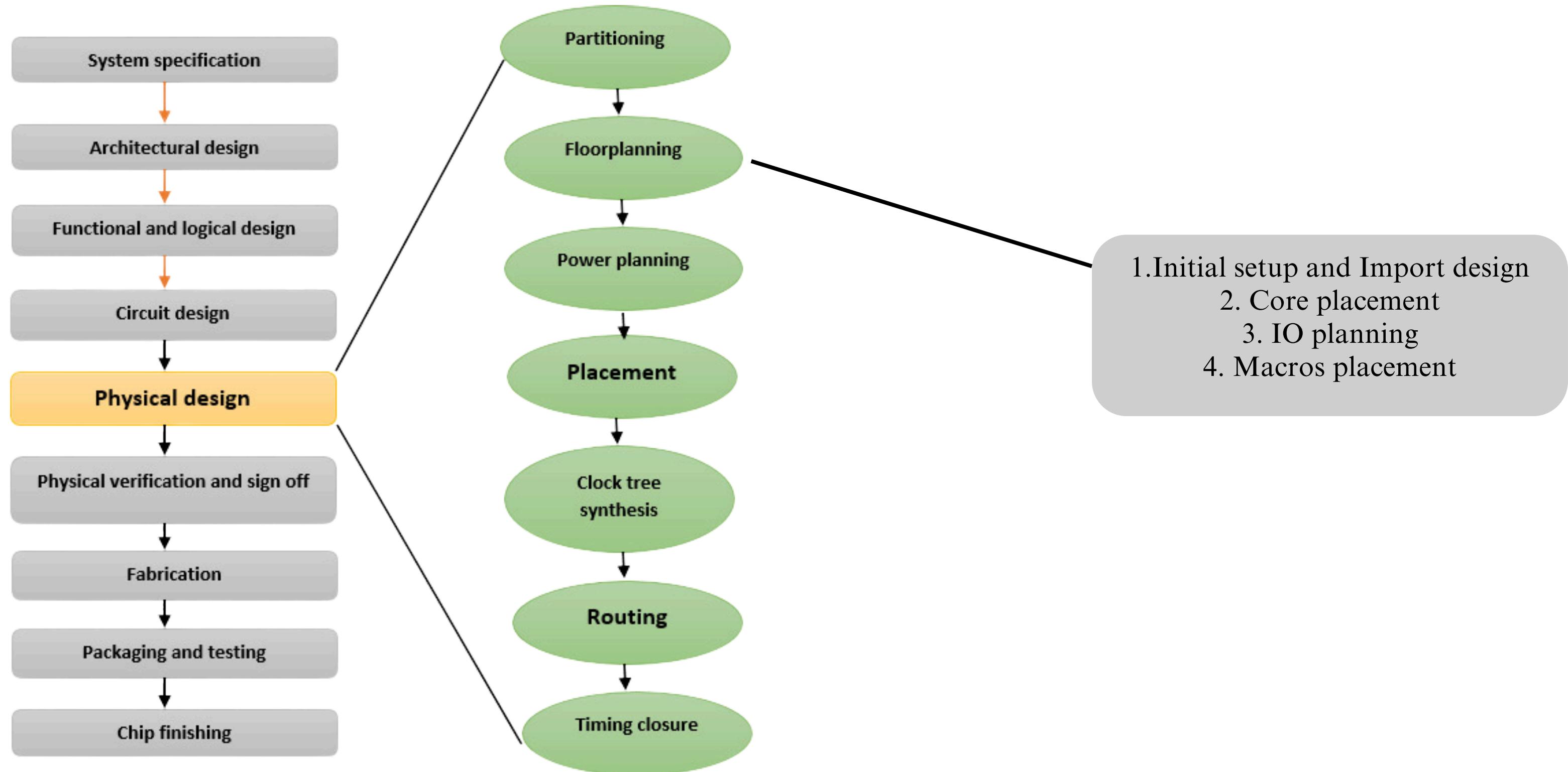
FPGA Design and 180nm Standard Cell Flow

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PES University | Electronic City Campus

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Standard Cell based ASIC Design flow

Physical design flow



Standard Cell based ASIC Design flow

File types



1. Synopsys Design Constraint file (.sdc)

- Timing Constraints - to meet timing requirements like Clock definitions, delays, Clock exceptions, etc.
- Input and Output Constraints - Specify the required times for input-output signals relative to the clock.

2. Cap Table file

- Parasitic capacitance values, Capacitance values for different dimensions

3. LEF files

- Technology Information, Route Information, Design Rules, Layer Information, Via Definitions

4. LIB files

- Library Name and Version
- Defines the units for measurements
- Technology information

Standard Cell based ASIC Design flow

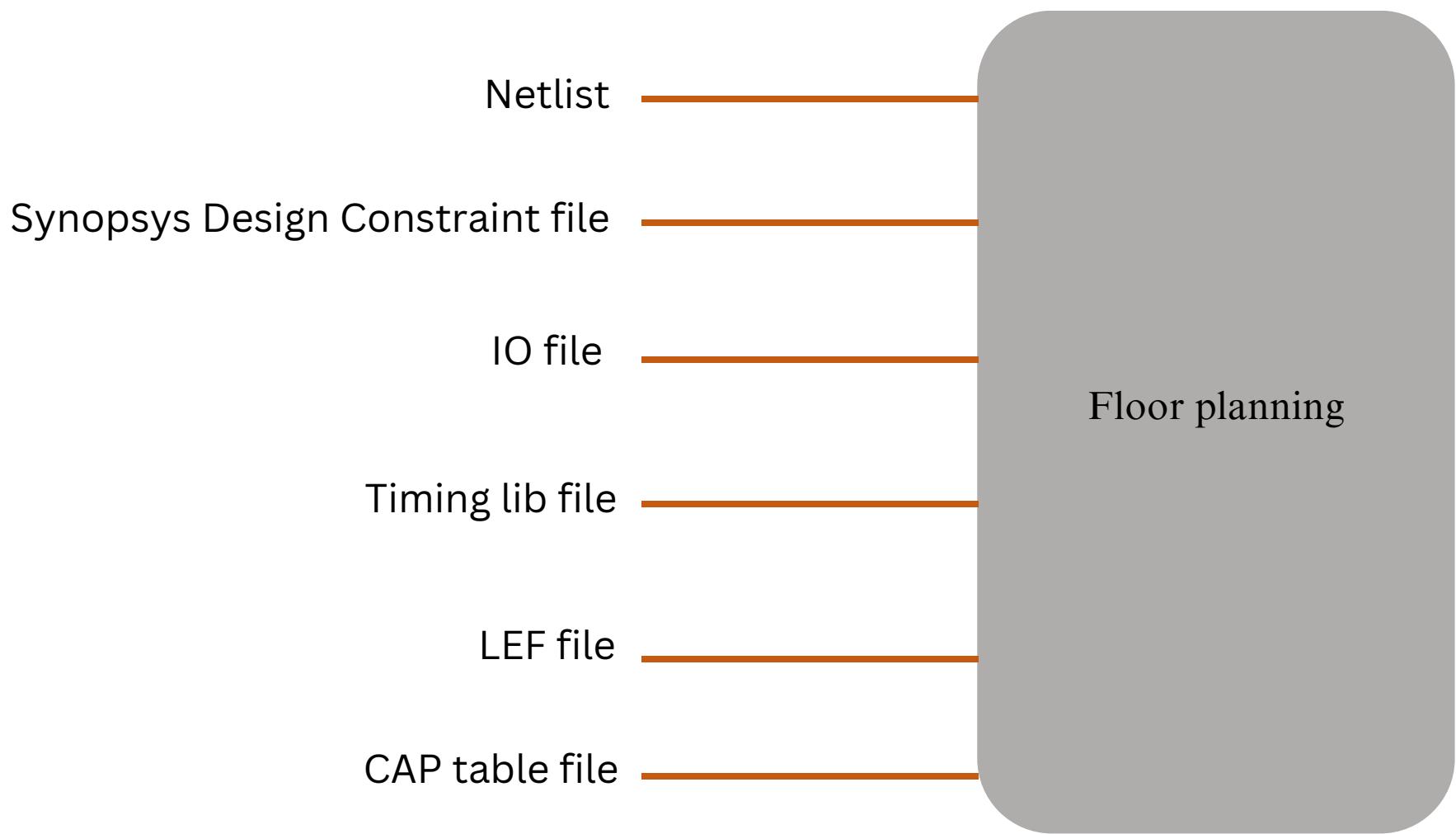
Physical design flow



Importing the design

Standard Cell based ASIC Design flow

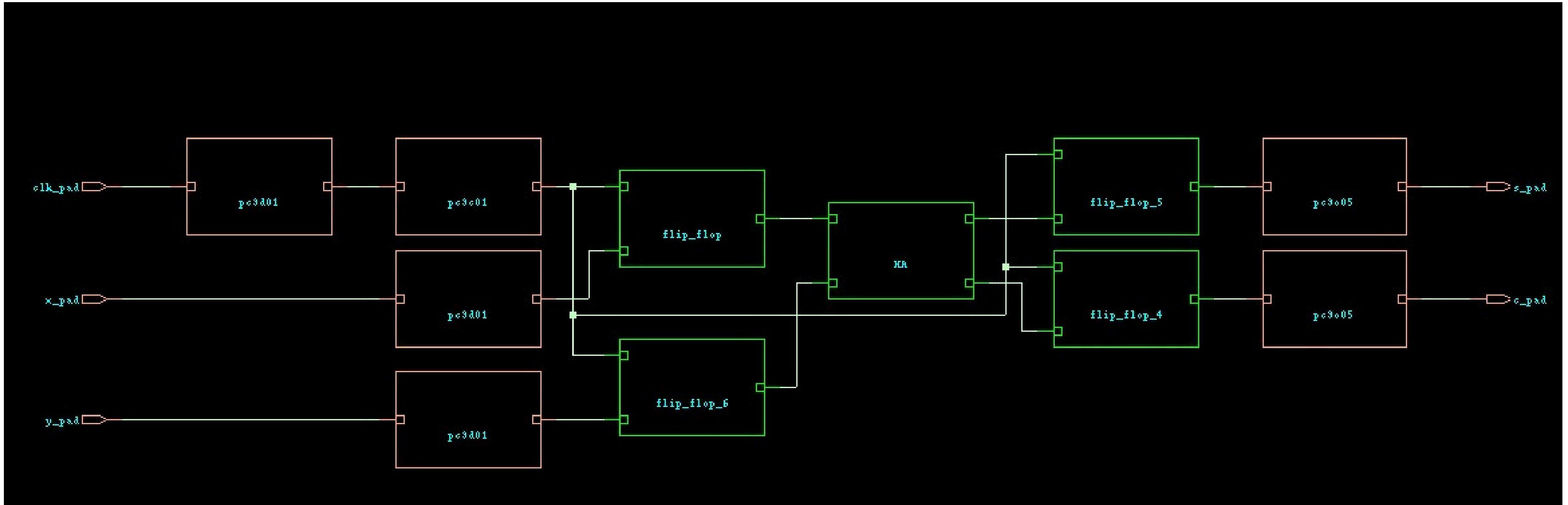
Import design



From Synthesis	From PDK	From user
Netlist file	LEF Files	IO File
.sdc file	CAP table file	(.view file)
-	LIB files	-

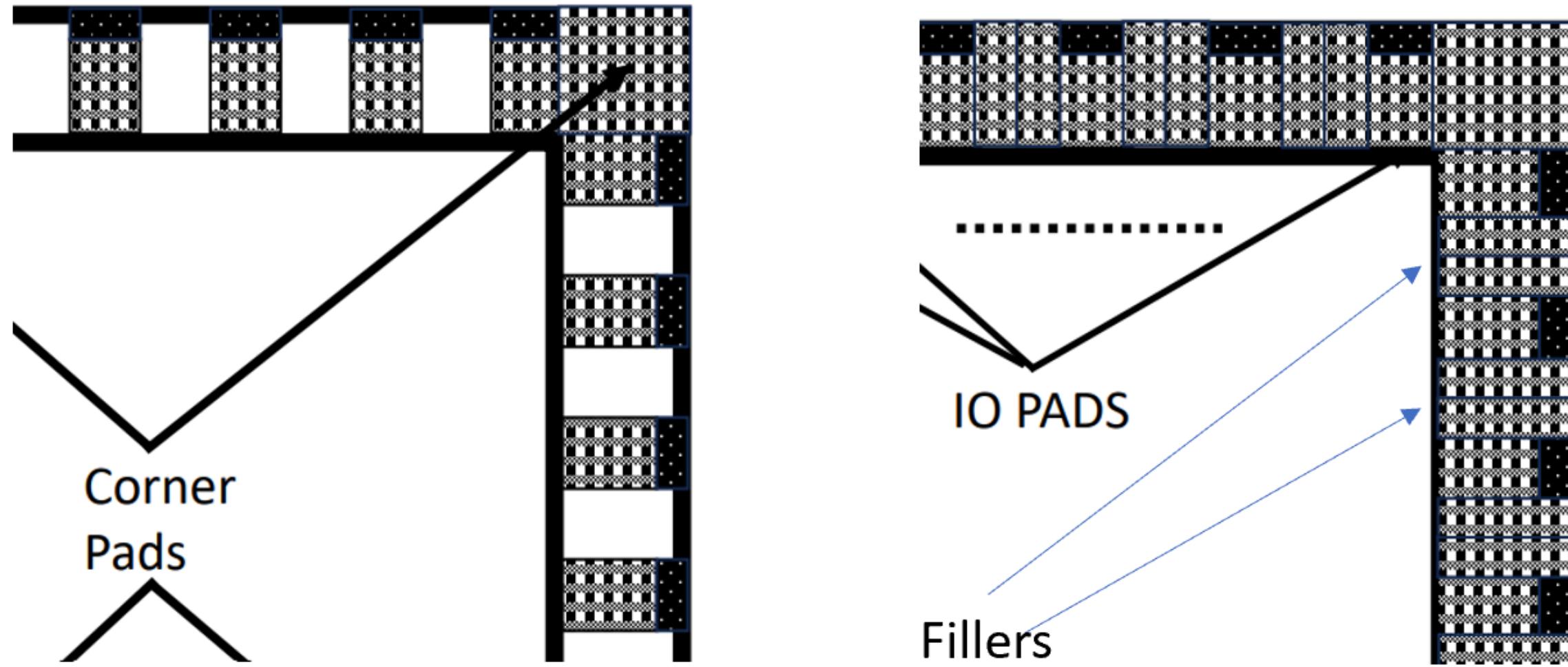
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IO file



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IO file



- 1. pc3c01- Clock pad
- 2. pc3d01- Data input pad
- 3. pc30o5- Data output pad

- 1. pvdi
- 2. pv0i
- 3. pvda
- 4. pv0a

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Multi-mode Multi-corner analysis



- Timing analysis using library files
 - Slow cells
 - Fast cells
- RC corners (using Cap Table)
 - Interconnect delays can significantly impact the overall timing of a circuit.
 - Best case - This represents the scenario with the least resistance and capacitance, leading to the fastest signal propagation.
 - Worst case - Represents the scenario with the highest resistance and capacitance, leading to the slowest signal propagation
- Operating conditions
 - Process corners
 - Voltage corners
 - Temperature corners
- Delay corners
- Setup analysis
- Hold analysis

PVT Corners				
Sl.No.	Corners	Voltage (V)	Temp.(°C)	Process
1	Max	1.62	125	ss (slow-slow)
2	Typ	1.8	25	tt (typical)
3	Min	1.98	-40	ff (fast-fast)

Standard Cell based ASIC Design flow

Sanity checks



- Design checks
 - Floating pins
 - Undriven inputs
 - Unloaded outputs
 - Port direction matching
 - Multiple driver checks

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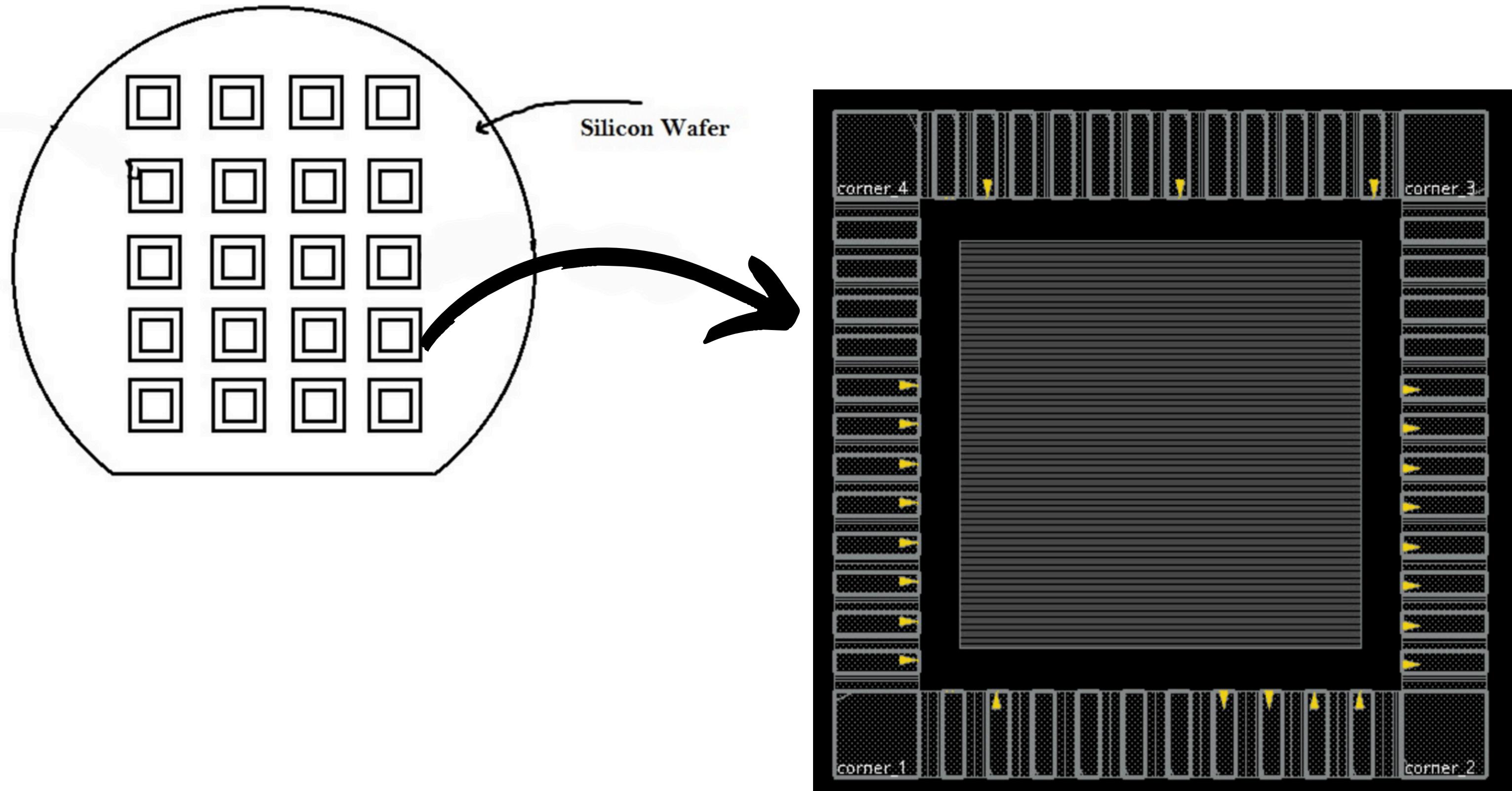
Physical design flow



Floorplanning

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Die and Core



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Die and Core



Instance	Module	Cell Count	Cell Area	Net Area	Total Area	Wireload

dsgn		11	8045.460	1.236	8046.696	16000 (S)
HA1	HA	1	34.500	0.000	34.500	ForQA (S)
f1	flip_flop	1	59.580	0.000	59.580	ForQA (S)
f2	flip_flop_6	1	59.580	0.000	59.580	ForQA (S)
f3	flip_flop_5	1	59.580	0.000	59.580	ForQA (S)
f4	flip_flop_4	1	59.580	0.000	59.580	ForQA (S)
(S) = wireload was automatically selected						

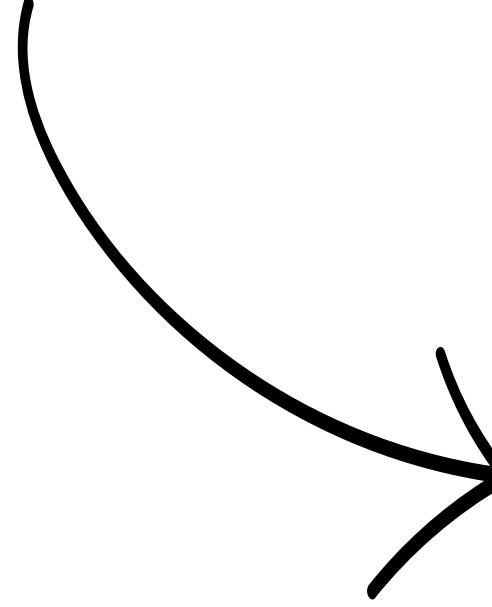
Die area = Core area + IO area + seal-ring area

Core area = {(Std. cell area / Std. cell utilization) + Macros + Halos}

$$\begin{aligned}\text{Core area} &= (34.5/0.42) + ((59.58/0.73)*4) \\ &= \mathbf{406.83 \text{ square micrometers}}\end{aligned}$$

Standard Cell based ASIC Design flow

IO Fillers



- IO fillers are used to fill gaps between functional I/O cells (such as input/output pads, power pads, and ground pads) to maintain uniform spacing and alignment along the chip's edge.
- They ensure the physical integrity of the chip by preventing gaps that could lead to physical damage or manufacturing defects.

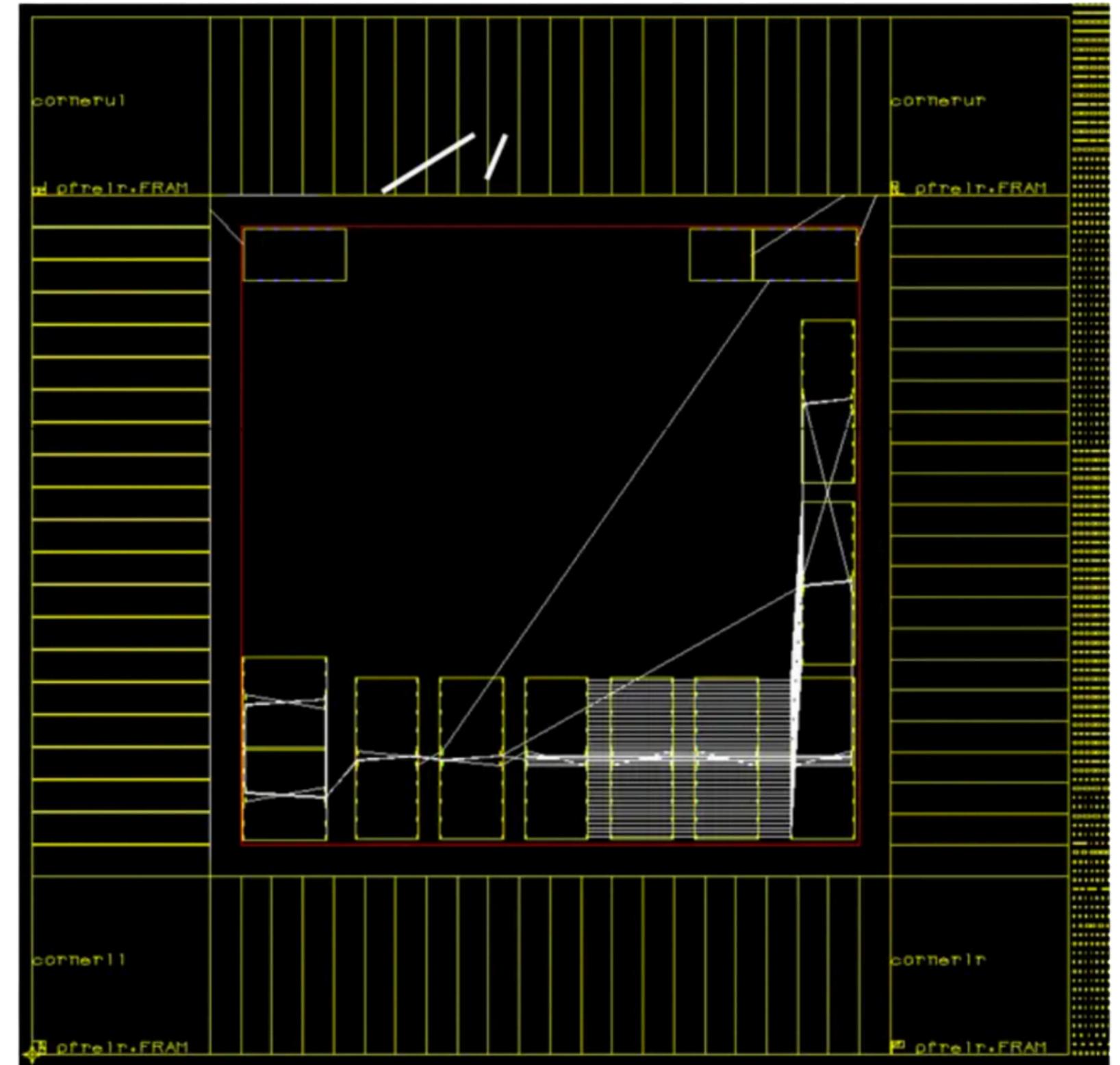
Name	Width (um)
pfeed00010	0.01
pfeed00040	0.04
pfeed00120	0.12
pfeed00540	0.54
pfeed01000	1
pfeed02000	2
pfeed10000	10
pfeed30000	30
pfrelr	Corner Pad

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Macros placement



- Placing macros early is crucial due to their **size and complexity**. This ensures adequate space allocation, optimizing floorplan and preventing design issues later.
- **Placed at the edges-** Placing macros near the chip's edges minimizes the distance to I/O pads, reducing routing complexity and improving signal integrity.

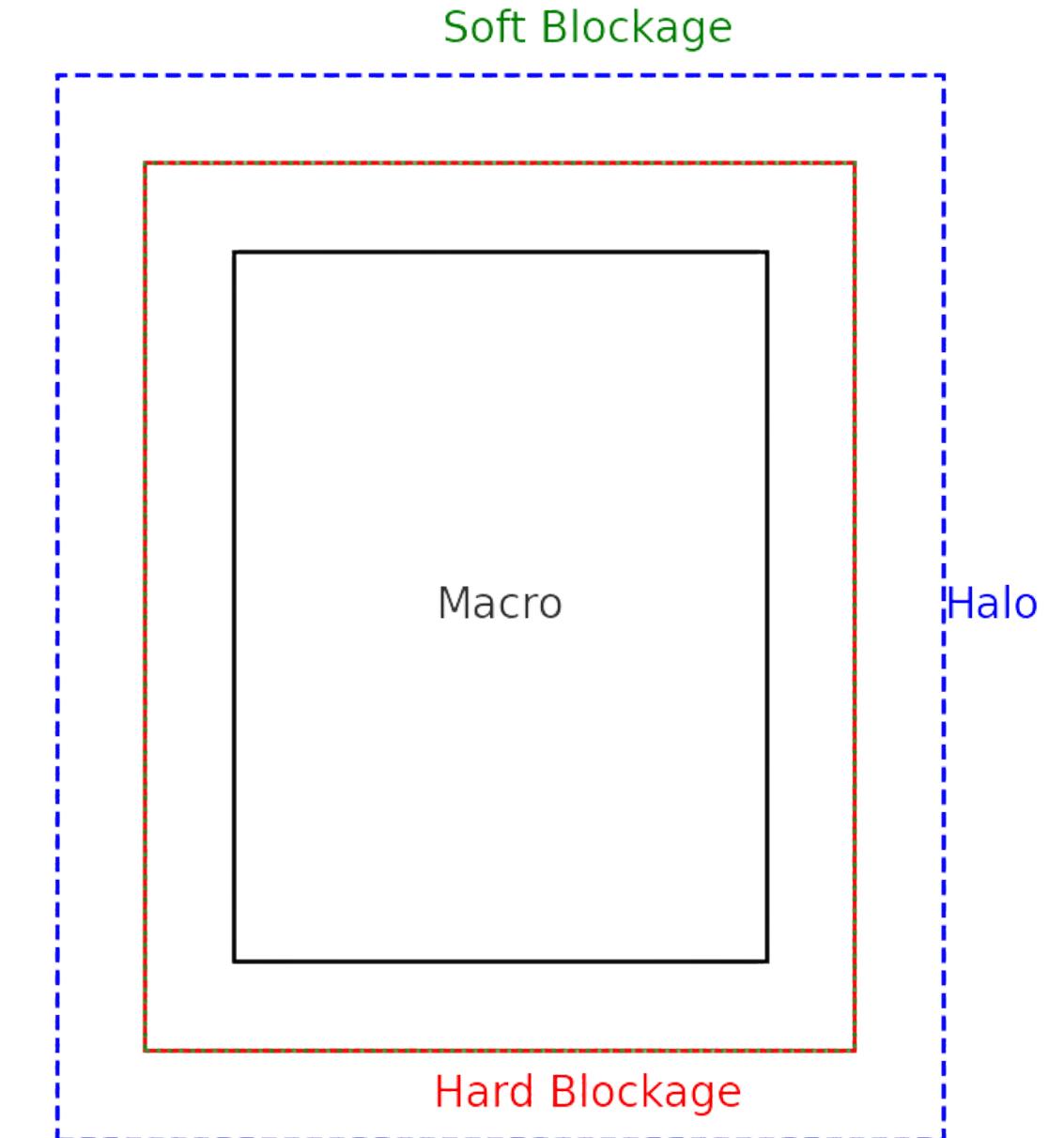


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Blockages and Halos

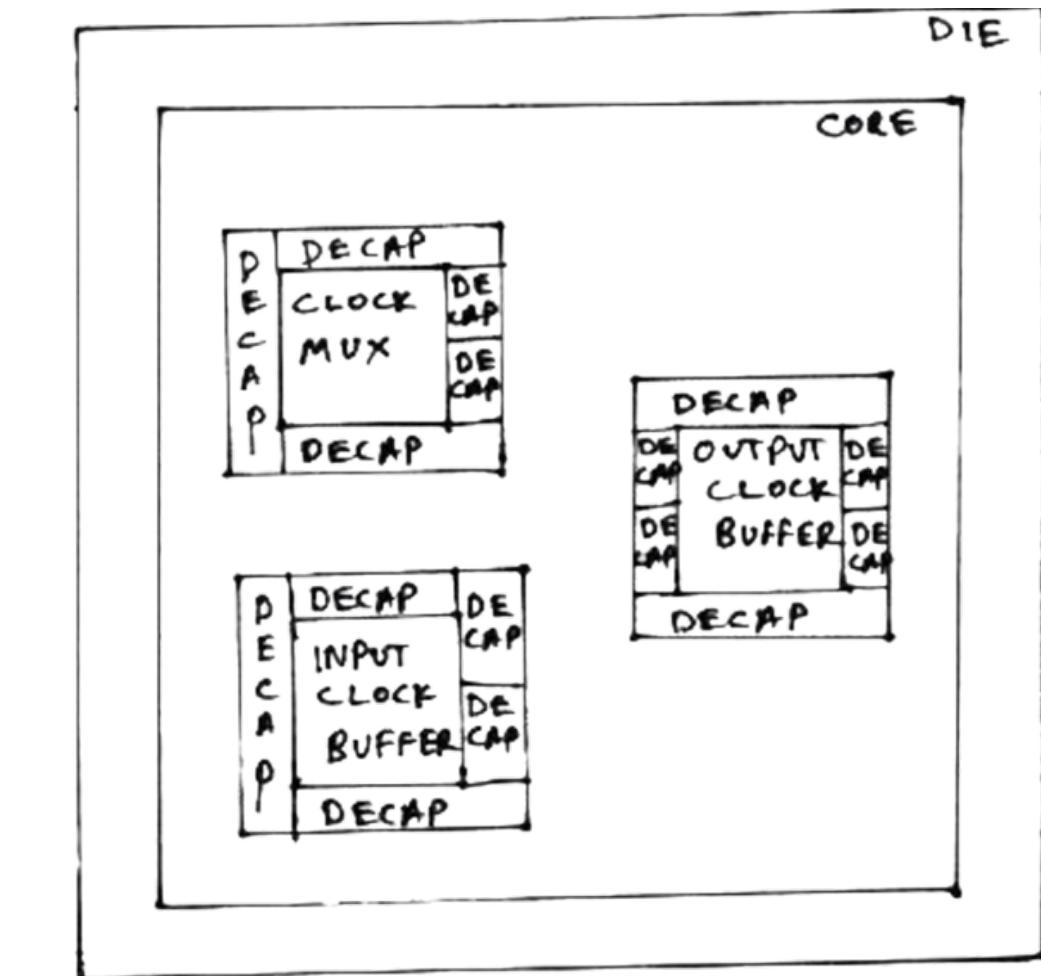
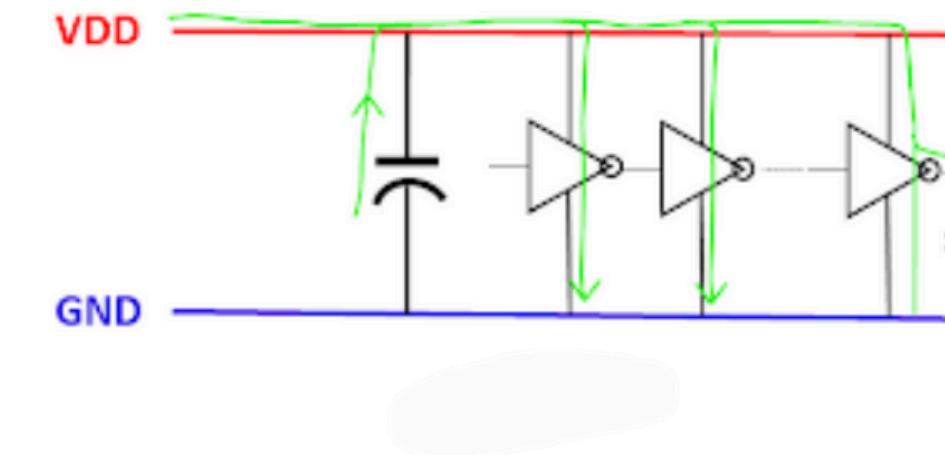
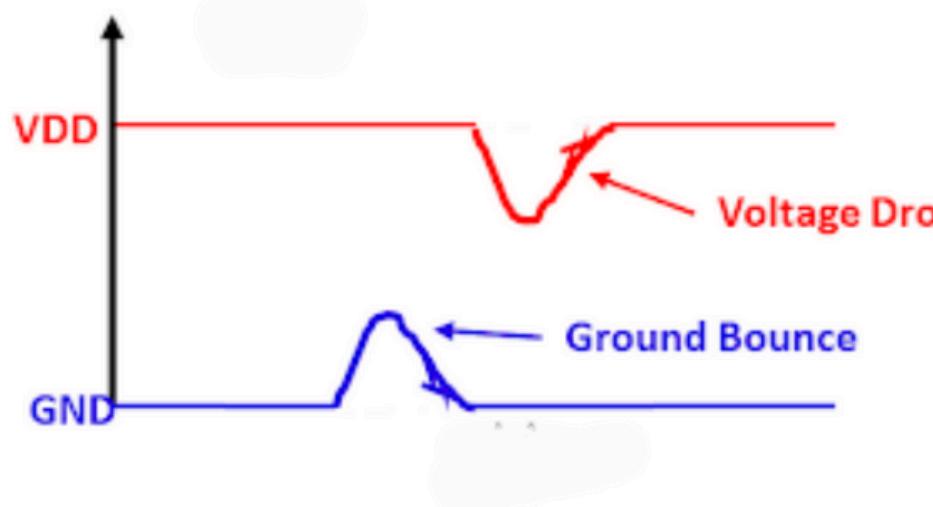
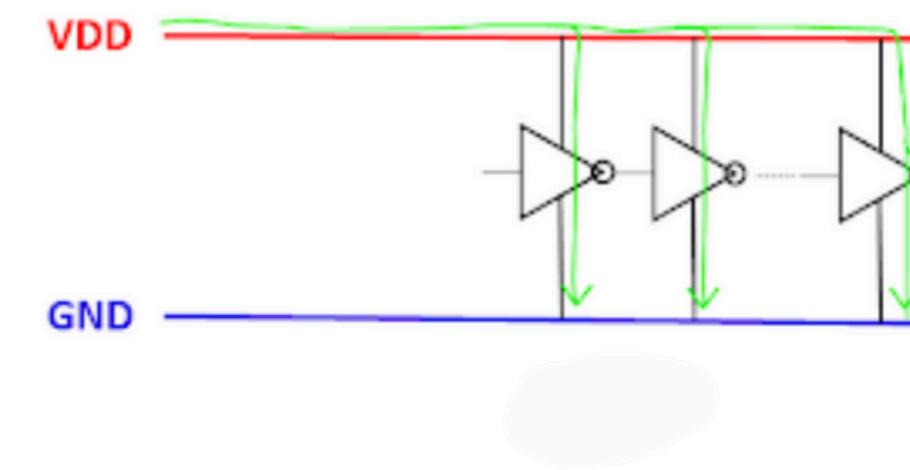
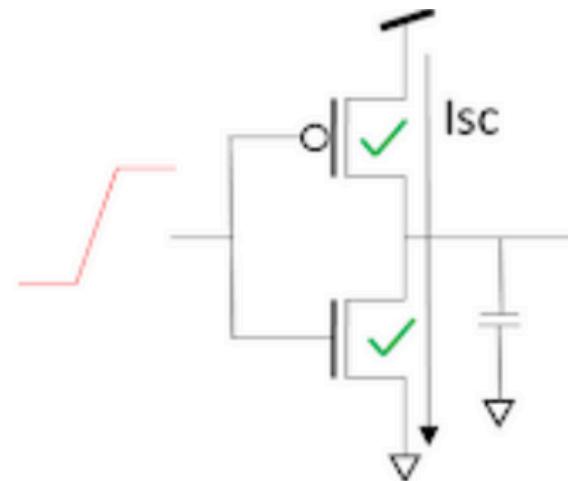


- **Halo** is an additional space around the macro to facilitate routing and prevent congestion
- **Hard Blockages**: Prevent any routing through the blocked area, ensuring no wires or connections can pass through
- **Soft Blockages**: Allow limited routing, often used to guide the placement and routing tools



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De-Cap cells



DE-COUPLING CAPACITORS
...OROUNDING DEPLACED CELLS

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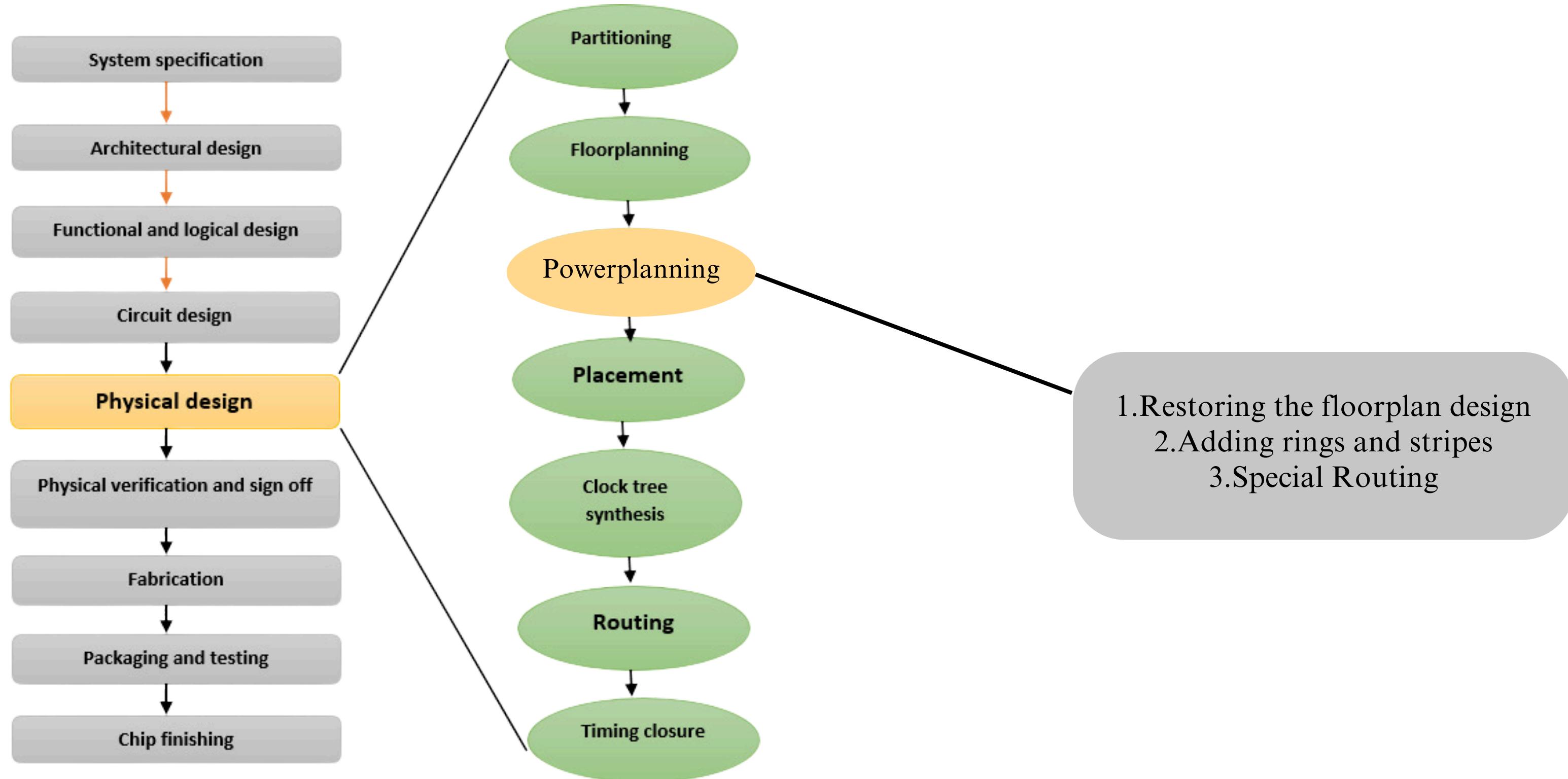
Physical design flow



Powerplanning

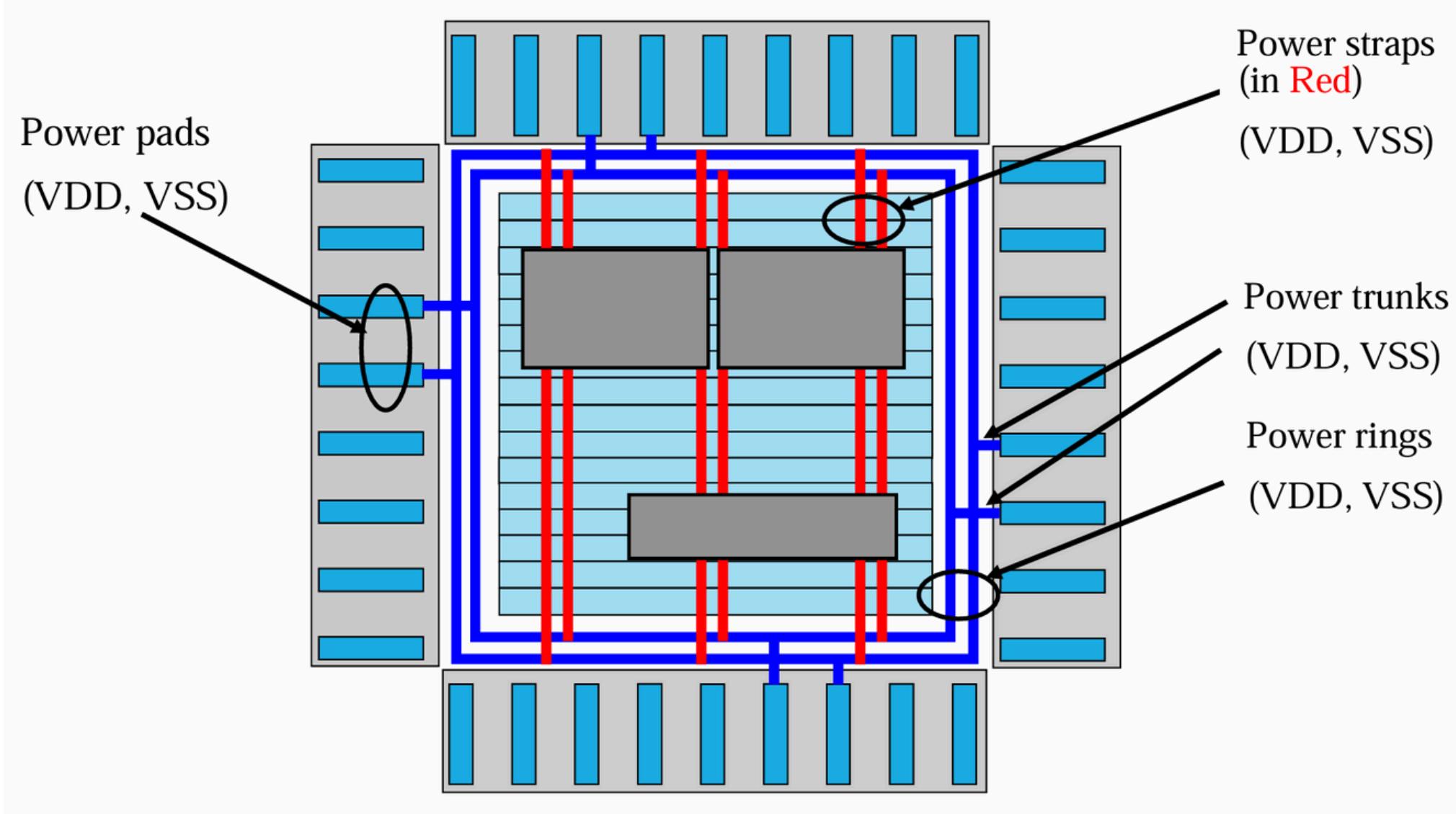
Standard Cell based ASIC Design flow

Physical design flow



Standard Cell based ASIC Design flow

Rings and Straps



Core Power Ring Width =

Total Dynamic Core Current

$\frac{\text{Total Dynamic Core Current}}{2 \times \text{No. of Sides} \times J_{MAX} \text{ of the Metal layer for Ring} \times \text{Current Sources per side}}$

Rings - Circulate power around the chip, ensuring uniform distribution to different sections.

Trunks - Connects rings to pads

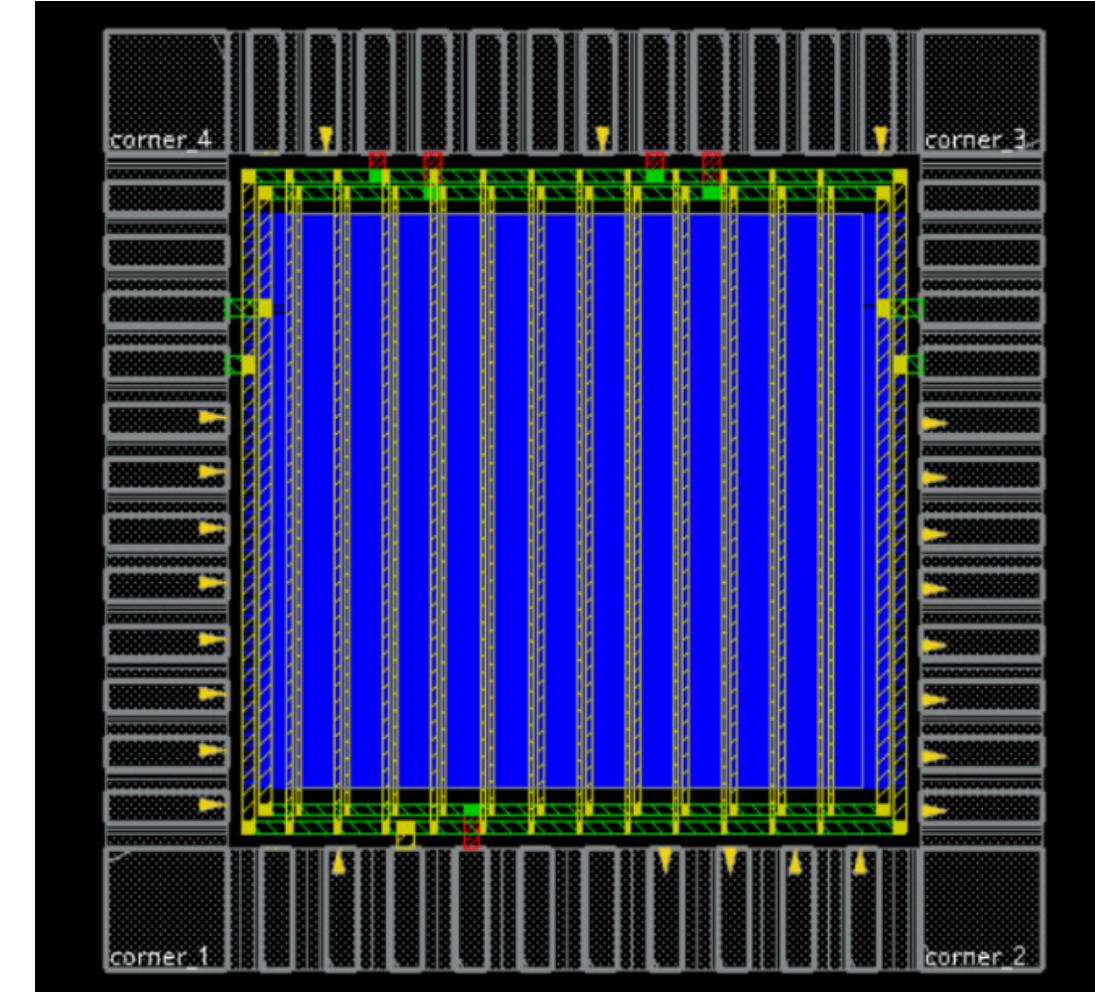
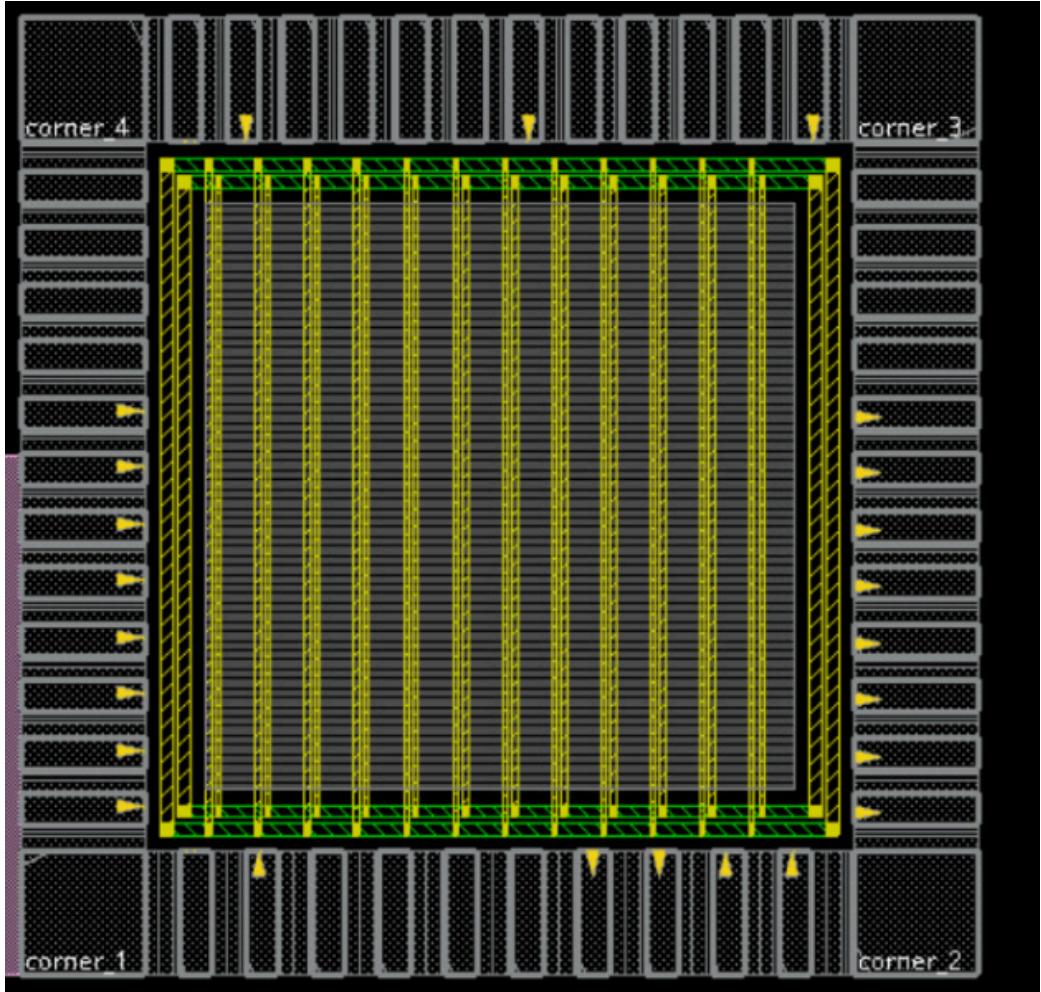
Straps - Carries VDD and VSS from Rings across the chip
Horizontal and vertical metal wires placed in an array across the entire section die

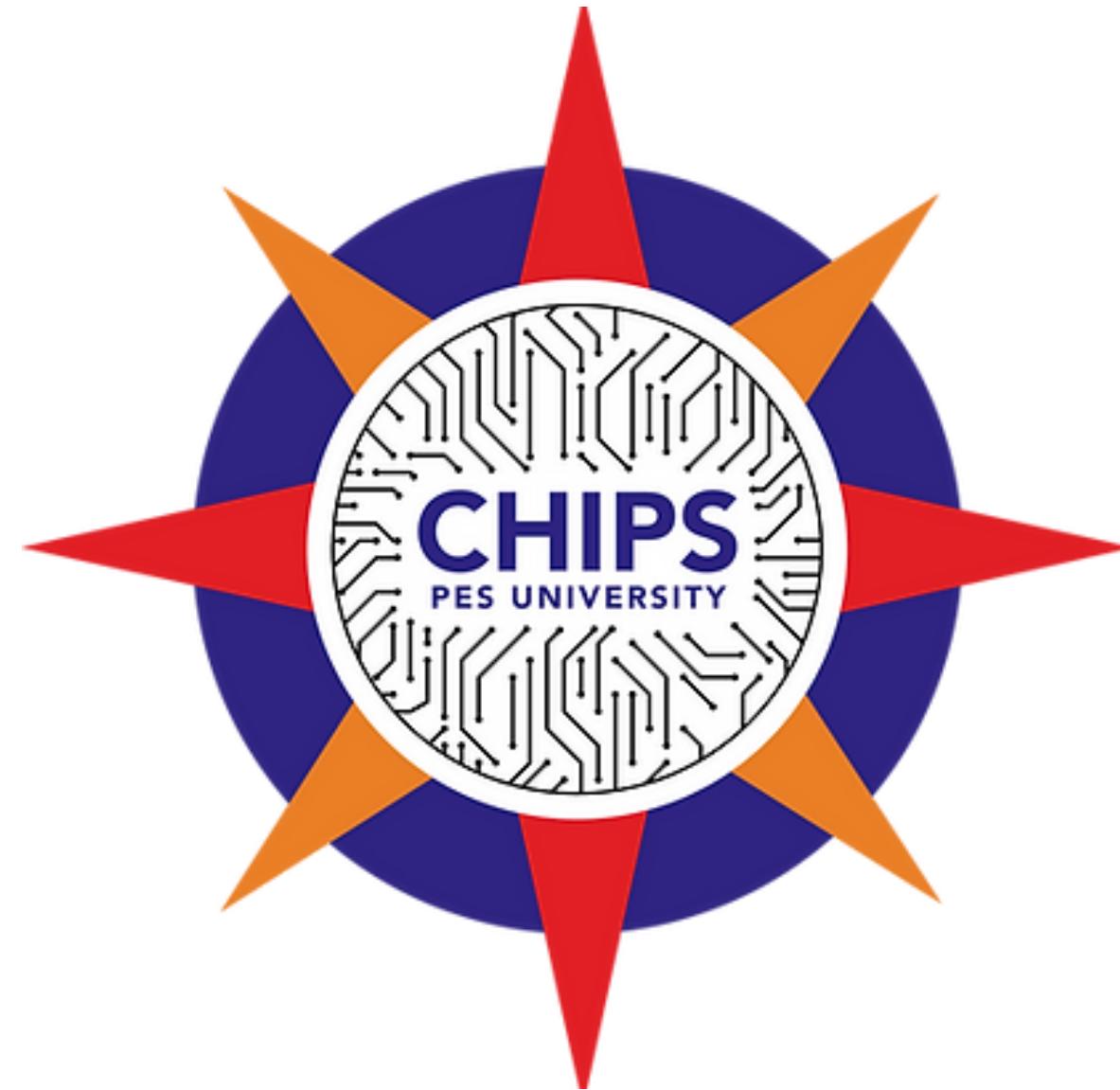
Standard Cell based ASIC Design flow

Sroute



- involves routing power and ground nets, as well as clock nets and other critical signals, before the standard signal routing
- During sroute, these lines are meticulously routed to ensure that every part of the chip can access stable power and ground connections.
- This involves creating wide, low-resistance paths for the power and ground nets and placing vias to connect different metal layers.





Thank You

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