

# Semiconductor Packaging

→ Equipment → around 91% by USA

Materials, Wafer fab, Assembly & packaging → East Asia (57%, 56%, 93%)

Mainly China

→ Nodes → originally referring to transistor gate sizes

↳ Now it indicates improved density, performance & power efficiency

## → OSAT

- Specializes in cutting edge methods

- Economical for high volume needs

- Highly scalable

## → ATMP

- Limited by fab capabilities

- Higher costs due to internal setup

- Limited by inhouse capabilities.

→ Packaging → process of enclosing a semiconductor die within a protective

- package which provides mechanical & environmental protection while enabling electrical connectors b/w chip & external world

- 1. Electrical interface

- 2. Physical & environmental protection

- 3. Heat dissipation

- 4. Customer form factor → enables customers to upgrade to higher performance products quickly using standard sockets.

→ Packaging hierarchy → Level 1 - Single chip modules

Level 2 - Motherboard with assembled IC's

Level 3 - Connects multiple boards

## → Single chip packages

- 1. Pin through hole
- 2. Surface mount technology

## → TO packaging

Metal/ceramic casing → durability

→ thermal dissipation

→ PTH technology

→ Robust mechanical & thermal performance

→ Easy to solder & replace

## → DIP technology

→ 2 parallel rows of pins for through-hole PCB mounting

→ 8-40 pin counts

→ PDIP or CxDIP

→ Simple prototyping & breadboarding

→ Easy manual assembly

1. Standard DIP → plastic body → effective cost-effective

2. Cx DIP → hermetic ceramic casing → military applications

3. Shank DIP → compact variant for space constrained designs

## → PGA (pingrid array) ⇒ Precision packaging

→ Pins arranged in a dense grid for high I/O density

→ CPGA (ceramic) ⇒ for high reliability ⇒ in high end CPUs

→ PPGA (plastic) ⇒ for cost efficiency

→ Superior thermal & electrical performance

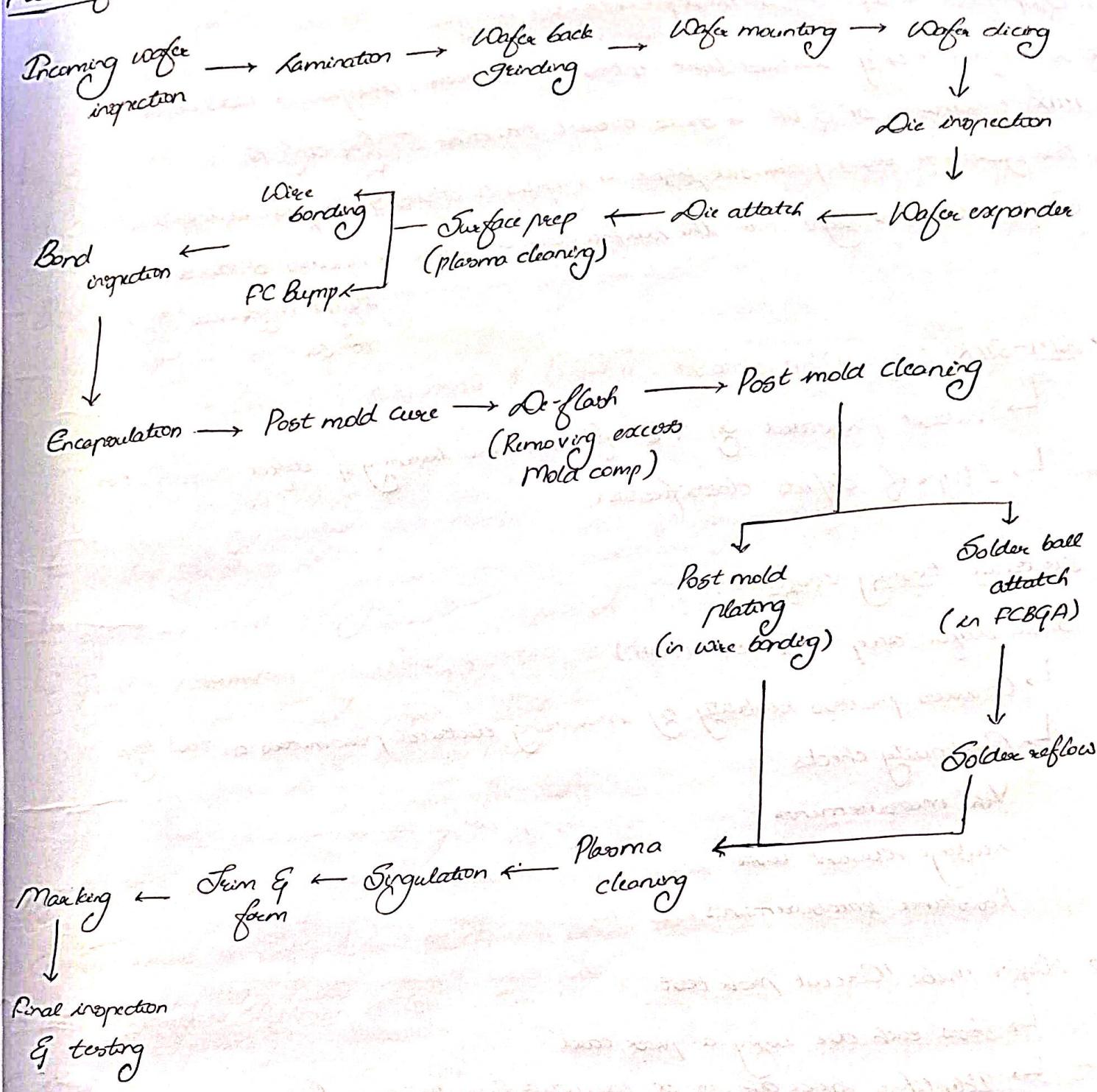
## → BGA ⇒ high density interconnection

→ Reduced signal delay & inductance

→ Higher I/O density & smaller package size

→ Stronger mechanical reliability & reduced risk of lead damage

## Process flow



## → Wafer inspection

- ↳ To ensure quality & prevent defective wafers
- ↳ Incoming quality check →
  1. Documentation review
  2. Moisture sensitivity check
  3. Visual inspection → Macro inspection for scratches & cracks
    - ⇒ Discoloration & contamination check
    - ⇒ Notch / flat orientation confirmation
- ↳ Using high resolution optical / digital microscopes
- ↳ Particle detection & counting

## → Observation methods in microscope

1. Brightfield → light shines straight onto the surface
2. Darkfield → only scattered light enters the camera, background looks dark
3. MIX → combines BF & DF → shows overall structure & fine defects
4. Polarization → uses polarised light → highlights streets & crystal orientation
5. Oblique (OBlique) → light hits the surface from one side → creates shadows, makes height differences easy to see

## → WDM-811K Wafer Map dataset

↳ Dataset provided by TI for machine learning & defect classification.

↳ 8 type of defects classification

## → Electrical testing verification

### 1. Basic wafer acceptance test (WOAT)

↳ Ensures process reliability by measuring electrical parameters on test pads

↳ Continuity checks

Vth measurements

Leakage current tests

Resistance measurements

### 2. Wafer probe / Circuit probe test

↳ Tests each die using a probe card

↳ Identifies bad dies to be excluded from packaging (or mapping)

↳ DC Tests

Functional tests

Speed Boring

ESD screening

a) Pneumatic

b) Electric

## Lamination

- ↳ Wax → using thermoplastic waxes (55-85 °C)
  - ↳ good planarity but cleaning & contamination issues
- ↳ BG Tape → UV curable adhesive tape
  - ↳ easy handling but limited thermal stability

## Back grinding

- ↳ Thinning → makes ultra thin wafers for modern packaging
  - Flexible & less prone to internal stress
  - Lower chance of chipping defects
  - Better heat dissipation
- ↳ Coarse grinding followed by fine grinding & dry polishing
- ↳ Diamond wheel with grit is used for grinding
- ↳ Grinding parameters → 1. Grinding wheel speed  
2. Wafer rotation speed  
3. Grinding depth  
4. Coolant flow rate

## BG Tape release

- 1) Chemical release → using solvent or chemical agent that dissolves the adhesive layer
- 2) Thermal release → Adhesion is lost when exposed to heat of 150-200 °C
- 3) Laser release → Transparent carrier wafer like glass allows laser to pass through & break the adhesive bond at interface
- 4) Mechanical release → Physical peeling is used

## Wafer dicing

- ↳ Process of separation of individual dies from silicon wafer
- ↳ Early method → Slice & break
- ↳ Slurry gang saw → chips are removed en masse
- ↳ 1. Blade dicing → diamond blade
- 2. Ablation dicing → laser
- 3. Stealth dicing → laser modifies the wafer before grading
- 4. Plasma dicing

- 1. Single cut
- 2. Step cut → dual spindle dicing saws are used  
↳ solution for backside chipping
- 3. Bevel cut → V-shaped dicing blade produces a groove on top side, this eliminates sharp corner when dicing
- 4. Chopper cut → No contact b/w dicing blade & workpiece edge. Blade enters the workpiece from the top at a selected position
- 5. Circle cut → To reduce wafer diameter
- 6. ~~Ultrasonic~~ Ultrasound dicing

→ Laser dicing

- Ablation → high energy pulsed laser removes layer by layer material via vapourisation
- used for brittle, ultrathin & low-k wafers
- $N_2/Arc/CO_2$  or liquid cooling system is used to prevent thermal damage & remove byproducts
- Grove → Laser grooving + Blade dicing
  - To reduce chipping & improve die strength
  - laser beam creates a shallow groove along scribe lines & weakens the wafer along cutting line (10-50% of t)
  - Dicing blade then cuts through wafer along pre-grooved lines

→ Stealth dicing → Lamination → Stealth dicing → Grinding → Tape removal

- Creates internal modifications inside the wafer without cutting through the surface.

- Near IR pulsed laser is used

## Die attach (Die bonding/Dismount)

↳ Bonding of semiconductor die to package substrate/leadframe/Interposer

- 1. Provides mechanical support
- 2. Enables heat dissipation
- 3. Facilitates electrical grounding
- A. Prevents die cracking

### Leadframe

- Older technology
- Substrate is metallic
- Enables higher thermal dissipation & high reliability
- Interconnects on perimeter of the package

### Laminate

- Newer technology
- Enables advanced packaging
- Substrate made from laminated layers of metal & organics
- Interconnects usually under the die

## Die attach tooling

1. Poker pin/needle - a thin pin that pushes the die from below by poking the tape
2. Vacuum dome (Pepper dome) - holds the pin steady & turns the tape steadily  
(Vacuum keeps the tape flat & still)
3. Slider - slides sideways under the tape & reels the tape away from die
4. Ejector - Pushes the die up in steps thus reducing stress
5. Alignment stage - A temporary holding place for die before passing to bonding arm
  - Has tiny vacuum that aligns & positions the die
6. Heater blocks - Heated plate under the substrate facilitating better bonding
7. Substrate clampers - Holding tool for substrate to prevent substrate movement
8. Collet adapter - Aligns & positions the collet
9. Collet - Touches the top surface of the die, uses vacuum suction to lift the die

# Die bonding

## Solder - based

1. Soft - solder
2. Silver sintering
3. Eutectic
4. Thermocompression

## Adhesive - based

1. Epoxy die attach
2. DAP
3. Glass frit
4. Flipchip

→ Soft solder  $\Rightarrow$  1. Clean the die (plasma/chemical etching)  
2. Ni/Au/Ni layer is deposited to enhance solder wettability  
3. Solder applicator  
4. Die placement  
5. Reflow under controlled atmosphere  
6. Cooling & solidification  
7. Post processing to remove flux residues

→ Eutectic  $\Rightarrow$  1. Leadframe is coated with silver  
2. Backside of Si is coated with gold  
3. At eutectic temp, Au-Si liquid spreads over the leadframe  
4. On cooling, it solidifies to form a strong metallic joint

→ Silver sintering  $\Rightarrow$  Advanced bonding method using  $\mu\text{g}$  nanosized Ag particles to create high strength, highly thermally conductive bond between semicond. & substrate

→ Thermocompression  $\Rightarrow$  Solid state bonding process

- ↳ Heat & pressure applied together
- ↳ Creates strong intermetallic/diffusion bonds
- ↳ Gold-Gold are brought into atomic contact leading to
  - a) Surface diffusion
  - b) Grain boundary diffusion
  - c) Bulk diffusion
- ↳ Used in CMOS to enable vertically integrated devices

→ Groxy die attach → uses epoxy based adhesive to form strong mechanical & thermal connector

→ 1. Electrically conductive (has silver)

2. Non conductive epoxy (when insulation is reqd)

3. Thermally conductive (has boron nitride or aluminium oxide)

→ Epoxy is dispensed by stamping or screen printing

→ DAF → pre cut adhesive film

↳ offers precise thickness control, clean application & minimal void formation

↳ ideal for high density

→ 1. Thermosetting DAF → heat curable

2. UV activated DAF

3. Pressure sensitive DAF → under mechanical pressure

→ Glass frit bonding

↳ Using low melting glass material to mechanically bond a die to substrate or another wafer

↳ Eliminates the need for polymer encapsulation by providing hermetic sealing

↳ Glass powder + organic binders & solvents → Bonding at elevated temperature

→ Wire bonding

1. Thermo compression → controlled heat, pressure & time. Cu/Au/Al are commonly used

2. Ultrasonic → Ultrasonic with pressure & vibration

3. Thermosonic → for ball to ball wire bonding

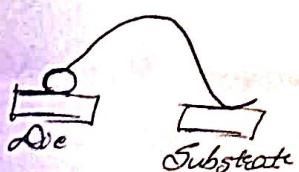
↓  
high diffusion rates

→ Ultrasonic wedge to wedge → Bonding angle of 30 to 60°

→ wedge tool flattens the wire & generates a weld

ball to wedge → Edge of capillary is used to form the ball bond

↓  
made at silicon chip



## → Flip chip bonding

- Controlled collapse chip connection (C4)
  - Solder bumps are deposited on the chip pads on top side of the wafer and then its flipped over
  - Reduces packaging size & improves electrical & thermal performance
  - Low signal inductance
- Under bump metallization

a) Printing ⇒ a metal paste (Ag/Cu based) is screen printed on the pad

- Additive, mask based process

b) Plating ⇒ Thin seed layers (Ti/Cu or Cr/Cu) are deposited by PVD

- PR defines UBM areas
- UBM metals are electroplated & then PR is removed
- Lithography based ⇒ highly controlled
- High uniformity

→ Encapsulation ⇒

1. Physical protection
2. Environmental protection
3. Heat dissipation
4. Signal integrity
5. Marking

→ Transfer molding ⇒ Transferring preheated molding compound into the mold cavity

- provides mechanical support, environmental protection & electrical insulation.

- ↳ Risk of wire sweep
- ↳ Internal voids & delamination can occur
- ↳ Limited flexibility for custom shapes

- 1. Semiconductor devices are positioned in mold cavities
- 2. B-staged epoxy mold compound pellet is heated (165-185°C)
- 3. EMC pellet softens & turns into a low viscosity liquid
- 4. On application of pressure, the liquid compound flows through runners & gates filling multiple mold cavities simultaneously
- 5. Heated mold initiates curing of EMC
- 6. Once material reaches its gel point, and complete curing occurs during post mold bake

### → Compression molding

- ↳ Uses direct pressure to shape the encapsulant around IC components
  - ↳ Low stress on wire bonds
  - Suitable for fine-pitch & large area IC's
- 1. Semiconductor wafers are placed inside the mold cavity
  - 2. EMC is in form of pellet or sheet & is preheated
  - 3. Pre heated mold closes & EMC is placed onto the substrate
  - 4. Compression pressure is applied to distribute mold compound evenly
  - 5. Mold remains closed at high temperature for set time to cure
  - 6. Encapsulated IC's are removed, followed by post mold bake

### → Encapsulation materials

- Phenol novolac or Cetol novolac
- 1. EMC → epoxy resin, silica filler, curing agents, catalysts → Phenonium/Pimidazoles
  - ↳ High mechanical strength & thermal cond.
  - Excellent adhesion & chemical resistance
- 2. Silicone encapsulants → Polysiloxane based
  - ↳ for high performance applications
  - ↳ Superior flexibility
- 3. Polyimide encapsulants → aromatic polyimide resins
  - ↳ High temperature applications
- 4. Acrylic encapsulants → acrylic polymers
  - ↳ UV & moisture protection with fast curing properties

→ Different methods/types of encapsulation

1. Mop type molding
2. Preindustrial type
3. Potting
4. Dam and fill
5. Glob top encapsulation → Direct encapsulation

→ TO-can package

- 1. TO-can (with chip which is wire bonded and lid placed) is placed inside the sealing chamber
2. Vacuum condition is brought in & then filled with  $N_2$  and  $Ar$
  3. Metal lid is welded to the TO-can
  4. Package is now hermetically sealed (later the leak testing is performed)

→ Post mold cure

↳ To complete the polymer crosslinking of the epoxy resin

↳ Stabilizes thermomechanical properties

→ Deflashing → removal of excess molding compound from the package surface

↳ Ensures clean & accurate dimensions

Techniques → 1. Dry blasting → Ice blasting - using solid  $CO_2$  pellets at very low temp

- Pellets hit the flash, cracking & breaking it off

-  $CO_2$  later sublimates

→ Sand blasting - Uses hard particles like silica or glass beads

- Effective for thick flash

2. High pressure water jet → removes coating via delamination

3. Chemical deflashing - using chemical solvents like  $N$ -methyl- $\alpha$ -pyrrolidone

4. Wet blasting - Water with abrasives like  $Al_2O_3$  or glass beads

↳ Smoother surface finish

- PC lead plating → surface treatment where thin layer of metal is coated onto IC leads
  - ↳ Improves solderability
  - ↳ Prevents oxidation & corrosion
  
- Singulation → separates the multiple semiconductor devices in single molded package into individual units.
  - ↳ 1. Mechanical sawing
  - 2. Laser cutting
  - 3. Punching
  
- Trim and form
  - ↳ Trim ⇒ Removes dam bar to electrically isolate leads
  - Form ⇒ Shapes leads as per requirement
    - a) Straight leads
    - b) T-leads
    - c) Gull wing leads
  
- Marking → Standard information is printed on the IC
  - LM358AN → LM → Family: Linear Monolithic
  - 358 → Model number
  - A → Variant
  - N → Dual inline package
  
- ATmega 328 PPU → P → Low power variant
- PPU → PDIP package
  
- 8 digit code → YYWW
- Methods → 1. Laser marking (Fiber / CO<sub>2</sub> / UV laser)
- 2. Ink or pad printing
- 3. Hot stamping / Transfer printing