Low Power VLSI

Project Title: SP- Type TSPC Latch

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Introduction

The True Single-Phase Clocking (TSPC) latch, a fundamental CMOS circuit element in digital logic design, offers high-speed performance with simple clock generation and distribution. TSPC latches provide efficient temporary data storage by capturing and holding digital values until overwritten. They synchronize different parts of a circuit, ensuring accurate timing and reliable operation. TSPC latches feature a small number of clocked transistors, enhancing their speed and efficiency in digital systems.

There are two types of TSPC latches

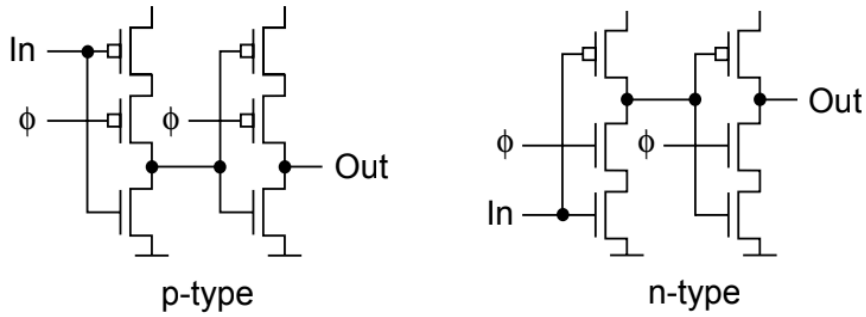
1. Precharged TSPC Latches (PN and PP type)
2. Non-precharged TSPC latches (SP and SN type)

Feature	Non-Precharge TSPC Latch	Precharge TSPC Latch
Data Capture Mechanism	Direct from data input (D)	Precharge followed by data overwrite
Race Condition Susceptibility	High	Low
Design Complexity	Lower	Higher
Power Consumption	Potentially lower	Slightly higher
Speed	Potentially slower	Potentially faster

Non-Precharged TSPC latch

A TSPC non-precharged latch is a variation of the TSPC latch design used in digital circuitry. Unlike traditional TSPC latches, which use precharge and evaluate phases to achieve storage and transfer operations, TSPC non-precharged latches do not have a precharge phase.

- The latch directly captures and holds the input data during the clock's active phase without the need for precharging the internal nodes.
- This design simplifies the latch structure and can lead to reduced power consumption and improved speed, particularly in high-frequency applications.
- However, TSPC non-precharged latches may have limitations in terms of robustness and noise immunity compared to their precharged counterparts.



SP type latch

The latch relies on the clock signal and the data input (D) to capture and hold a data value. Here's a step-by-step explanation:

- Clock Low (CLK = 0):
    - During the low phase of the clock signal, a path is created between the data input (D) and the latch output (Q) using transmission gates formed by NMOS and PMOS transistors controlled by the clock signal.
    - The current state of the data input (D) is directly passed through this open path and reflected on the latch output (Q).

- Clock High (CLK = 1):
    - When the clock signal goes high, the transmission gates controlled by the clock become inactive, effectively closing the path between the data input (D) and the latch output (Q).
    - The latch now enters a hold state, where it retains the value that was present at the output (Q) just before the clock went low. This captured value remains stable until the next clock cycle.

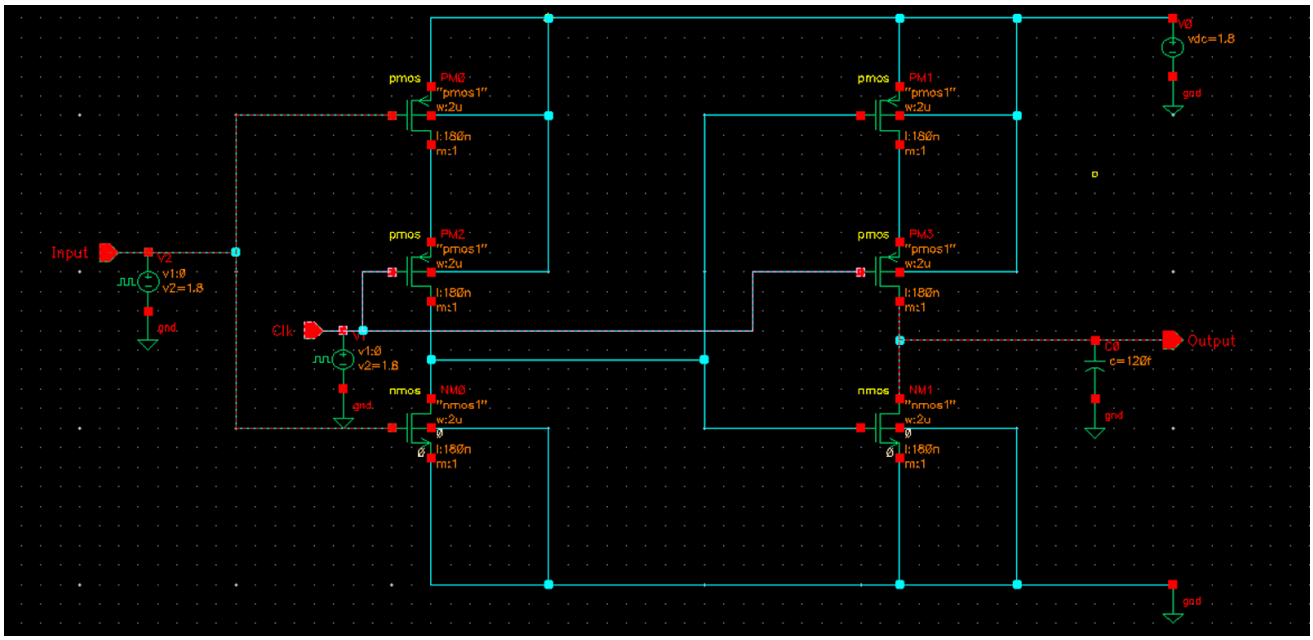


Fig 1: Schematic of SP type TSPC latch with VDD as 1.8V and a load of 120f F

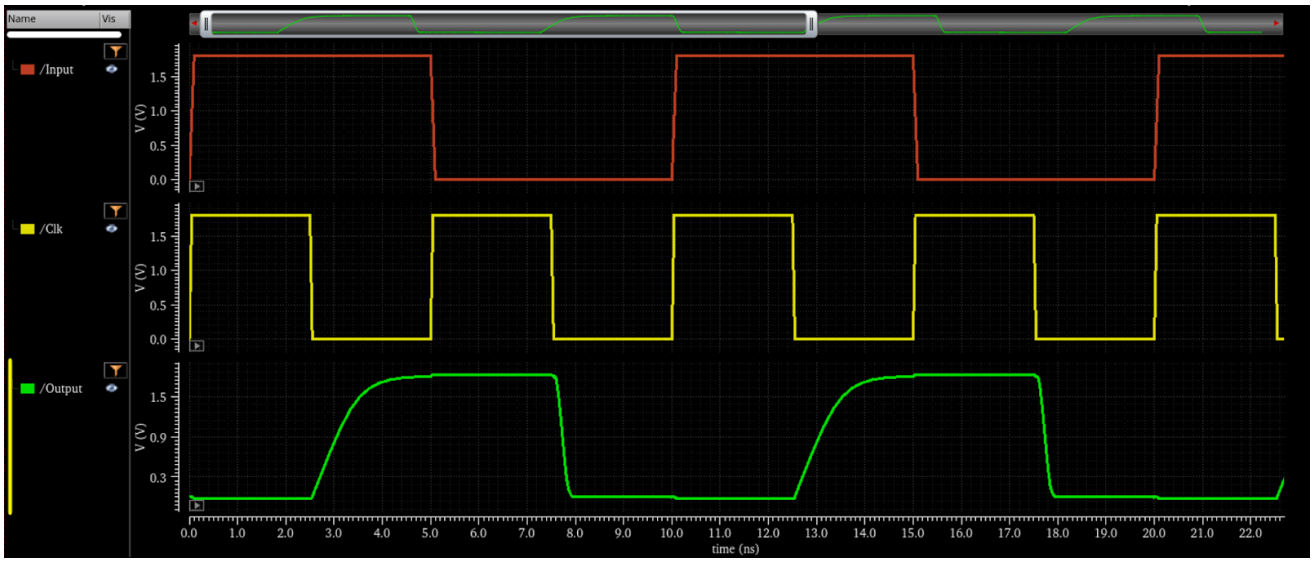


Fig2: VIVA-XL plot for SP TSPC latch Here it can be seen that output follows the input whenever the clock is 0. If clock is 1, it holds the previous value

Power Analysis

D-Latch with the requirement of both clock and its complementary

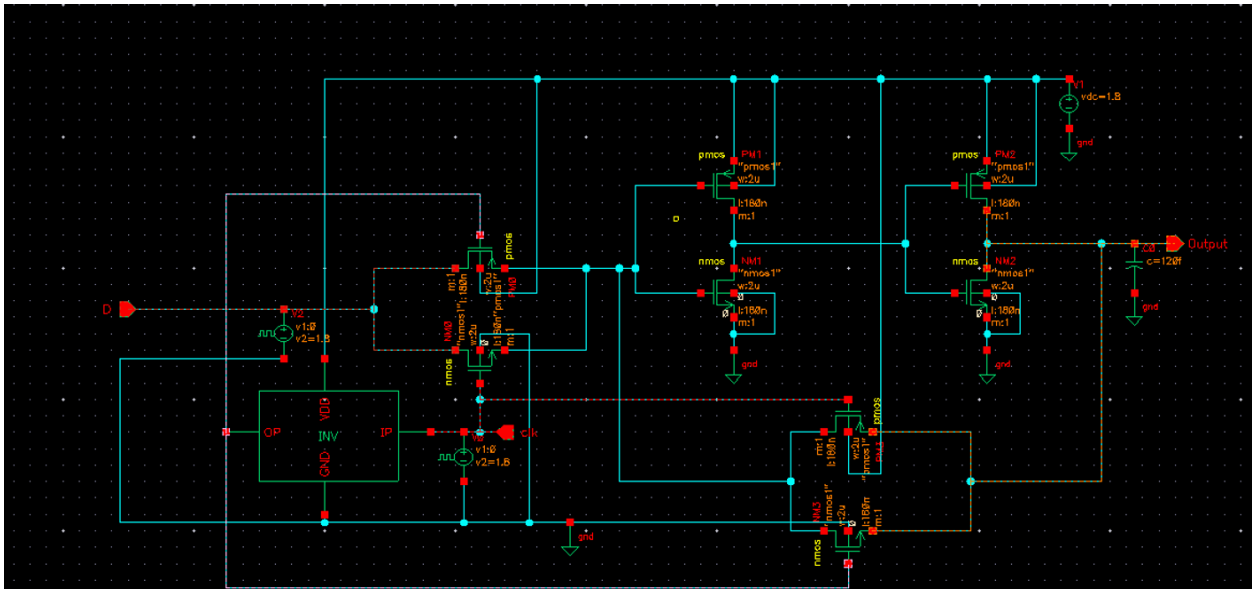


Fig3: Schematic of Traditional D-latch with Vdd as 1.8V and a load of 120f F

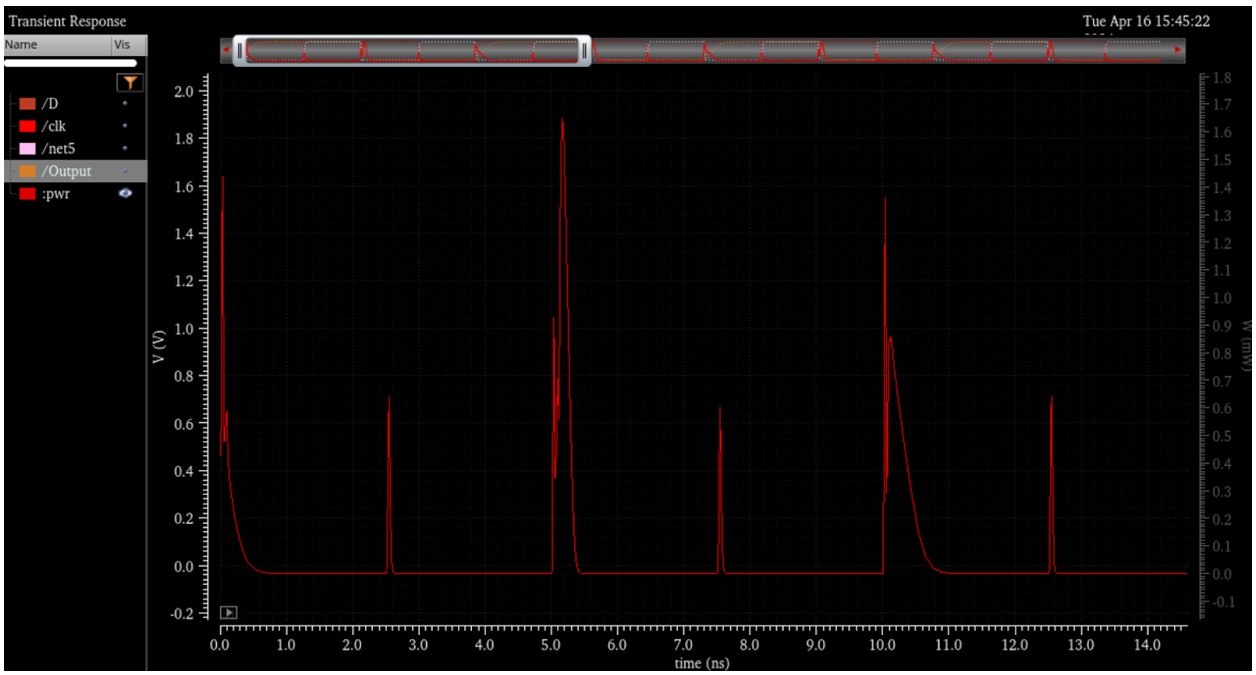


Fig4: Power graph for Traditional D-latch A spike in the graph can be observed when the transistors are on. When all the transistors are on, a high peak in the graph at around 5.2ns can be observed.

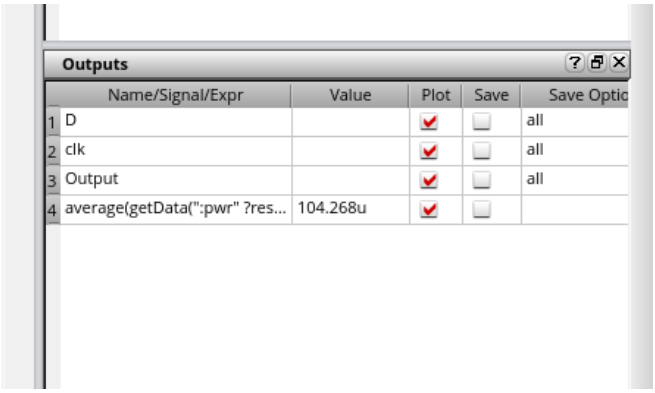


Fig 5: Average power consumption for D-latch, with a load of 120f F

SP-type TSPC latch

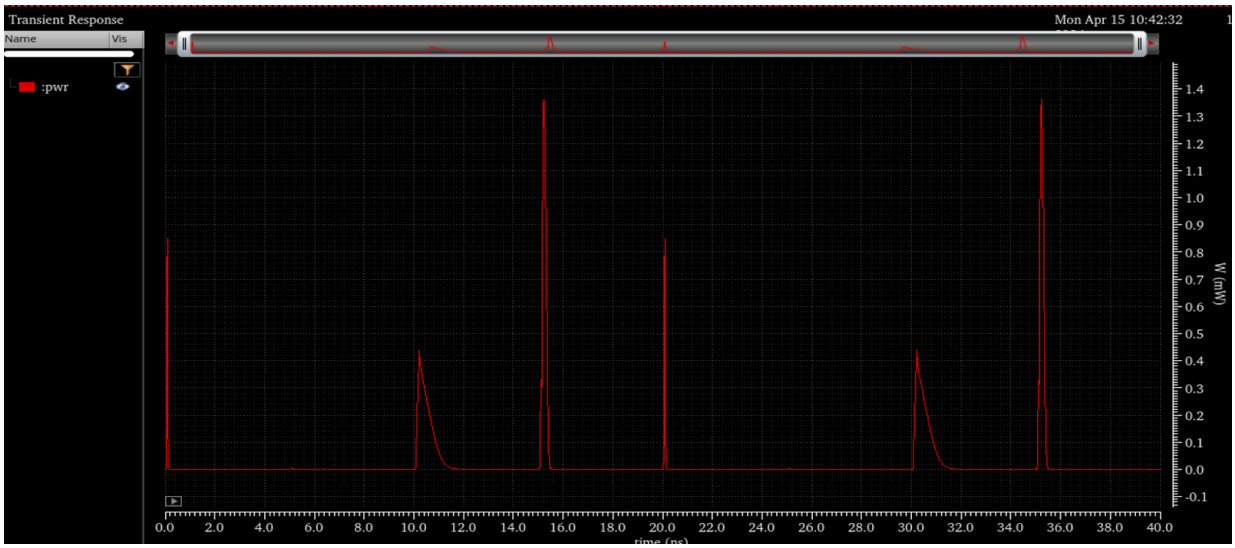


Fig6: Power graph for Non-precharged TSPC latch of P-type

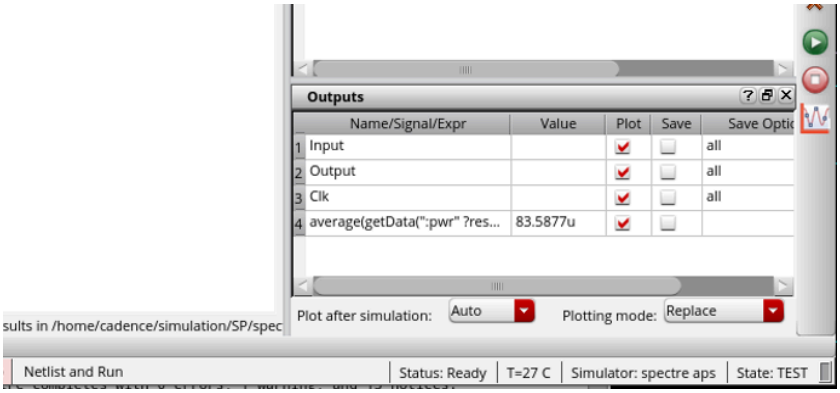


Fig7: Average power consumption for SP latch with a load of 120f F

Conclusion

Traditional D-latches consume an average of 104 microwatts of power. In contrast, TSPC SP-type latches significantly reduce this consumption to just 83 microwatts. This impressive power saving of nearly half (19%) is achieved by eliminating the reliance on a complementary clock signal in the TSPC SP-type latch design.