2020

Full Marks : 70

Time : 3 hours

The figures in the right-hand margin indicate marks

Answer from **all** the Parts as directed

Part—A

(Objective Type Questions)

1. Choose the correct answer in each of the following : 5×1

(a) In digital circuits, shift register circuits is a cascade of

(i) flip-flop (ii) memory

(iii) SP (iv) None of these

(b) Demultiplexer is also known as

(i) Demux

(ii) A/D converter

(iii) Multiple

(iv) None of these

(c) Half-adder first adds

(i) two bits (ii) three bits

(iii) four bits (iv) None of these

(d) Which is the microprocessor (μP) comprises?

(i) Register Section

(ii) ALU

(iii) Control Unit

(iv) All of these

(e) Associative Memory is also known as

(i) Associative Storage

(ii) Neural Network

(iii) Cache Memory

(iv) None of these

2. Fill in the blanks : 5×1

(a) INTR : it implies the ——— signal.

(b) In Register org. PC stands for ———.

(c) DMA stands for ———.

(d) Encoder is reverse form of ———.

(e) The size of each sequents in 8086 is ———.

(Continued)

Part—B

(Short Answer Type Questions)

3. Answer *any four* questions of the following : 4×5

(a) What is instruction cycle? Explain the types of instruction cycle.

(b) Explain the microprogrammed control with diagram.

(c) Differentiate between half-adder and full-adder.

(d) What is mapping? Explain the types of mapping in CSA.

(e) Differentiate between real mode and protected mode.

(f) Write short notes on *any two* of the following :

(i) Addressing modes

(ii) Associative memory

(iii) Ports

(iv) Pipelining

(v) Parallel processing.

(Turn Over)

Part—C

(Long Answer Type Questions)

4. Answer *any four* questions of the following : 4×10

(a) What is Bus System? Explain the Bus Architecture and Organisation with diagram.

(b) What is Register? Describe the Register Organisation with diagram.

(c) Differentiate between ISA and EISA Bus Architecture.

(d) Explain the Architecture and Organisation of 8086 microprocessors (μP).

(e) Differentiate between DX and SX of different microprocessor (μP).

(f) Write short notes on *any three* of the following :

(i) DMA controller

(ii) Parallel processing

(iii) Instruction set

(iv) Cache memory

(v) Core if

(vi) Clock pulse generator.

***