











Board Stack Report

Design Rules Verification ReportFilename : C:\Users\Public\Documents\Altium\Projects\CAN_Dongle\CAN_dongle_V3.Pcb

Warnings 0 Rule Violations 0

Warnings Total 0

Rule Violations	
Clearance Constraint (Gap=7mil) (All),(All)	0
Short-Circuit Constraint (Allowed=No) (All),(All)	0
Un-Routed Net Constraint ((All))	0
Modified Polygon (Allow modified: No), (Allow shelved: No)	0
Width Constraint (Min=10mil) (Max=50mil) (Preferred=12mil) (All)	0
Power Plane Connect Rule(Relief Connect)(Expansion=20mil) (Conductor Width=10mil) (Air Gap=10mil) (Entries=4)	0
Hole Size Constraint (Min=7.87mil) (Max=248mil) (All)	0
Hole To Hole Clearance (Gap=10mil) (All),(All)	0
Minimum Solder Mask Sliver (Gap=0mil) (All),(All)	0
Silk To Solder Mask (Clearance=8mil) (Disabled),(All)	0
Silk to Silk (Clearance=0mil) (AII),(AII)	0
Net Antennae (Tolerance=0mil) (All)	0
Height Constraint (Min=0mil) (Max=1000mil) (Prefered=500mil) (All)	0
Total	0