BRAC UNIVERSITY DEPT. OF COMPUTER SCIENCE AND ENGINEERING COURSE NO.: CSE250

Circuits and Electronics Laboratory

Experiment No. 4 (SIMULATION)

Name of the Experiment: Verification of Thevenin's Theorem and Maximum Power Transfer Theorem.

Part 1

OBJECTIVE:

To verify Thevenin's theorem with reference to a given circuit theoretically as well as experimentally.

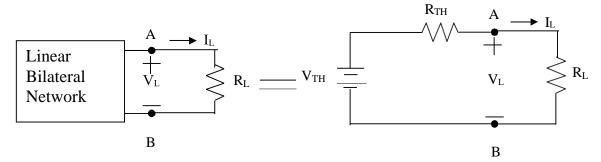
INTRODUCTION:

It is often desirable in circuit analysis to study the effect of changing a particular branch element while all other branches and all the sources in the circuit remain unchanged. Thevenin's theorem is a technique to this end, and it reduces greatly the number of computations which we have to do each time a change is made. Using Thevenin's theorem the given circuit excepting the particular branch to be studied is reduced to the simplest equivalent circuit possible and then the branch to be changed is connected across the equivalent circuit.

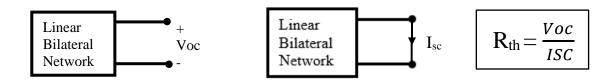
Thevenin's theorem states that any two-terminal linear bilateral networks containing sources and passive elements can be replaced by an equivalent circuit consisting of a voltage source (Vth) in series with a resistor (Rth) where,

Vth = The open circuit voltage (VOC) at the two terminals A & B.

Rth = The resistance looking into terminals A and B of the network with all sources removed.



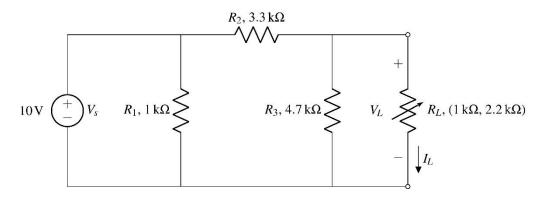
There are several methods for determining Thevenin resistance R_{TH} . An attractive method for determining R_{TH} is: (1) determine the open circuit voltage, and (2) determine the short circuit current I_{SC} as shown in the figure; then



PROCEDURE:

For Original Circuit:

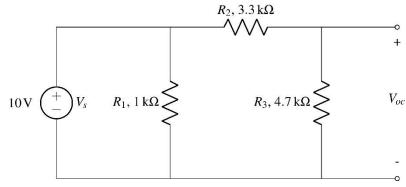
- Arrange the original circuit as shown in the figure. Apply 10V dc from dc power supply.
- \blacktriangleright Measure V_L , I_L for three values of RL & record the data in the table.



Circuit 1: Original Circuit

FINDING V_{Th} & R_{TH}:

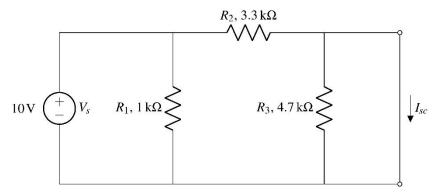
➤ Remove the load resistance RL and find the open circuit voltage between terminals A & B. This voltage is Thevenin voltage i.e., VTH=VOC.



Circuit 2: Circuit for finding V_{OC}

➤ Place a short circuit between terminals A & B and find the short circuit current ISC. Divide the open circuit voltage by short circuit current to find the Thevenin resistance, i. e.

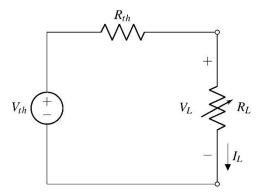
$$R_{th} = \frac{Voc}{Isc}$$



Circuit 3: Circuit for finding I_{SC}

For Thevenin Equivalent Circuit:

 \triangleright Construct Thevenin's equivalent circuit as shown in figure 4 setting the power supply at V_{TH} volts and the rheostat at R_{TH} ohms. Now measure the load current I_L and the load voltage V_L for the values of R_L determined in step 2. Compare these values with previous values.

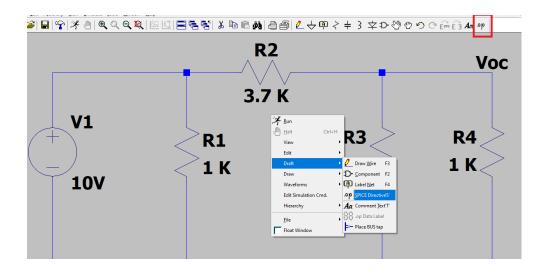


Circuit 4: Thevenin equivalent circuit

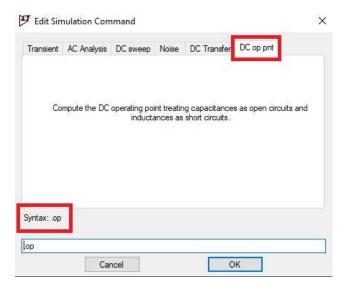
CIRCUIT SIMULATION USING LTSPICE:

- 1. Draw the circuit shown in Circuit.1 in a new schematic in LTspice. Modify the components with their values and name the nodes. To name the nodes, *Right-click on the wire/node* \rightarrow *Label Net*. **Do not forget to add a ground to the circuit.** Here, $R_L = 1 \text{ K}\Omega$.
- 2. To measure the node voltages and branch currents we have to do 'DC operating point' analysis.

To run the 'DC operating point' analysis we have to write the analysis command. Find the 'Spice Directives' option by Right-clicking on the schematic \rightarrow Draft \rightarrow Spice Directives or find it from the toolbar above.



3. After clicking the 'Spice Directives', the 'Edit Text on the Schematic' window will appear. Now Right-click on the blank space on this window → Select 'Help me Edit' → Analysis Command. A window titled 'Edit Simulation Command' will appear. Select 'DC op pnt' → OK. It will generate a '.op' command which is the command for DC operating point analysis. Place this command somewhere in the schematic.



[Notice the '.op' syntax for DC operating point analysis. You could just write the command in the command editor box and place that command in the schematic.]

4. To run the simulation, click 'Run'. Find the 'Run' button from the above toolbar or by just Right-clicking on the schematic.

5. After clicking 'Run' a new window titled 'Operating Point' will appear containing all node voltages and branch currents. From this window note down the required values. For this circuit, these are the V_L and I_L which is the current through the resistance R_4 .

Operating Point			
V(n001):	10	voltage	
V(vl):	1.82241	voltage	
I(R4):	1.82241	device current	
I(R3):	0.387747	device_current	
I(R2):	2.21016	device current	
I(R1):	10	device current	
I(V1):	-12.2102	device current	

- 6. For V_{TH} draw and simulate the circuit in Circuit. 2 and measure Voc. (Follow instructions 1-5).
- 7. For \mathbf{R}_{TH} draw and simulate the circuit in Circuit. 3 and measure \mathbf{I}_{SC} . (Follow instructions 1-5). Calculate $\mathbf{R}_{TH} = \mathbf{Voc} / \mathbf{I}_{SC}$.
- 8. Draw and simulate the circuit in Fig. 4 and measure V_L and I_L . (Follow instructions 1-5). Compare these values to the previously measured V_L and I_L for the circuit in Fig. 1.

Save the Schematic by *clicking File* → *Save as* → '*Name.asc*' for future use.

REPORT:

- 1. Find theoretically the Thevenin equivalent circuit for the values of R_1 , R_2 , R_3 & V_S recorded in the table. Also find I_L , and V_L .
- 2. Show the results in tabular form.
- 3. Comment on the results obtained and discrepancies (if any).

QUESTION:

1. Mention the advantages of using the Thevenin Theorem.

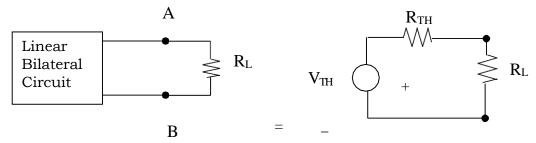
Part 2

OBJECTIVE:

The objective of this experiment is to verify the maximum power transfer theorem.

THEORY:

The maximum power transfer theorem states that a resistive load will receive maximum power when its total resistive value is exactly equal to Thevenin's resistance of the network as "seen" by the load.



We know that any circuit A terminated with a load R_L can be reduced to its Thevenin's equivalent. Now according to this theorem, the load R_L will receive maximum power when R_L = R_{TH}

The efficiency of power transfer is defined as the ratio of the power delivered to the load P_{OUT} , to the power supplied by the source P_{IN} .

$$\% \eta = \frac{P_{OUT}}{P_{IN}} \times 100 = \frac{V_L}{V_{TH}} \times 100 = \frac{R_L}{R_L + R_{TH}} \times 100$$

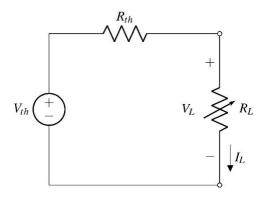
The voltage regulation is defined as,

% VR =
$$\frac{\text{Load voltage at no load} - \text{Load voltage at full load}}{\text{Load voltage at full load}} \times 100$$
$$= \frac{R_{TH}}{R_{L}} \times 100$$

At maximum power transfer condition, $\eta = 50 \% \& VR = 100 \%$.

A relatively low efficiency of 50 % can be tolerated in situations where power levels are relatively low such as in electronic & communications circuits for transmission & reception of signal where the Engineer's goal is to receive or transmit maximum amount of power.

However, when large power levels are involved, such as at generating stations, efficiencies of 50 % would not be acceptable. The goal here is high efficiency and not maximum power. Power utility systems are designed to transmit the power to the load with the greatest efficiency by reducing the losses on the power lines. Thus, the effort is concentrated on reducing RTH, which would represent the resistance of the source plus the line resistance.



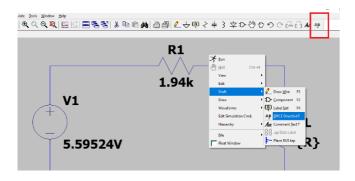
Circuit 5: Circuit for maximum power transfer theorem verification

CIRCUIT SIMULATION USING LTSPICE:

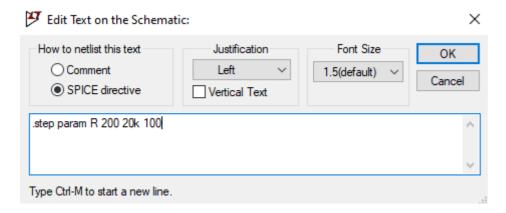
1. Draw the circuit shown in Circuit. 5 in a new schematic in LTspice. Modify the components with their values and name the nodes. Notice that, the value of the voltage source is equal to V_{TH} and that of the resistance is equal to R_{TH} To name the nodes, *Right-click on the wire/node* → *Label Net*. Do not forget to add a ground to the circuit.

As we have to calculate the power at load resistance \mathbf{R}_{L} for different values of \mathbf{R}_{L} , we will vary the value of \mathbf{R}_{L} . For this, assign the value of \mathbf{R}_{L} with $\{\mathbf{R}\}$ so that \mathbf{R} can be used as a variable parameter.

2. Find the 'Spice Directives' option by Right-clicking on the schematic \rightarrow Draft \rightarrow Spice Directives or find it from the toolbar above.



3. After clicking the 'Spice Directives', the 'Edit Text on the Schematic' window will appear. To calculate the power associated with the load RL for different values of RL, we have to vary the value of RL. Type '.step param R 200 20k 100' in the text box and click OK. It will generate a command. Place it somewhere in the schematic.

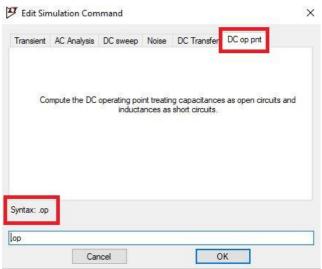


Notice the **'.step'** syntax here. This command causes an analysis to be repeatedly performed while stepping the temperature, a model parameter, a global parameter, or an independent source. Steps may be linear, logarithmic, or specified as a list of values. Here, **'.step param R 200 20k 100'** this command causes the parameter R to increase from **200** Ω to **20** Ω with a step size **100** i.e. it will perform simulation for $RL = 200 \Omega$, $(200+100) \Omega$, $(200+2*100) \Omega$ up to **20** K Ω .

4. To calculate the power at the load we will measure the voltage and current at the load ($P_L = V_L * I_L$). To do so we have to do 'DC operating point' analysis.

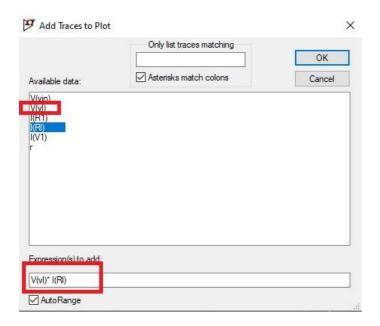
To run the 'DC operating point' analysis we have to write the analysis command. Find the 'Spice Directives' option by Right-clicking on the schematic \rightarrow Draft \rightarrow Spice Directives or find it from the toolbar above.

5. After clicking the 'Spice Directives', the 'Edit Text on the Schematic' window will appear. Now Right-click on the blank space on this window → Select 'Help me Edit' → Analysis Command. A window titled 'Edit Simulation Command' will appear. Select 'DC op pnt' → OK. It will generate a '.op' command which is the command for DC operating point analysis. Place this command somewhere in the schematic.

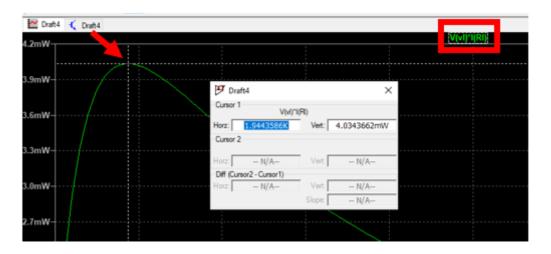


[Notice the '.op' syntax for DC operating point analysis. You could just write the command in the command editor box and place that command in the schematic.]

- 6. To run the simulation, click 'Run'. Find the 'Run' button from the above toolbar or by just Right-clicking on the schematic.
- 7. After the simulation 'run' is complete a blank plot window will appear. Now Right-click on the blank plot space \rightarrow Add trace \rightarrow Select $V_L \rightarrow$ Type '*' \rightarrow Select $I(R_L) \rightarrow OK$.



8. A power vs resistance plot will be generated. Here on the y-axis, there is the power associated with the load resistance, and on the x-axis the values of load resistance **R**_L. Click on the title of the plot, a cursor will appear. Using this cursor find the maximum power (peak of the graph) point from the plot and note down the corresponding value of the load resistance RL from the x-axis. The value should be equal to that of the Thevenin resistance.



9. Save the Schematic by *clicking File* → *Save as* → '*Name.asc*' and the plots by *clicking File* → *Save plot settings* → '*Name.plt*' for future use and analysis.

REPORT:

- 1. Plot the following:
 - % η vs R_L .
 - Loss (Pin Pout) vs R_L.
 - VL vs R_L.
 - IL vs R_L.
 - PL vs R_L
- 2. Attach all the circuit schematics and plots in your report.