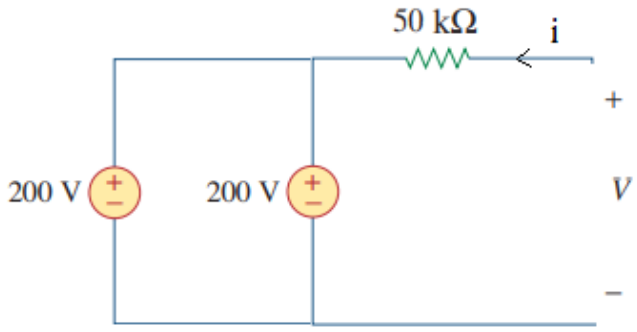
Assignment 2

BRAC University

Semester: Spring 2023
Course No: CSE251
Course Title: Electronic Devices and Circuits

Full Marks: 100
Deadline: **2 March 2023**

1.



(i) Draw the i-V graph of the circuit drawn above**.** Clearly mention the coordinates of x and y-intersecting points on the graph *[Free-hand drawing is sufficient]***.**

(ii) What happens when the resistance becomes **(a) 100kΩ, (b) 200kΩ instead of 50 kΩ? Plot** these cases on the graph and explain the result**.**

[10+10]

2. Analyze the circuit shown below. Assume all the diodes to be ideal.

Part a:

(ii) Assuming w, x, y, z are boolean variables, **analyze** the circuit to find an expression of ckt-1 (the dotted ... rectangle) in terms of w and x, and an expression of ckt-2 (the dashed - - - rectangle) in terms of y and z. **[5+5]**

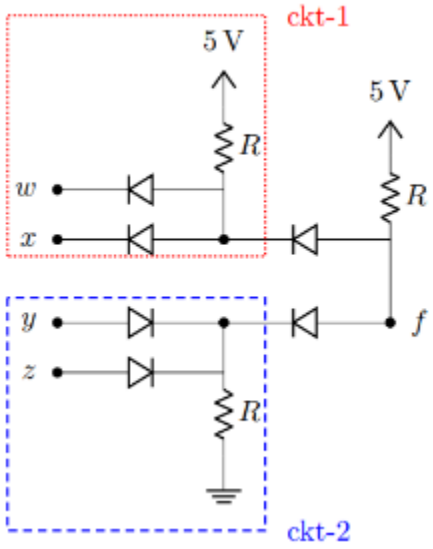
(b) **Analyze** the circuit again to find an expression of f in terms of w, x, y, z. Use results from (a). **[5]**

Part b: Jawad has created a new ride-sharing app: **Juber**. When you request a Juber ride, Juber's algorithm generates 4 signals to determine whether it will be forwarded to a rider. (1) Signal F determines if the rider is free. (2) Signal R determines if the rider is

within close proximity. (3) Signal G determines if the rider has a good rating. (4) Signal N determines if the rider is new. If both conditions 1 and 2 are satisfied, and either condition 3 or condition 4 are satisfied, the request will be connected.

(c) Deduce the logic function using boolean signals F, R, G, and N to implement Juber's algorithm. **[10]**

(d) Design a circuit using ideal diode logic gates to implement this function. **[15]**

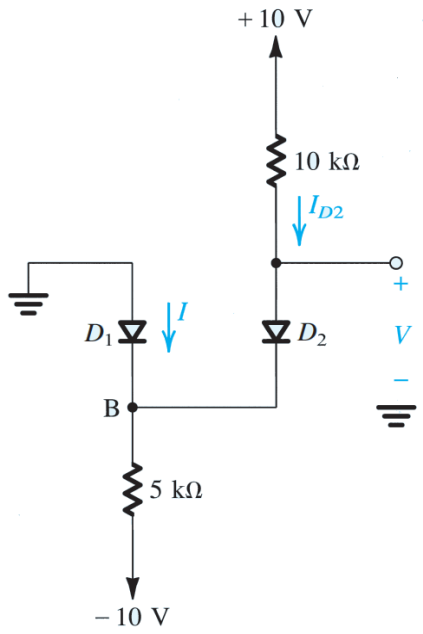


3. Find the values of I and V in the circuit shown below for the following cases:

(i) Assuming the diodes to be ideal**.**

(ii) Assuming the diodes to be non-ideal ***[Hints: use constant voltage drop model with V_{D0}=0.7 V].***

(iii) Assuming the diodes to be non-ideal and use 5kΩ instead of 10kΩ ***[Hints: use constant voltage drop model with V_{D0}=0.7 V].*** **[8×3=24]**



4. Consider the circuit shown in the following Figure. The cut-in voltage of each diode is V_{D0} = 0.7 V**.**

Let v_1 = (5+last digit of your ID×10^{-2}) V. Assume both diodes are conducting. Is this a correct assumption? Why or why not? Determine I_{R1}, I_{D1}, I_{D2}, and v_O **(**if necessary, modify the assumption and **calculate the values for the correct one).**

[16]