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CSE-350: Digital Electronics and Pulse techniques

Exp-03: Study of a TTL NAND gate with totem pole output

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OBJECTIVES

1. Building standard TTL NAND Gate.
2. Measure the voltages and verify the circuit.

Equipments and component list

Equipments

1. Digital Multimeter
2. DC power supply

Component

- NPN Transistor (C828) - x5 pieces
- Diode 1N4003 - x1 piece
- Capacitor - 4.7 μF - x1 piece
- Resistors -
  - 4K - x1 piece
  - 1.5K - x1 piece
  - 1K - x1 piece
  - 100 - x1 piece

Task-01: TTL NAND gate

THEORY

In this task, we will implement a Transistor-Transistor Logic (TTL) NAND gate with a totem-pole output. Transistor-Transistor Logic, or TTL, refers to the technology for designing and fabricating digital integrated circuits that employ logic gates consisting primarily of bipolar transistors. TTL is the successor of diode-transistor logic (DTL), overcoming the main problem associated with DTL, i.e.. lack of speed. TTL provides faster switching compared to DTL; in fact, TTL is the fastest saturated logic family. Figure 1 shows a basic 2-input TTL NAND gate with a totem-pole output.

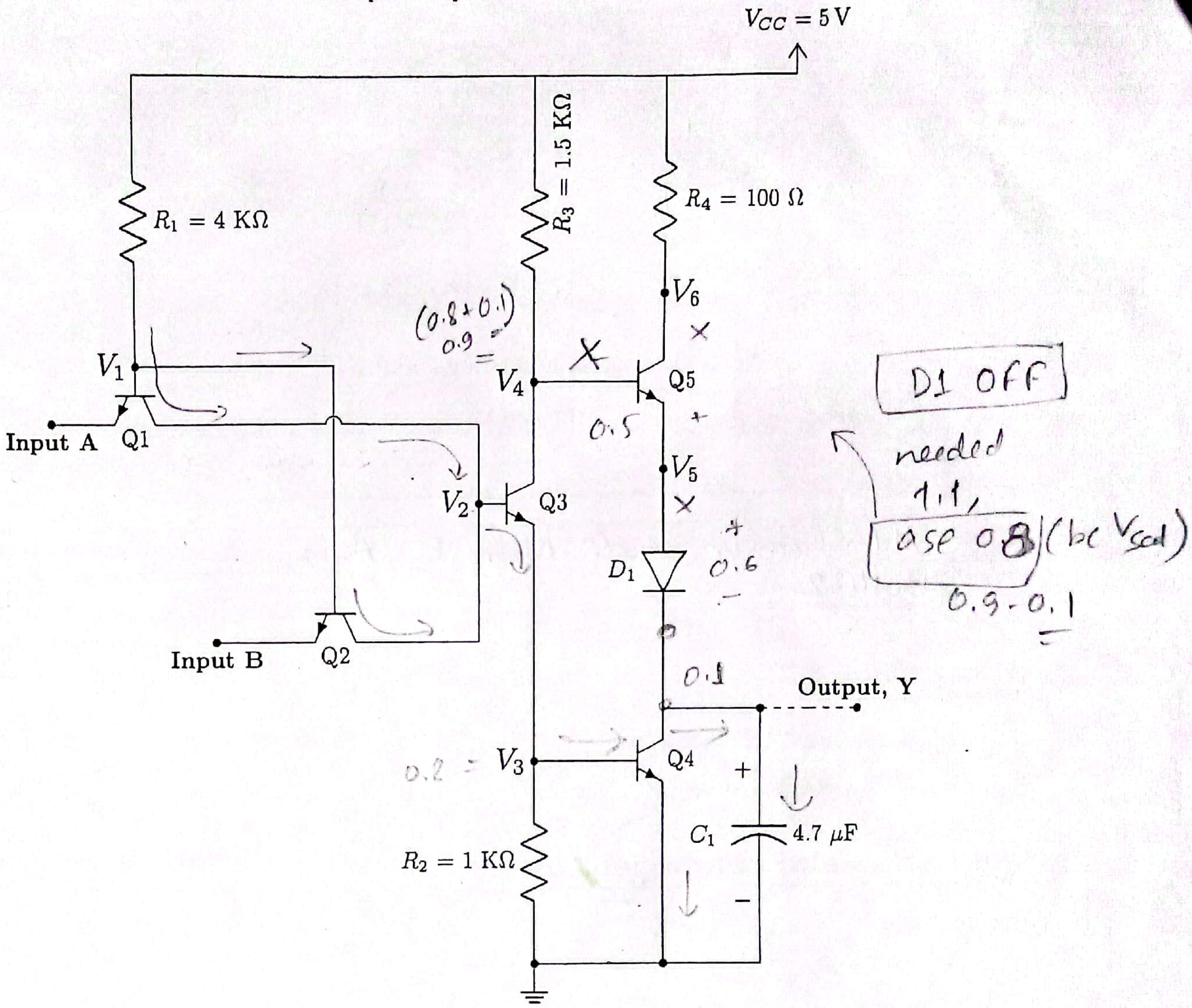


Fig 1: TTL NAND Gate

If any of the inputs A and B is LOW (0.2V), transistor Q1 and/or Q2 will operate in saturation mode and V_2 node will have a voltage of 0.2V + $V_{CE}(sat)$ = 0.4V which causes transistors Q3 and Q4 to be in cut-off mode. Now, node V_4 has 5V while V_6 is obviously less than 5V because of voltage drop in R_4 and Q5 will operate in forward-active mode which means V_{CE} of Q5 is 0.7V. As the diode D_1 has a conducting voltage drop of 0.7V and V_Y will be V_4 - 0.7 - 0.7 = 3.6V approximately which we shall consider as high voltage in output. When both inputs are HIGH (5V), transistors Q1 and Q2 will operate in reverse-active mode. In this case, transistors Q3 and Q4 will be in saturation which ensures that V_{CE} of Q4 is 0.2V and thus the output is 0.2V (LOW).

The most basic TTL circuit has a single output transistor configured as an inverter with its emitter grounded and its collector tied to V_{CC} with a pull-up resistor, and with the output taken from its collector. Most TTL circuits, however, use a totem pole output circuit, which replaces the pull-up resistor with a V_{CC}-side transistor sitting on top of the output transistor. The emitter of the V_{CC}-side transistor (whose collector is tied to V_{CC}) is connected to the collector of the output transistor (whose emitter is grounded) by a diode. The output is taken from the collector of the output transistor.

As mentioned earlier, TTL has a much higher speed than DTL. This is due to the fact that when the output transistor (Q4 in Figure 1) is turned off, there is a path for the stored charge in its base to dissipate through, allowing it to reach cut-off faster than a DTL output transistor. At the same time, the output capacitor is charged from V_{CC} through Q5 and the output diode (D_1), allowing the output voltage to rise more quickly to logic '1' than in a DTL output wherein the output capacitor is charged through a resistor.

Report

Please answer the following questions briefly in the given space.

1. Why is totem-pole output used in place of a passive pull-up resistor?

Ans.

Time to switch output from high to low / low to high affected by presence of capacitor. Time decreases if Req x Capacitance reduced. But just reducing Req also raises power consumption of circuit by a drastic amount as more I flows.

Totem pole allows low output resistence at logical 1 transition. Pullup network equivalent resistence now decreased (so faster switching of output from low to high) without as much power consumption

2. What is the function of Q3 transistor(phase-splitter)?

Ans. To switch on transistors Q4 and Q5 alternatively

If current is allowed to flow through from Q_3 emitter to Q4 base (turning it ON), no current flows through to base of Q5 (so OFF)

3. What may happen if diode D_1 is not used in the circuit?

Ans.

Q_5 may get shorted to ground through Q_4 hence damaging Q_4. Diode also prevents reverse current flow. ~~that may~~ Inaccurate & outputs also prevented

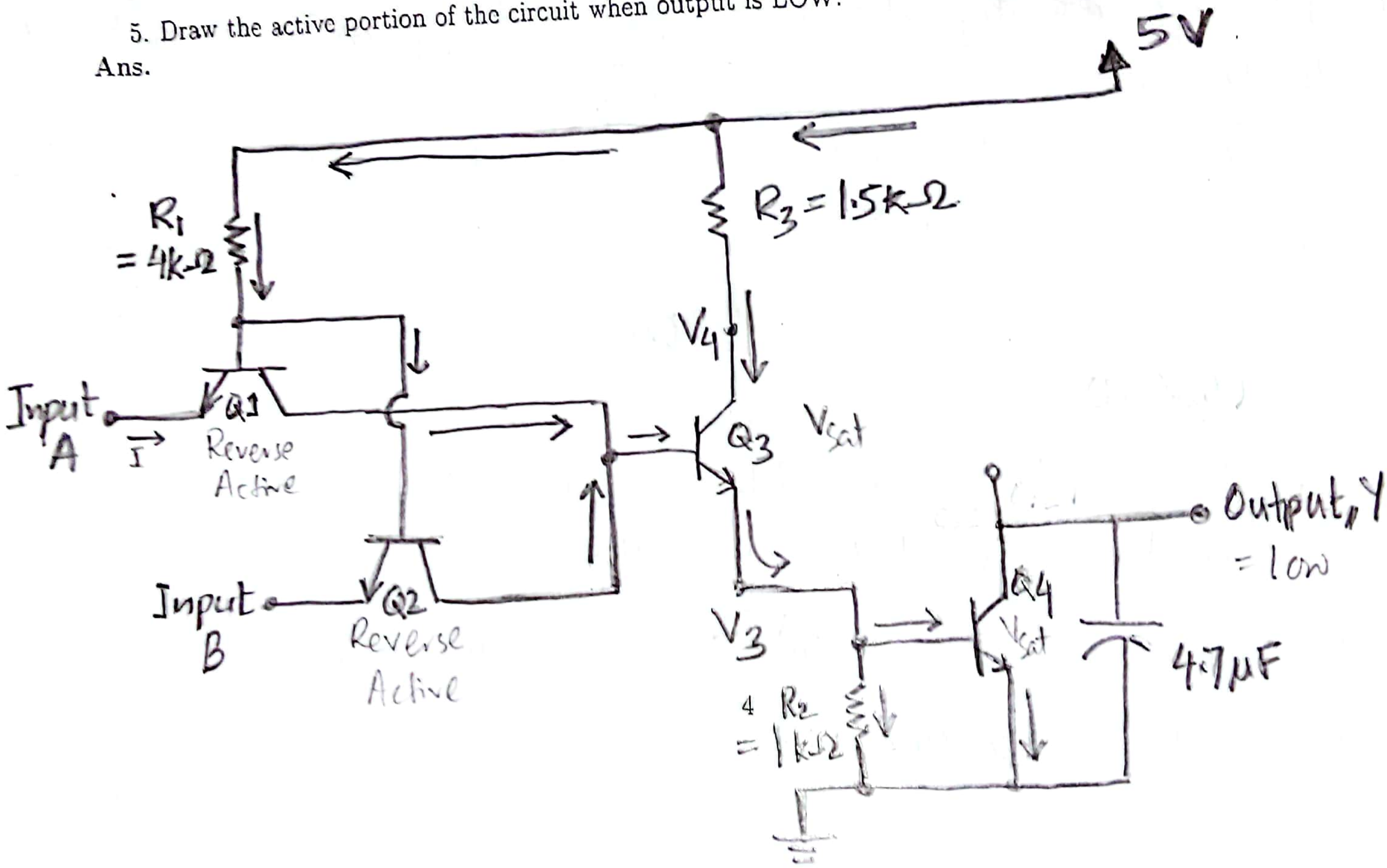
4. What is the mode of operation of the Q5 transistor when output is HIGH?

Ans.

forward Active

5. Draw the active portion of the circuit when output is LOW.

Ans.



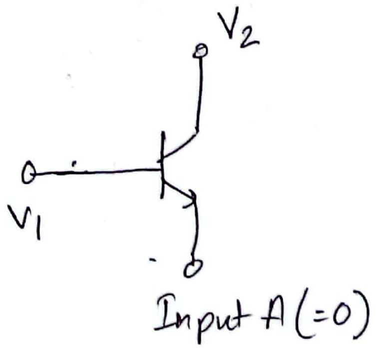
6. What is the operating mode of Q1 and Q4 transistors when Input A is LOW? Verify using experimental data.

Ans.

Q_1 = saturation

Q_4 = cutoff

Q1



$V_1 = 0.68$ V

$V_{BE} = 0.68$V (V_{sat})

$V_2 = 0$ V

$V_{CE} = 0$ V (very low)

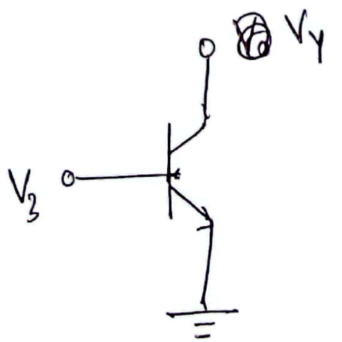
$V_1 = 0.71$ V

$V_{BE} = 0.71$ V (V_{sat})

$V_2 = 0.03$ V $\simeq 0$ V

$V_{CE} = 0$ V (very low)

Q4



$V_3 = 0$ V (both cases)

Since $V_{base} < 0.7$ V, transistor Q4 will not be turned on at all (cutoff)

Procedure:

1. Connect the circuit as shown in Figure 1.
2. Observe the output for all possible input combinations and fill up table-1.

Data Table

Adrita 17/06/23

$R_1 \rightarrow 3.89 k\Omega$
$R_2 \rightarrow 0.9 k\Omega$
$R_3 \rightarrow 1.46 k\Omega$
$R_4 \rightarrow 99.4 k\Omega$

V_A (V)	V_B (V)	V_1 $Q_1 \rightarrow B$ (V)	V_2 $Q_3 \rightarrow B$ (V)	V_3 $Q_4 \rightarrow B$ (V)	V_4 $Q_5 \rightarrow B$ (V)	V_5 $Q_5 \rightarrow E$ (V)	V_6 $Q_5 \rightarrow C$ (V)	V_Y $Q_4 \rightarrow C$ (V)
0	0	0.68	0.00	0.00	4.97	4.92	4.97	4.28
0	4.97	0.71	0.03	0.00	4.97	4.58	4.97	4.28
4.97	0	0.71	0.04	0.00	4.97	4.93	4.97	4.28
4.97	4.97	2.23	1.57	0.81	1.15	0.35	4.97	0.04

Table 1: Table for TTL NAND gate