

# CSE 350: Digital Electronics and Pulse Techniques.

Pre-Requisite: CSE 251, CSE 260 (DLD)



Course Instructor : Shahnewaz Ahmed (SHA)

Marks Distribution :-

	Attendance : 7% <Bonus>
→	Homework (box) : 8% <deadline>
(central)	Quiz (proctored) : 15% <4/best 3> [Saturday / Thursday]
	Lab : 20%
(13th May 2-5 pm)	Midterm (1hr) : 15% (offline on campus)
	Final (2.5 hr) : 35% ( .. .. .. )
	100%

# Course Content :-

70% 1. Digital Electronics :- { Logic families + DC analysis of these circuits }

30% 2. Pulse Technique :- Signal generators, A/D, D/A

# Review (Circuit and Electronics) (250)

Charge, Voltage, Current, Ohm's law, KCL, KVL, Node Analysis

■ Charge : Fundamental property of elementary particle

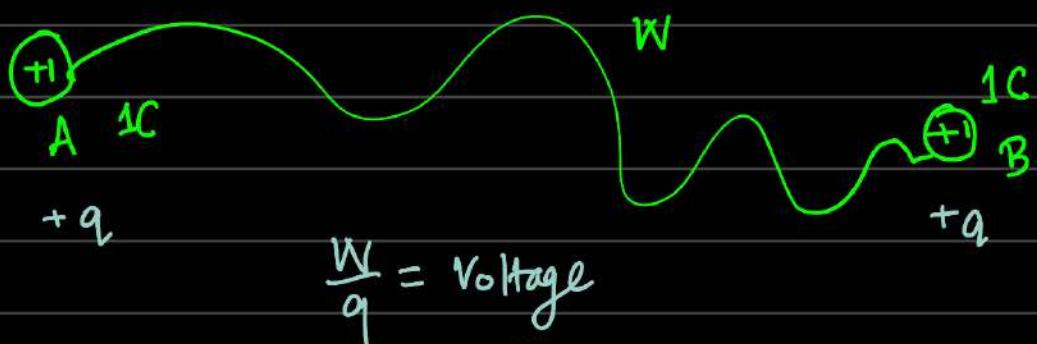
★  $\frac{\text{Electron}}{(-e)}$ ,  $\frac{\text{proton}}{(+e)}$ ,  $\frac{\text{neutron}}{0}$  }  $\text{atom}$   $\beta$   $v_e$

★ SI (Coulomb)

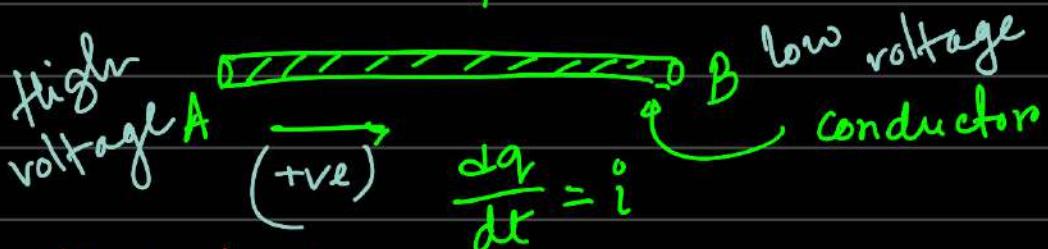
★ Force  $\rightarrow$  [Coulomb's law.]  $\rightarrow$  Work

$(\mu, \tau, q, \lambda^+, \Sigma)$

# Voltage: The amount of work needed to displace a unit charge from one place to another.



# Current: The amount of charge flow through a conductor per unit time.



# Ohm's law:-

In a fixed temperature the current flows through a conductor is proportional to the voltage difference across the conductor.

$$V_{AB} = V_A - V_B \quad I \xrightarrow{V_A} \xrightarrow{V_B} I \propto (V_A - V_B) \quad \Rightarrow I = G(V_A - V_B)$$

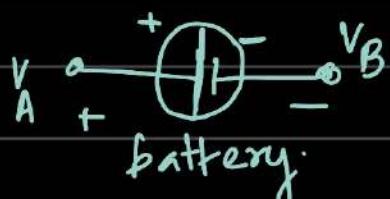
$$R = \frac{1}{G} \quad [G \rightarrow \text{conductance}] \quad \Rightarrow (V_A - V_B) = \frac{1}{G} I = R I \quad [R \rightarrow \text{resistance of the conductor}]$$

Resistor :-

$\xrightarrow{R}$  (symbol) (Ohm)

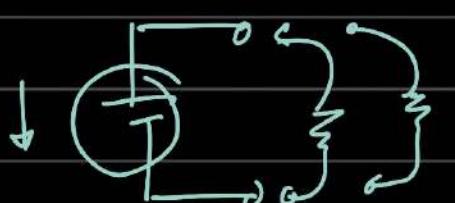
$\xrightarrow{R=0}$  Perfect conductor ( $R^{\text{unit}} = 0$ )

Voltage Source :-



$$V_A - V_B = V_D$$

They voltage will remain constant.



internal resistance ( $35\Omega$ )

source resistance  
voltage.  $v_s = \frac{I}{T} (m)$

Capacitor :-



$C$

parallel plate capacitor

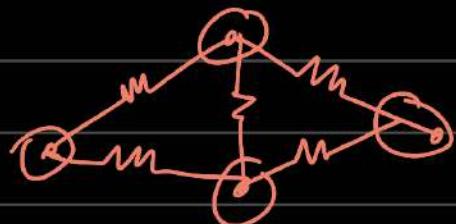
$$Q \propto V$$

$$Q = CV$$

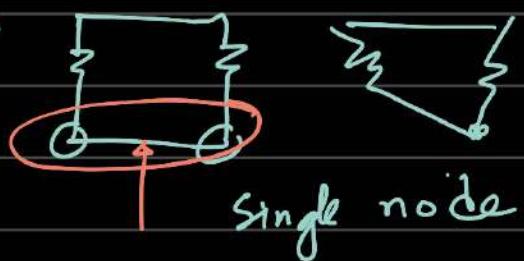
Amount of stored charge is proportional to voltage difference across the capacitor.

→ Electrical Components :- { Active  $\rightarrow$  power generate  
Passive  $\rightarrow$  not

Node :- The interconnected point between one or more electrical component is called node.



4 nodes



Single node

KCL : The algebraic sum of current in a node is zero.



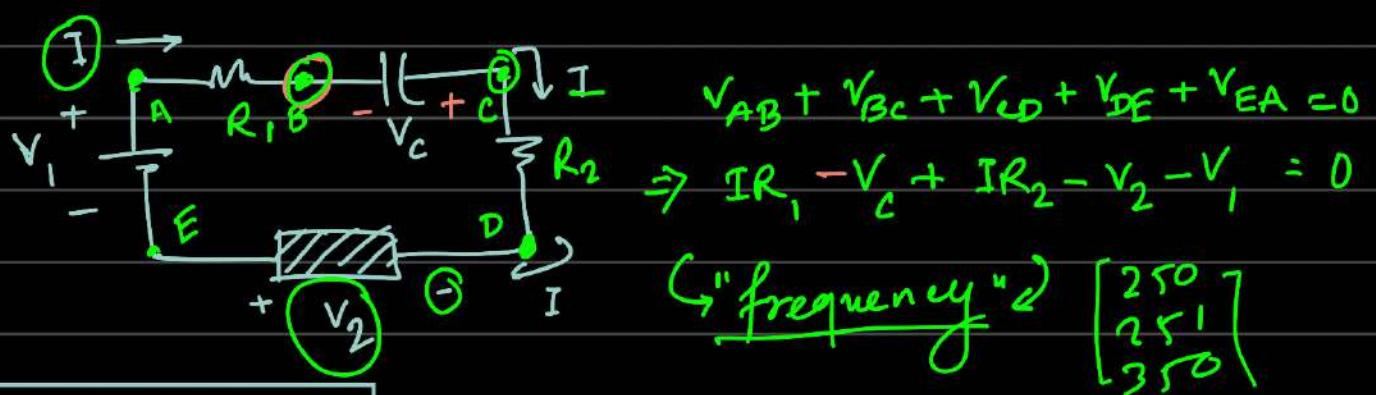
# current exiting a node is considered positive

# current entering a node is considered negative

$$-i_1 + i_2 - i_3 - i_4 + i_5 = 0$$

KVL : Kirchhoff's voltage law :

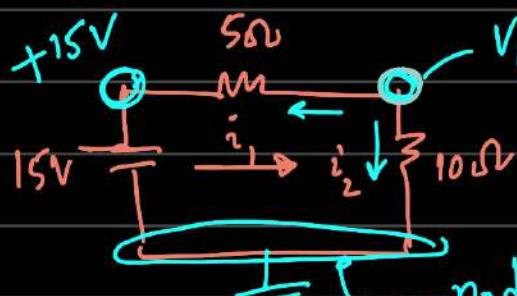
The voltage drop across within a loop inside a circuit is zero.



**Nodal Analysis** :- Goal :- "node voltage"  $\leftarrow$  find  
 "current"  $\rightarrow$  ohm's law.

1. Identify reference voltage (given)
2. Identify unknown node voltage
3. Write the node equation of
4. Solve the node equations together.

Example 1



$$V_1 : \frac{V_1 - 0}{10\Omega} + \frac{V_1 - 15}{5\Omega} = 0$$

$$\Rightarrow V_1 \left( \frac{1}{10} + \frac{1}{5} \right) = \frac{15}{5}$$

node voltage (0V)

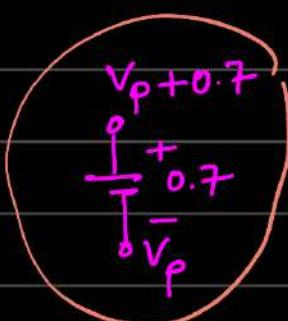
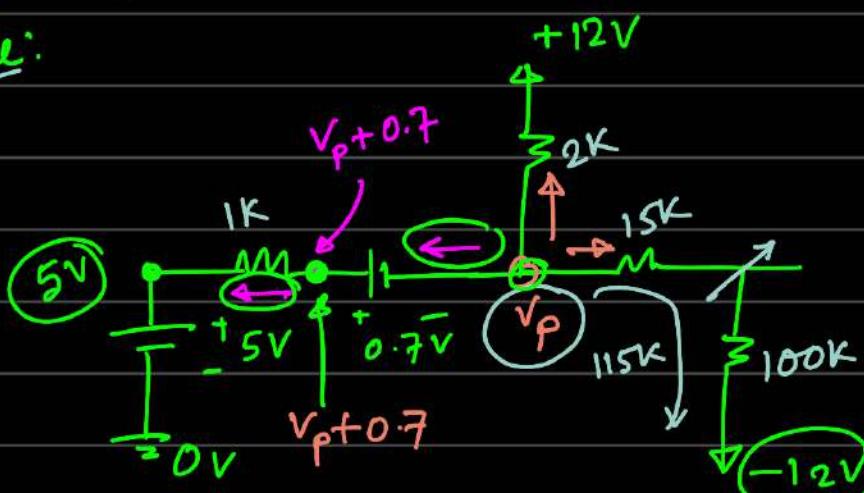
$$i_1 = \frac{15 - 10}{5} = 1 \text{ A}$$

$$\Rightarrow V_1 \left( \frac{3}{10} \right) = 3$$

$$i_2 = \frac{10 - 0}{10} = \frac{1}{9} \text{ A} = 0.11 \text{ A}$$

$$\Rightarrow V_1 = \frac{10}{9}$$

Example 2:



Node equation :  $V_p :$

$$\frac{V_p - 12}{2K} + \frac{V_p - (-12)}{115K} + \frac{(V_p + 0.7) - 5}{1K} = 0$$

$\Rightarrow V_p = \text{?} \quad (\text{Calculator})$

## Lecture 2: CSE 251 Review : Electronic Circuits and Devices.

Electronics : The method or process that can be used to control <sup>the</sup> flow of electron using external electric field/voltage.

Spintronics, Photonics, Twistrionics, Valleytronics...

Dependening on conductivity we can classify materials into three main category.

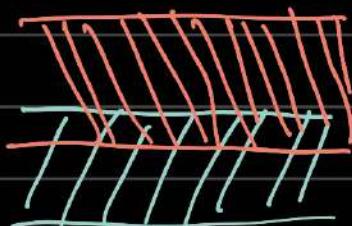
1. Metal (good conductor) ( $10^{-13} \Omega \text{m}$ )

2. Semiconductor ( $10^1 - 10^4 \Omega \text{m}$ )

3. Insulator (bad conductor) ( $10^{10} \Omega \text{m}$ )

Electron's Energy levels within a solid might form many bands. Quantum Mechanics

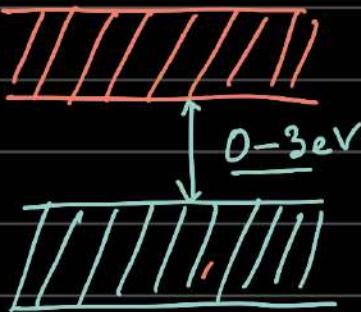
Metal



Ex: Al, Ag, Cu, Au  
Na, Mg, K

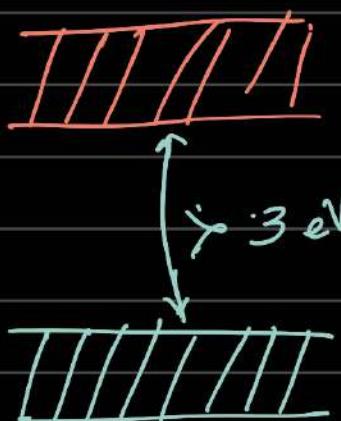
Semiconductor

Conduction band



Ex: Si, Ge  
GaAs, GaN, InSb

Insulator

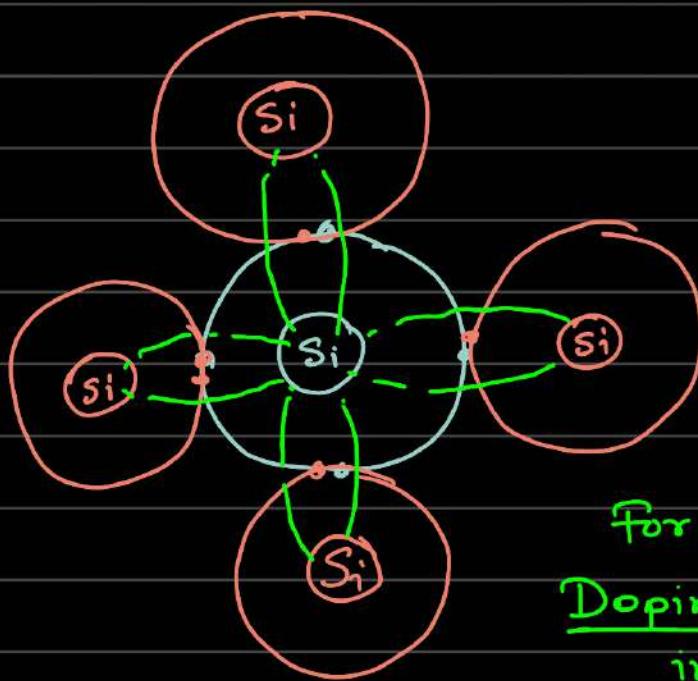


Ex:  $\text{SiO}_2$ ,  $\text{Si}_3\text{N}_4$   
 $\text{SiC}$ ,  $\text{Al}_2\text{O}_3$

### # (Si) Semiconductors

1. Intrinsic Semiconductor : Pure semiconductor crystal. (Not very useful)

2. Extrinsic Semiconductor : Impurity is being introduced here. (Main concern)



Si:  
electron configuration:  
 $1s^2 2s^2 2p^4 3s^2 3p^2$

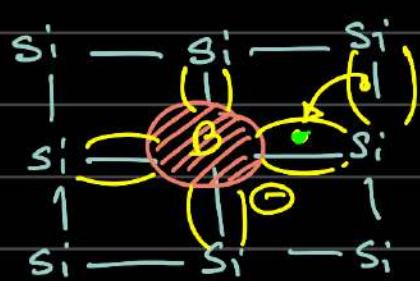
→ Pure Crystal

→ Intrinsic Semiconductor

for extrinsic semiconductor:-

Doping :- The process of introducing impurity

① P-type Semiconductor :-



① Dopant atom :- Group III A

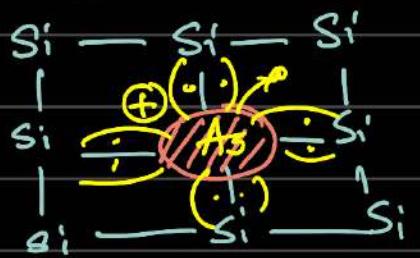
B, Al,

$1s^2 np^1$

③ (ve) bound charge

② Majority charge carrier is called hole.

② N-type Semiconductor :-



① Dopant atom :- Group VA

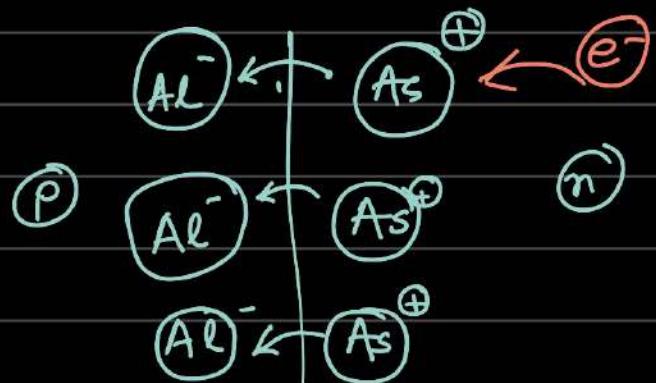
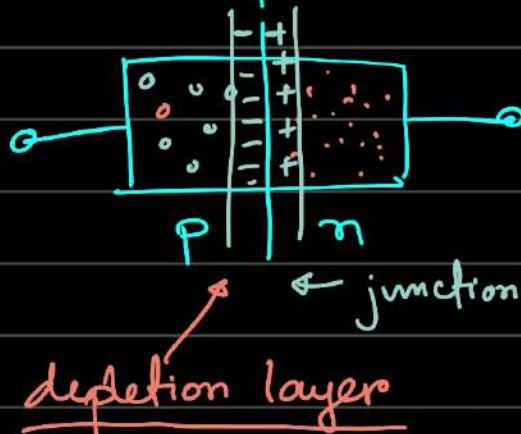
P, Sb, As

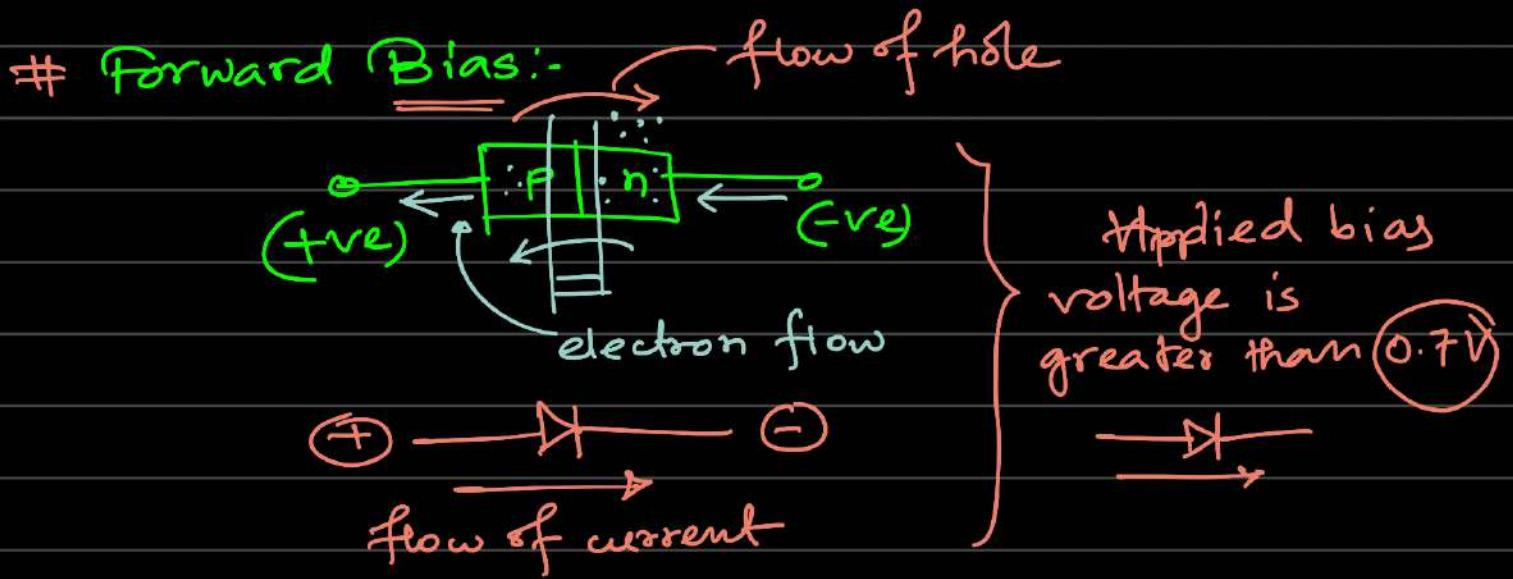
$ns^2 np^3$

② Majority charge carrier is electron.

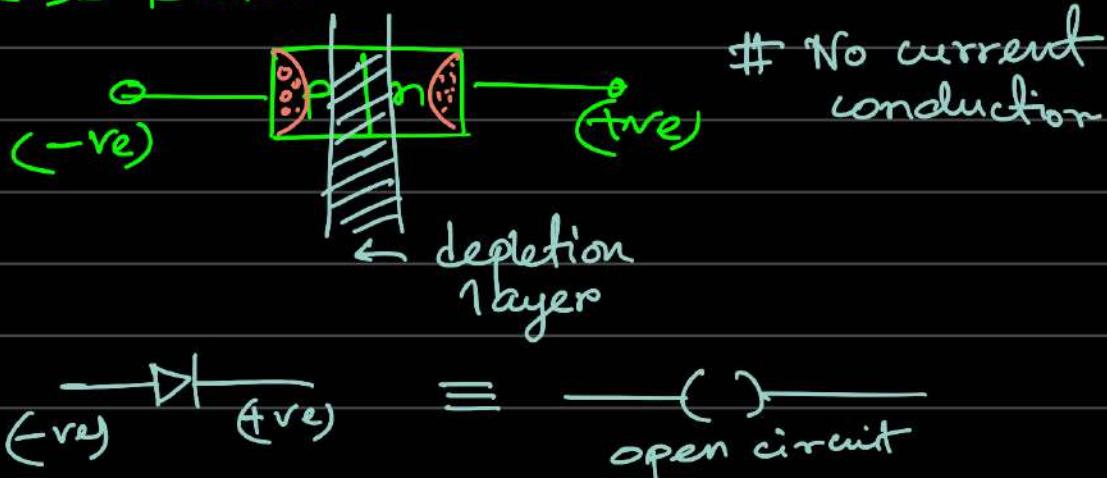
③ (tre) Bound charge.

P-n junction Diode:-

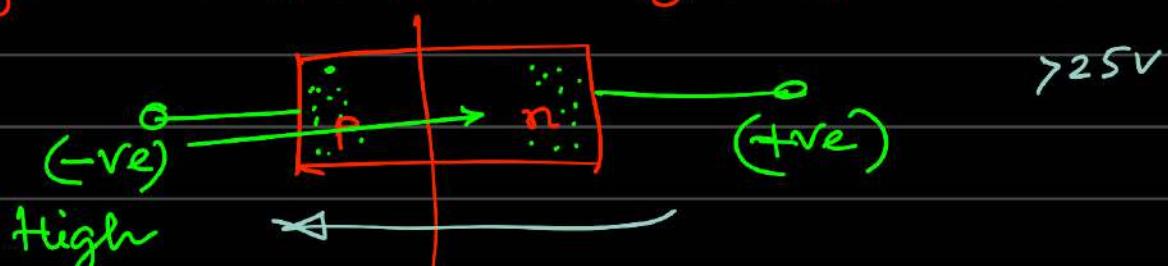




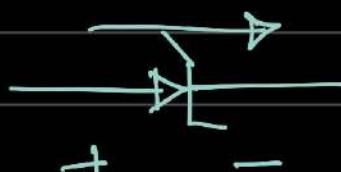
# Reverse Bias:-



# Breakdown: If reverse bias voltage is high then the diode might start conducting.



# Zener Diode:-



Forward conduction  
voltage = 0.7V

↑ Zener voltage

if the reverse bias voltage  
is greater than Zener voltage Zener  
diode will start conducting.

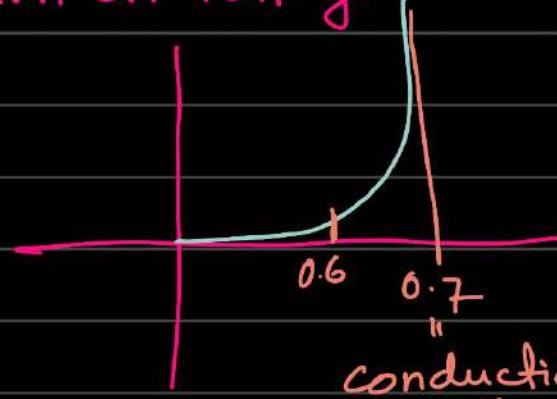
# Activation voltage/ Turn on voltage:

Si



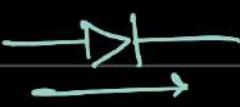
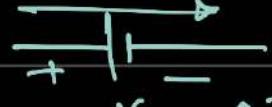
$$V_g = 0.6V / 0.65V$$

$$V_g \text{ (diode)}$$



conduction voltage =  $V_D$

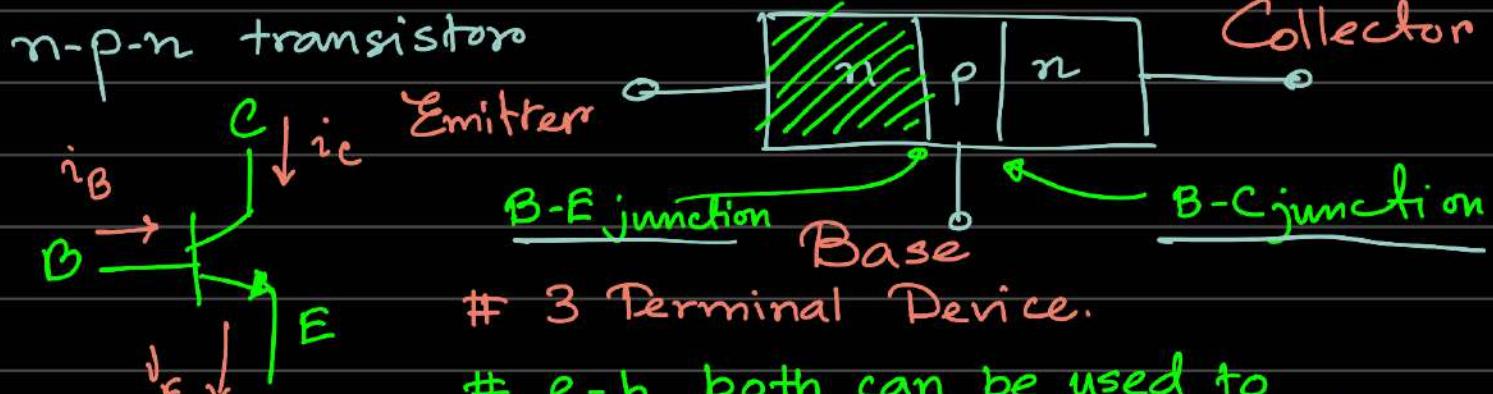
Constant Voltage Drop Model :-

①   $\equiv$    $V_D = 0.7V$

②   $\equiv$  

③ Activation voltage ?

Transistor :- Switching Application:



# e-h both can be used to conduct current. (Bipolar)

Bipolar Junction Transistor (BJT)

B-C Junction	B-E Junction	Mode
Reverse	Forward	forward Active (FA)
Forward	Forward	Saturation
Reverse	Reverse	Cutoff
forward	Reverse	Reverse Active

## Reverse Active mode

Collector and Emitter switch their roles.

$(V_{BE} < 0, V_{BC} > 0)$

$$V_{BC} = 0.7V, \frac{I_E}{I_B} = \beta_R$$

$\beta_R \sim 0.1, 0.2, 0.3$

$V_C < V_B \ll V_E$  (TTL)

## Cutoff mode

$(V_{BE} < 0, V_{BC} < 0)$

$$V_{BE} < 0.5V \quad \text{True}$$

$$I_C = I_B = I_E = 0$$

$$V_T(\text{transistor}) = 0.5V$$

Activation or turn on voltage.

$V_{BC}$

$(V_{BE} > 0, V_{BC} > 0)$

## Saturation mode

If BJT is in saturation mode

$$V_{BE} = 0.8V, V_{CE} = 0.2V/0.1V$$

$$V_{BC} = V_{BE} - V_{CE} = 0.6 > 0$$

$$\frac{I_C}{I_B} = \beta_{\text{forced}} < \beta_{\text{Forward}} \quad \text{Checking condition}$$

$V_{BE}$

## Forward Active

$(V_{BE} > 0, V_{BC} < 0)$

$$V_{BE} = 0.7V, \frac{I_C}{I_B} = \beta_{\text{Forward}}$$

$\beta_F \sim 30, 50, 100$

Forward  $\beta$ , common emitter current gain

$$V_{CE} > 0.2V \quad \text{Checking Condition}$$

## Lecture 3: Introduction to Digital logic families.

$\neg \neg \text{D} \text{O}$  NAND

$\neg \text{D} \text{O}$  NOT

$\neg \neg \text{D} \text{O}$  NOR

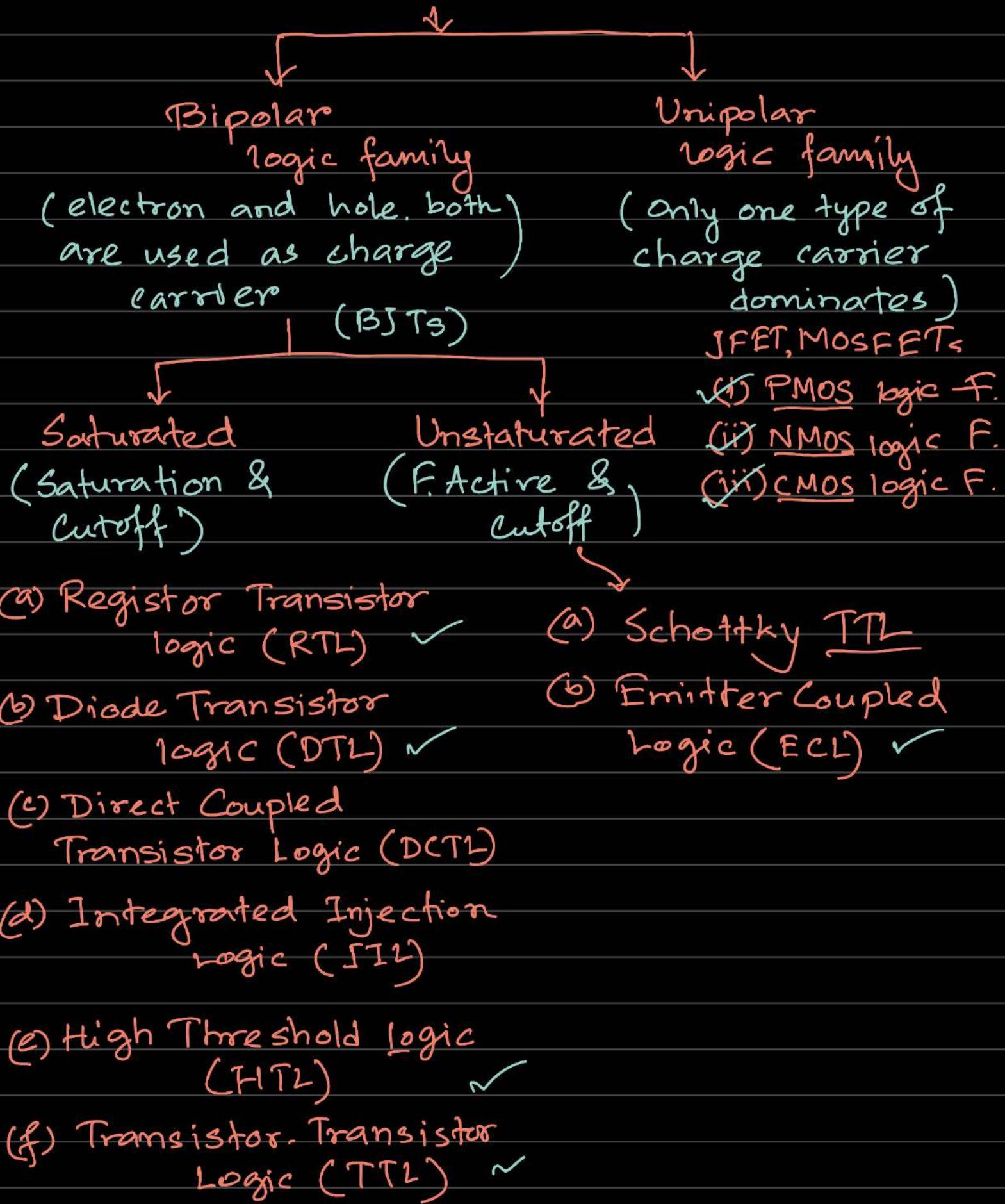
→ These gates are abstract, because they just represent logical operations.

→ Digital logic families distinguishes different ways of constructing logic gates using electronic devices.

$\neg \text{D} \text{O}$  NOT

$\neg \neg \text{D} \text{O}$  NAND

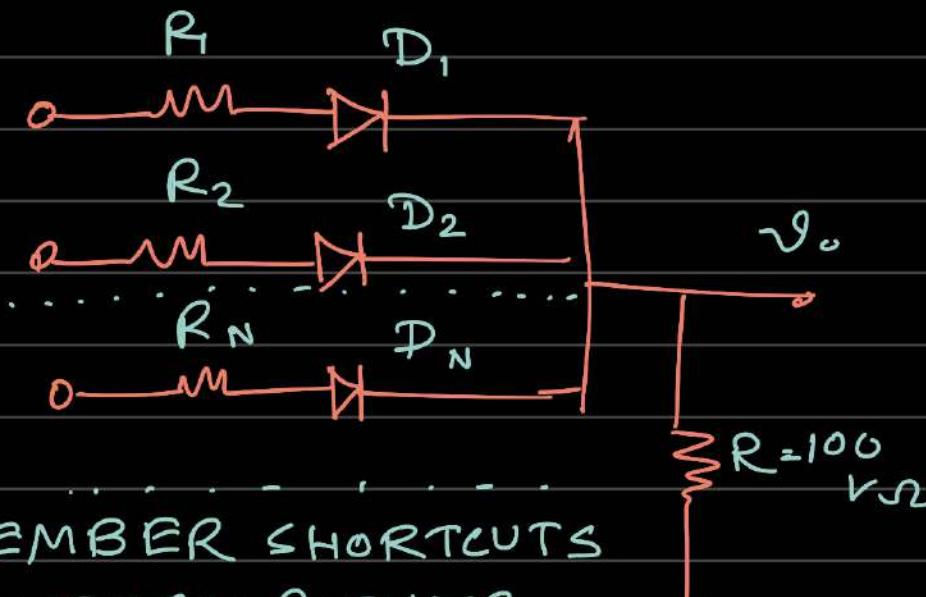
# Digital logic family



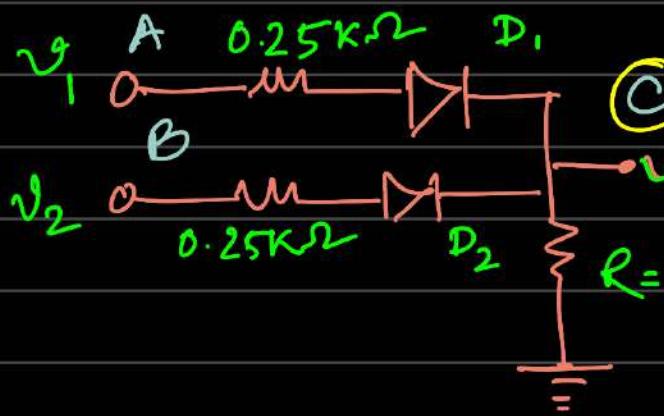
## # DIODE LOGIC :

### OR GATE :-

$$R_1 = R_2 = R_3 \\ = 0.25\text{ k}\Omega$$



# DON'T REMEMBER SHORTCUTS  
WITHOUT UNDERSTANDING  
THE LOGIC BEHIND IT.



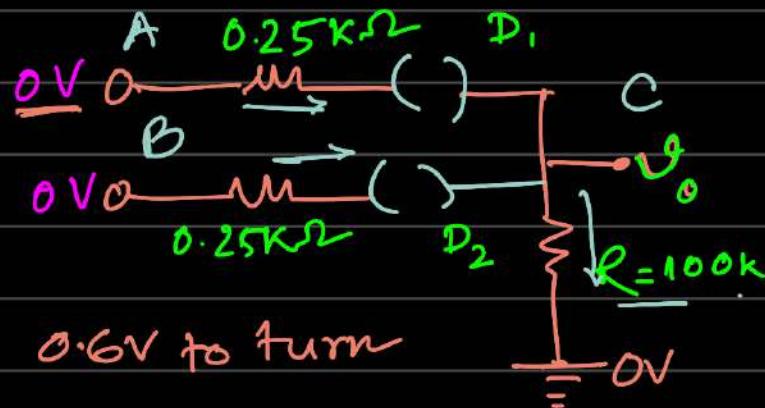
	A	B	$v_1$	$v_2$	$v_o$	C
①	0	0	0V	0V	0V	0
②	0	1	0V	5V	4.28V	1
③	1	0	5V	0V	4.28V	1
④	1	1	5V	5V	4.2946V	1

# Assume. logic 1 means 5V on input side.

From input side logic 0 understood as 0 voltage.

### Case ①:

First thing to check whether diodes are ON or OFF.



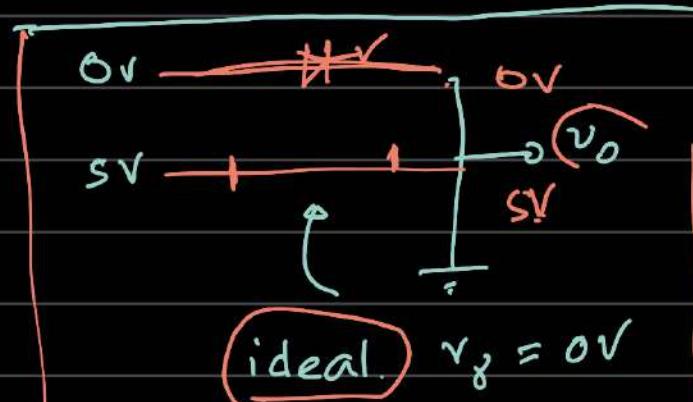
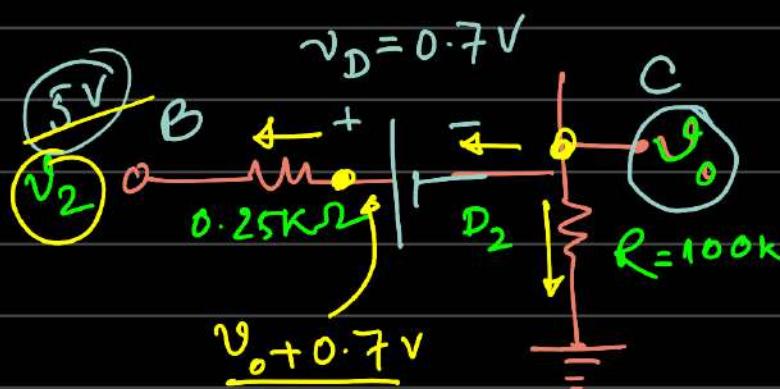
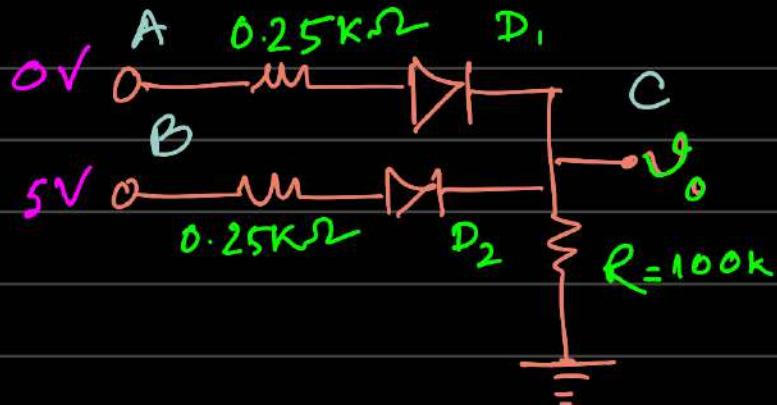
FACT: we need at least 0.6V to turn on any diode.

# Conclusion :  $D_1$  and  $D_2$  are OFF.

$$\frac{V_o - 0}{R} = i = 0 \Rightarrow V_o = 0V \quad | \quad V_o = 0V$$

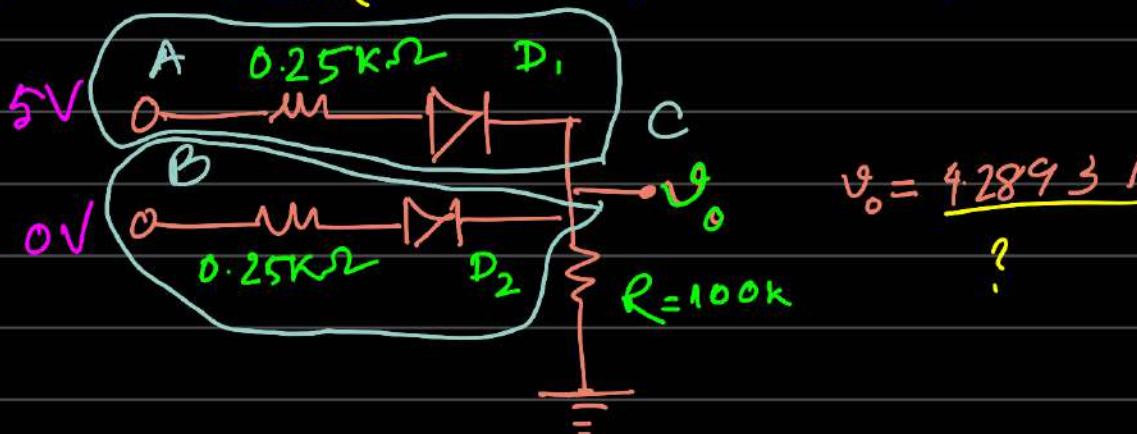
### Case ②:

- ① D1 diode will turn OFF
- ② D2 diode will be ON.



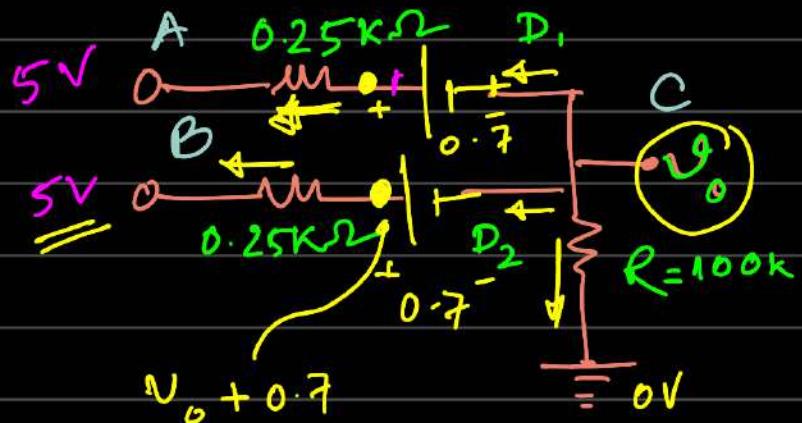
$$\frac{V_o - 0}{100k} + \frac{(V_o + 0.7) - 5}{0.25k} = 0 \Rightarrow V_o = 4.2893V$$

### Case ③:



### Case ④:

✓



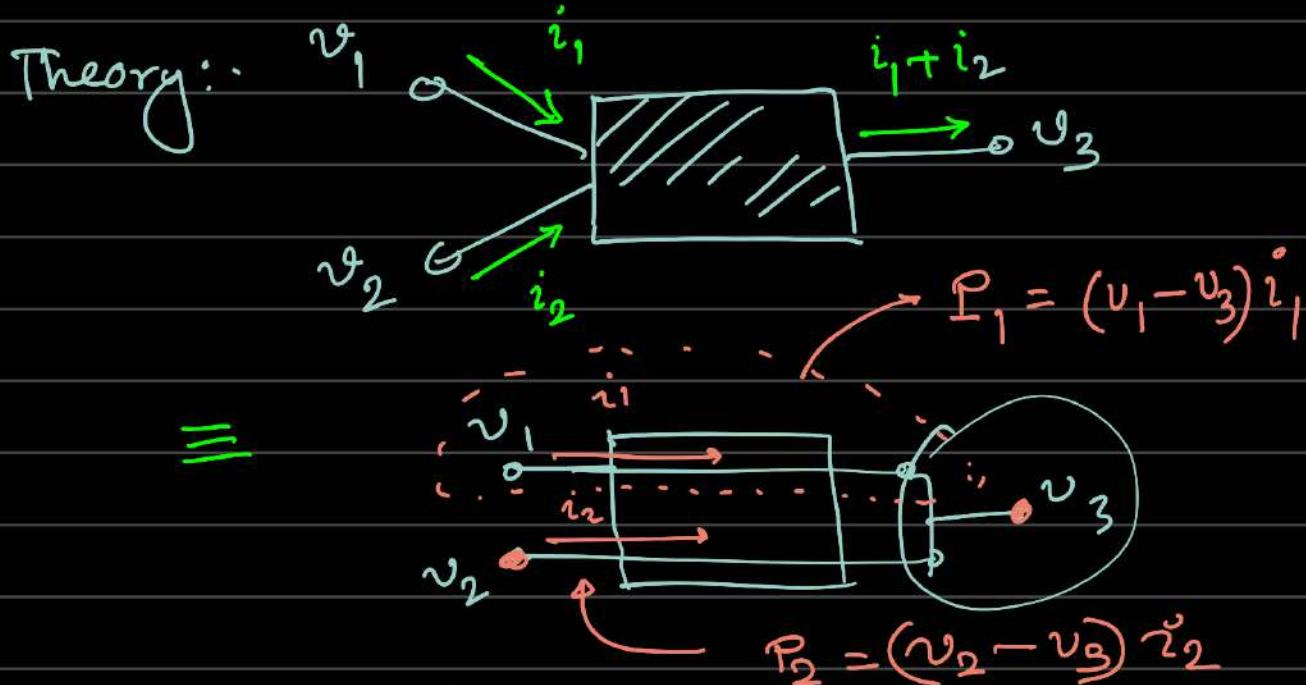
$$\frac{V_o - 0}{100k} + \frac{(V_o + 0.7) - 5}{0.25k} + \frac{(V_o + 0.7) - 5}{0.25} = 0$$

$$V_o = 4.2946V$$

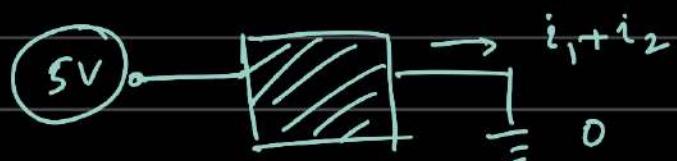
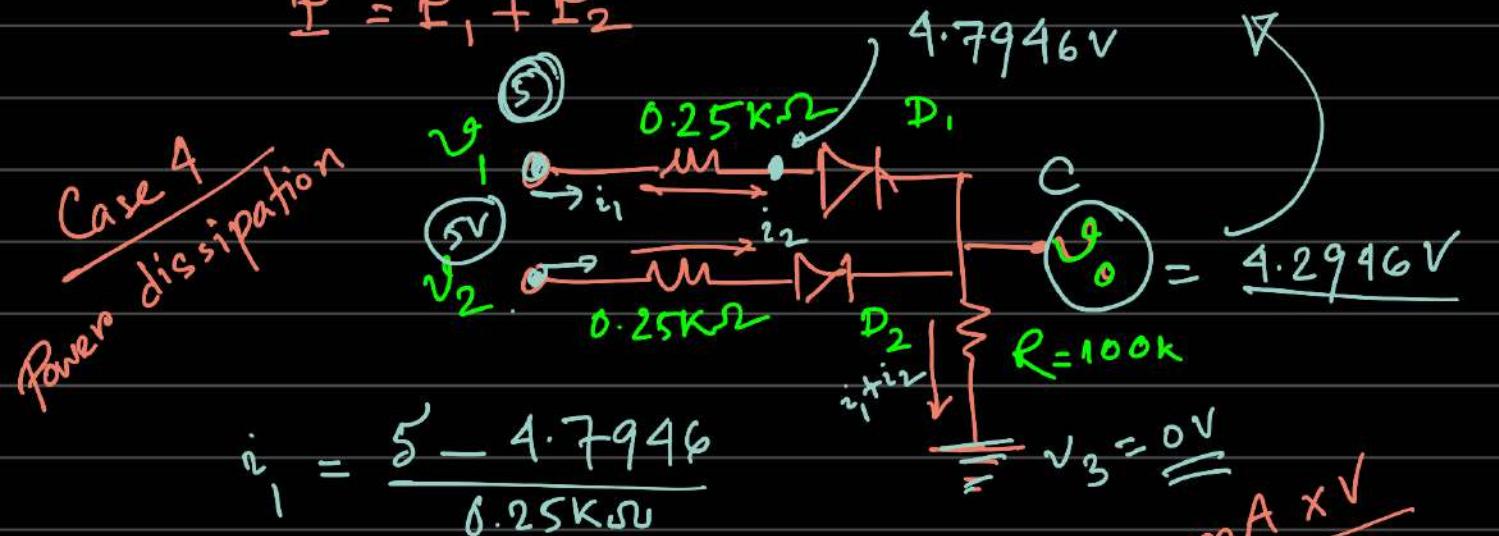
4.28, 4.29 # logical High Low can be different at input and output side.

# Smallest voltage will be considered as logical High.  $V_{OH} = 4.28..V$

## Power Dissipation Calculation :-

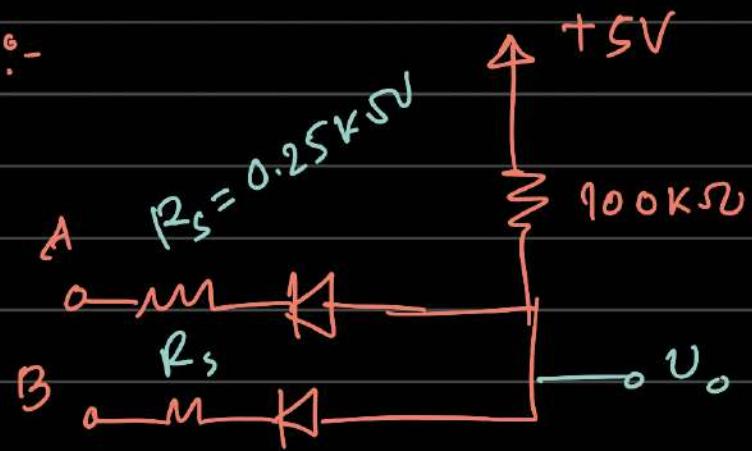


$$P = P_1 + P_2$$



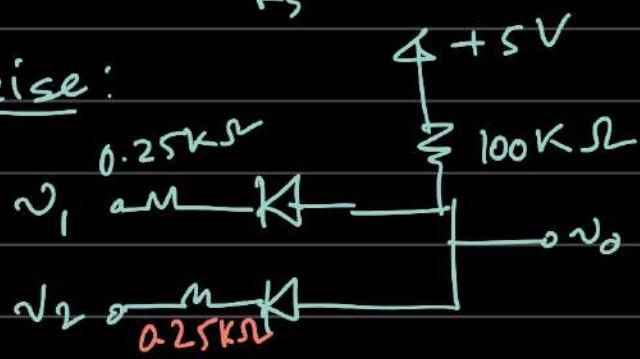
"BUX"

## AND GATE :-



.....  
N  $\text{---} \text{---} \text{---}$   
 $R_s$

## # Exercise :



$V_1$	$V_2$	$V_o$
5V	5V	5V
0V	5V	{ } 0.68V
5V	0V	{ } -0.7V
0V	0V	

# Logical low voltage at output side  $\rightarrow$  Highest voltage

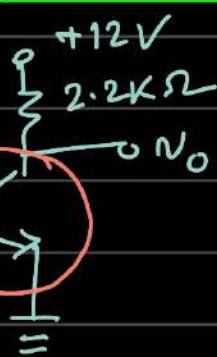
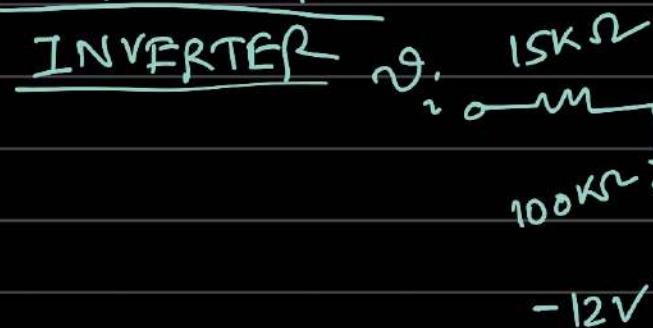
$$V_{oL} = 0.7V$$

↑  
Output low

# Any output voltage at this circuit will be regarded as output low voltage if the voltage is less than  $V_{oL}$ .

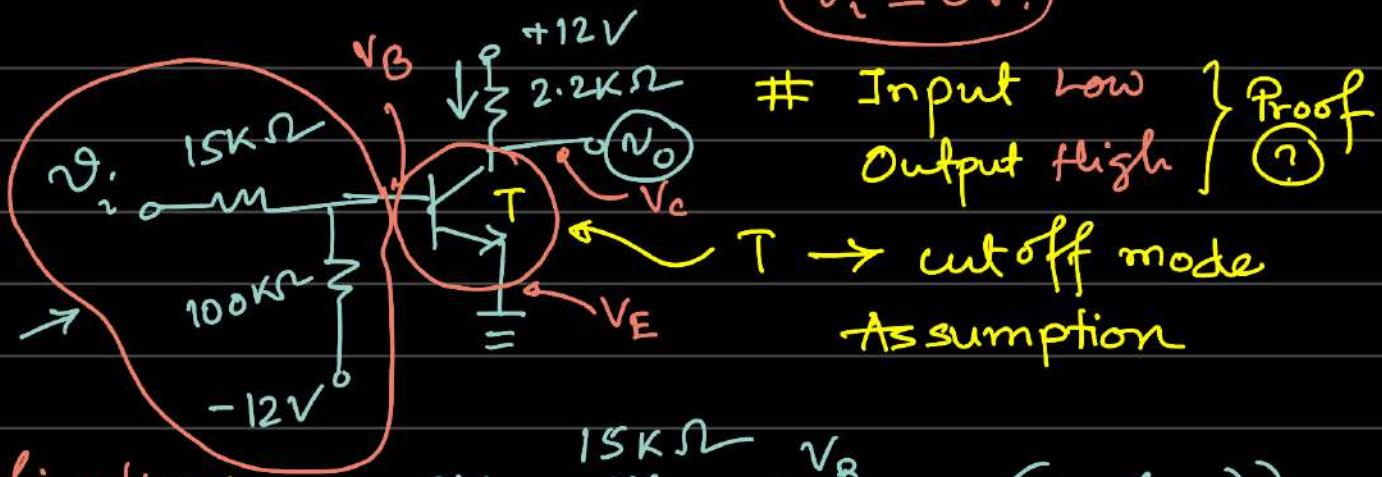
## Resistor-Transistor Logic (RTL)

### NOT GATE :-



$\rightarrow$  Saturated logic

## Case: ①



## Verification:

Verification circuit diagram. The input voltage  $V_i$  is 0V. The base voltage  $V_B$  is 0V. The collector voltage  $V_C$  is 12V. The emitter voltage  $V_E$  is 0V. The output voltage  $V_O$  is high (12V). The text "Assumption is correct." is written to the right of the circuit.

$$\frac{V_B - 0}{15k} + \frac{V_B - (-12)}{100k} = 0$$

$$\Rightarrow V_B = -1.565V \quad | \quad V_E = 0$$

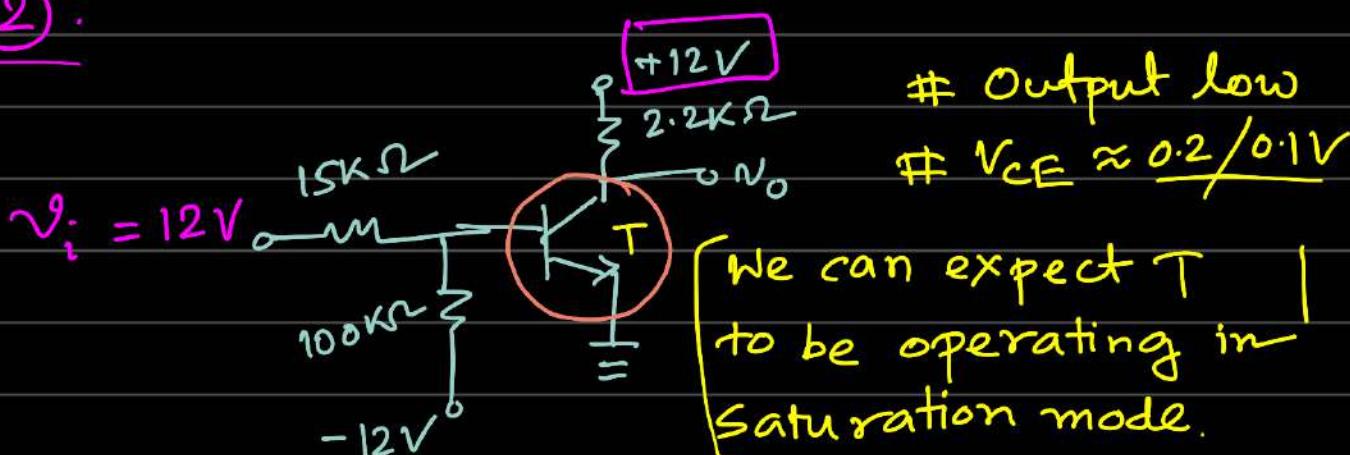
$$V_{BE} = -1.565V < 0.5V$$

$$\frac{(0 - (-12))}{115k} = \frac{V_B - (-12)}{100k}$$

For cutoff mode:  $I_B = I_C = I_E = 0$

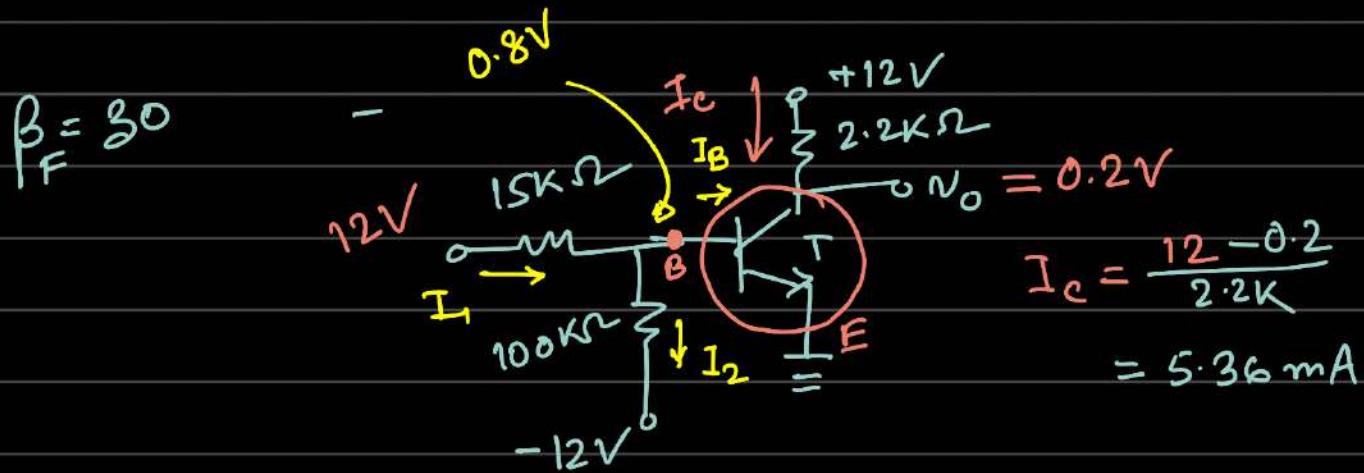
$$I_C = 0 = \frac{(12 - V_C)}{2.2k} \therefore V_C = 12V = V_o$$

## Case ②:

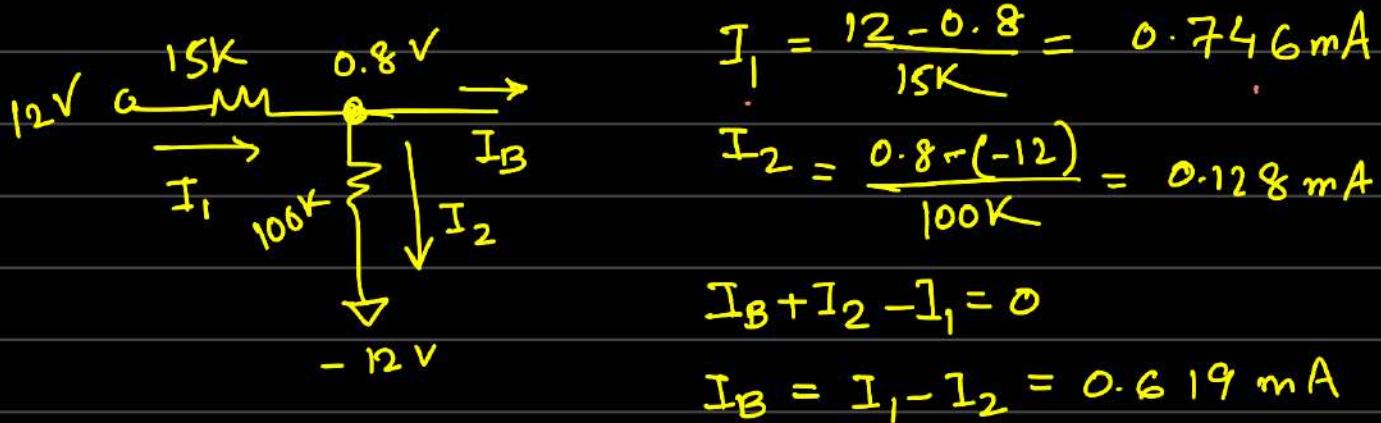


RTL  $\rightarrow$  saturated logic family.

Logic transistors are connected to the output terminal.



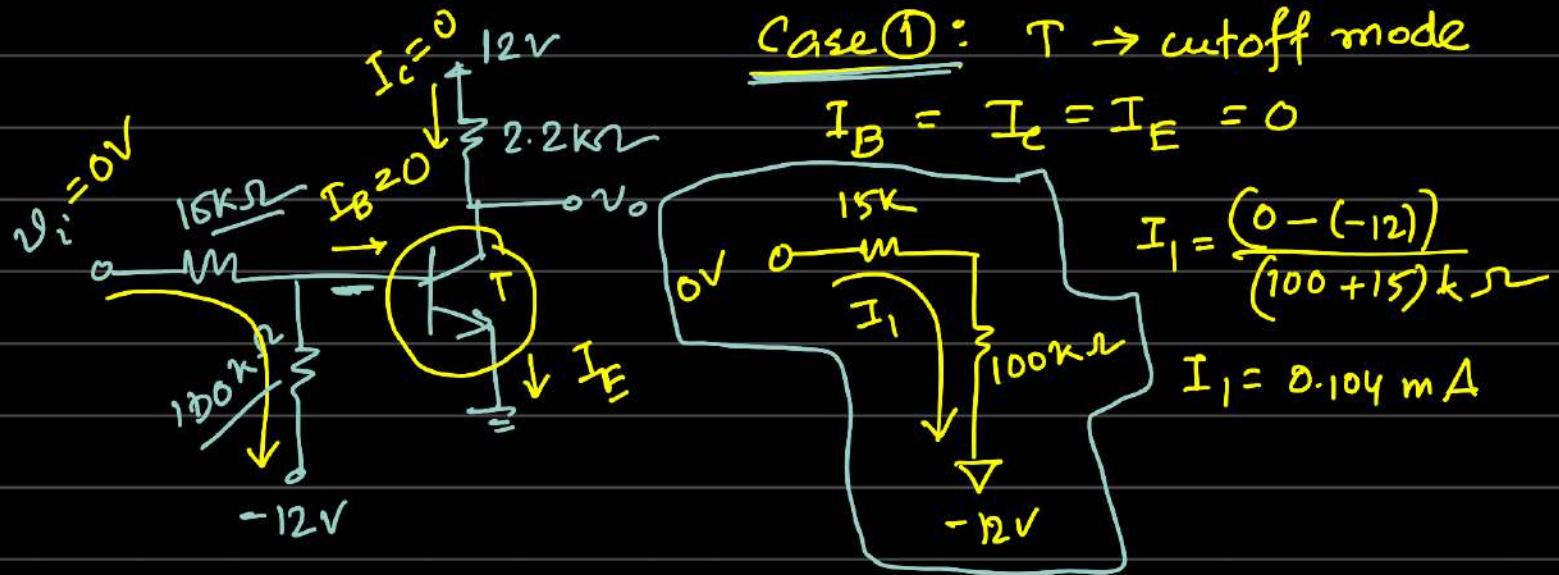
$T \rightarrow \text{Saturation}, \boxed{V_{BE} = 0.8V, V_{CE} = 0.2V}$

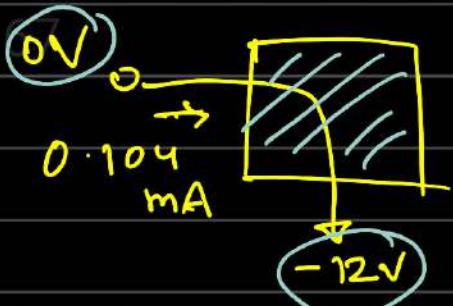


$$\beta_{\text{forced}} = \frac{I_C}{I_B} = \frac{5.36}{0.1072} = 50 < \beta_F \quad (\text{Saturation assumption is valid})$$

Lecture 9: RTL circuit : power dissipation, noise margin and fanout calculation.

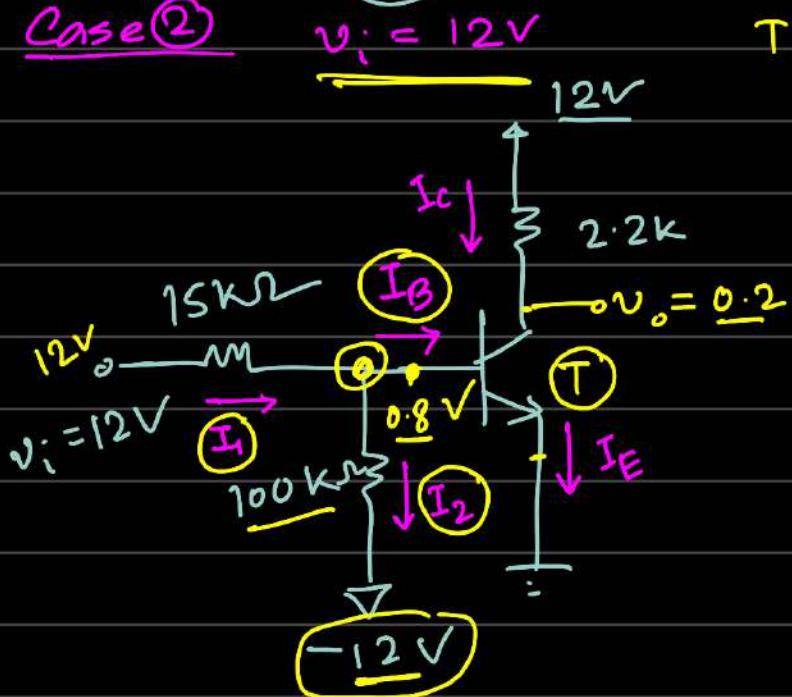
# Power dissipation for RTL inverters:





$$\begin{aligned}
 \text{Power dissipation} : P &= (0 - (-12)) \\
 &\times 0.104 \\
 &= 1.2521 \text{ mW}
 \end{aligned}$$

Case ②



T: Saturation

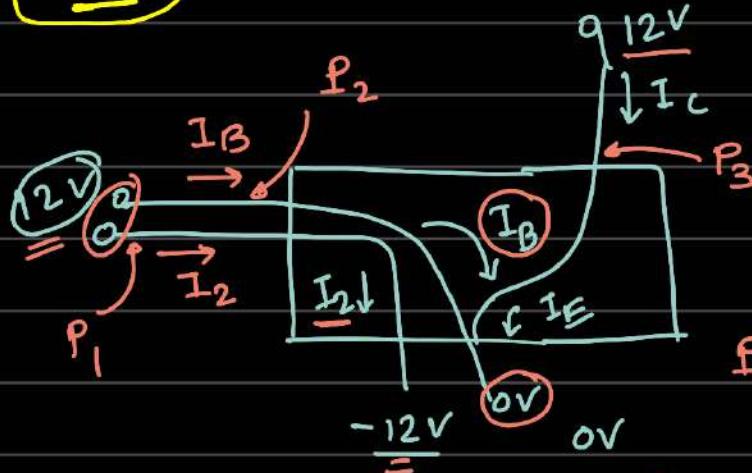
$$V_{BE} = 0.8 \text{ V}, V_{CE} = 0.2 \text{ V}$$

$$I_C = \frac{12 - 0.2}{2.2k} = 5.3636 \text{ mA}$$

$$I_I = \frac{12 - 0.8}{15k} = 0.7466 \text{ mA}$$

$$I_2 = \frac{0.8 - (-12)}{100k} = 0.128 \text{ mA}$$

$$I_B = I_I - I_2 = 0.6186 \text{ mA}$$



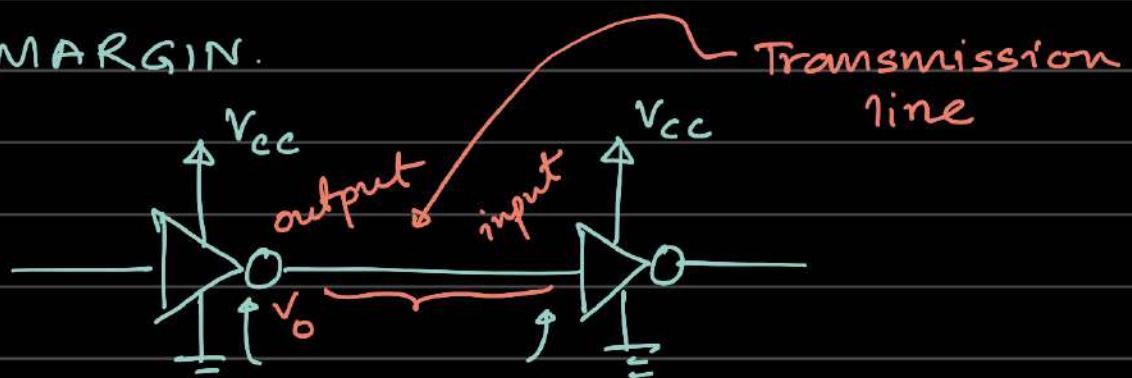
$$\begin{aligned}
 P_1 &= (12 - (-12)) \\
 &\times 0.128 \text{ mA} \\
 &= 3.072 \text{ mW}
 \end{aligned}$$

$$\begin{aligned}
 P_2 &= (12 - 0) \times 0.6186 \\
 &= 7.4323 \text{ mW}
 \end{aligned}$$

$$\begin{aligned}
 P_3 &= (12 - 0) \times 5.3636 \\
 &= 64.3632 \text{ mW}
 \end{aligned}$$

$$\text{Total Power} : P = P_1 + P_2 + P_3 = 74.8584 \text{ mW.}$$

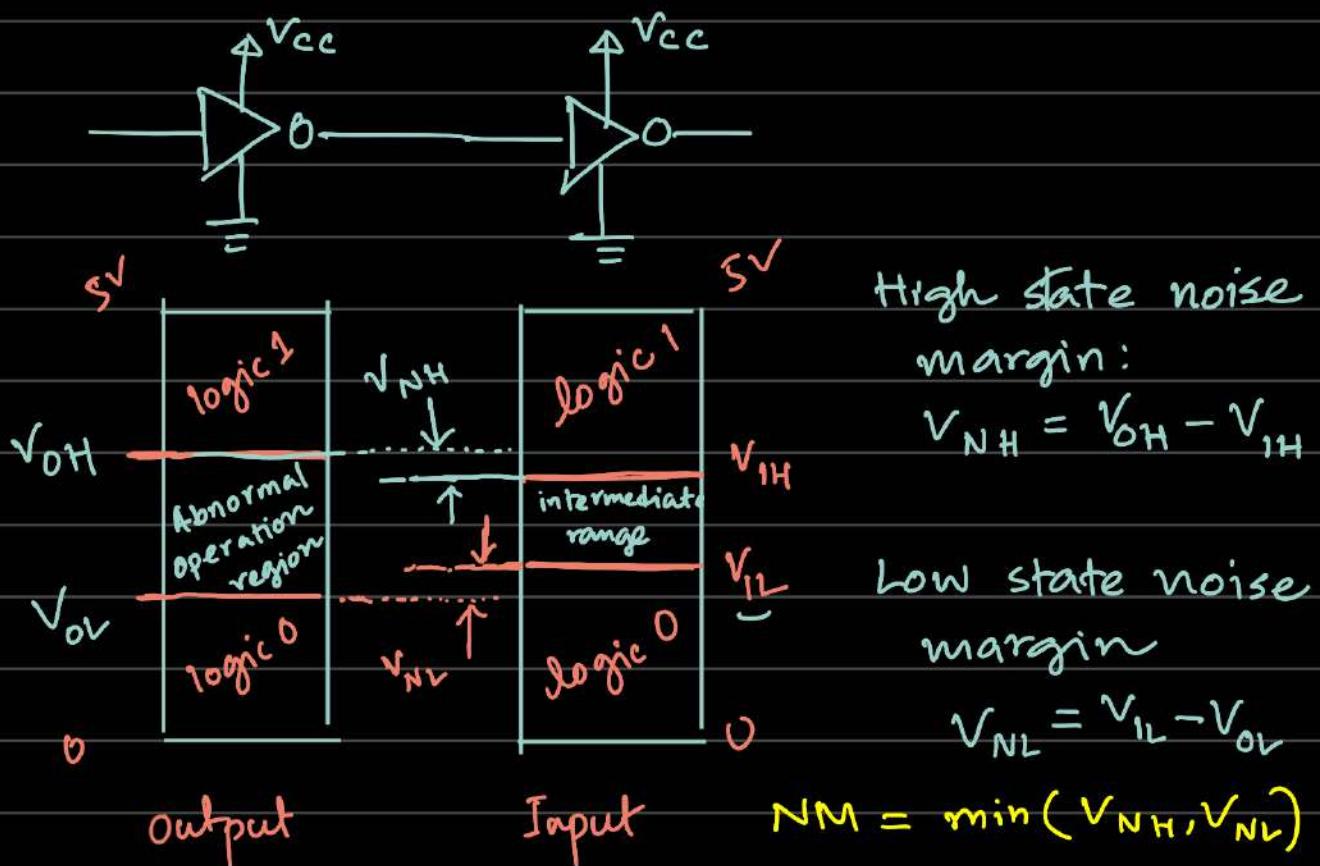
# NOISE MARGIN.



# external interference, noise can hamper

the signal transmission.

**■ NOISE MARGIN:** The maximum amount of "noise voltage" can be tolerated by a circuit while completing a successful transmission from output to input.



\*  $V_{OH}$  → The minimum voltage level at an output in the logical "1" state under defined load condition

\* VH → input

\*  $V_{OL} \rightarrow$  The maximum voltage level at an output in the logical "0" state under defined load condition.

\*  $v_{IL}$   $\rightarrow$  input

## Example

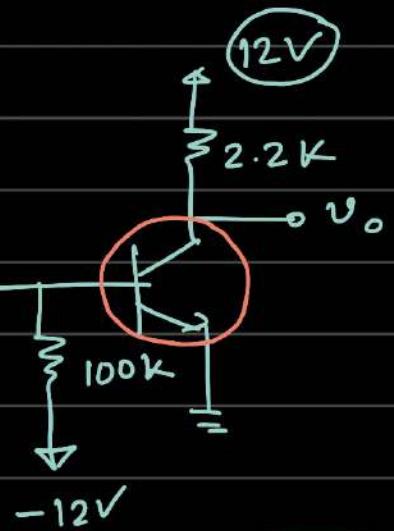
When output is low,  $V_o = 0.2V$

\*  $V_{OL} = 0.2V$  (Saturated)  $15k$  L. F.

\*  $V_{OH} = ?$  [will be given]

The output voltage might drop

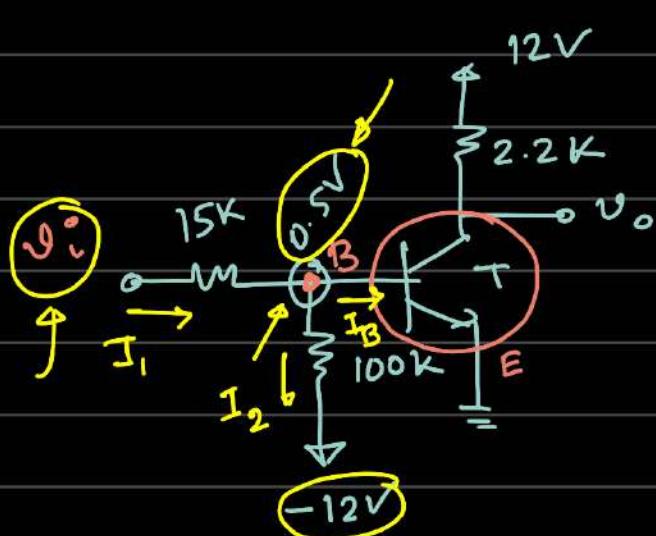
$0.5V$  from the maximum voltage.



Maximum output voltage =  $12V$ ,  $V_{OH} = 12 - 0.5 = 11.5V$

#  $V_{IL}$  calculation:

The maximum voltage we might apply so that the transistor is still turn off.



$V_{BE} = 0.5V$ , we are on the verge of turning on the transistor T.

$\Rightarrow T$ : cutoff.  $I_B = 0$ ,  $I_1 = I_2$

$$I_2 = \frac{0.5 - (-12)}{100k} = 0.125mA$$

$$I_1 = \frac{V_i - 0.5}{15k} = 0.125mA$$

$$\Rightarrow V_i = 0.5 + 15 \times 0.125$$

$$= 2.375V$$

This voltage is the maximum that we can apply to the inverter without turning on the transistor

$$V_{IL} = 2.375V$$

#  $V_{OH}$  calculation:

The minimum <sup>high</sup> voltage that we can apply to the input so that the transistor is still operating in saturation mode.

We need to apply such input voltage

that transistor T is operating on

the verge of going to saturation from forward active mode.

T  $\rightarrow$  saturation.  $V_{BE} = 0.8V$ ,  $V_{CE} = 0.2V$

$$I_c = \frac{12 - 0.2}{2.2K} = 5.3636 \text{ mA}$$

$\beta_{\text{forced}} = \frac{I_c}{I_B} \approx \beta_F$  (This will occur on the verge of going from sat. to forward active)

$$I_B = \frac{I_c}{\beta_F} = 0.1788 \text{ mA}, \quad I_2 = \frac{0.8 - (-12)}{100K} = 0.128 \text{ mA}$$

$$I_1 = I_2 + I_B = 0.3068 \text{ mA}, \quad \frac{V_i - 0.8}{15K} = I_1 = 0.3068 \text{ mA}$$

$$\Rightarrow V_i = 0.8 + 0.3068 \times 15 \\ = 5.4018V = V_{IH}$$

$$\begin{cases} V_{NH} = 11.5 - 5.4018 = 6.0982V & \leftarrow \text{high noise margin} \\ V_{NL} = 2.375 - 0.2 = 2.175V & \leftarrow \text{low noise margin} \end{cases}$$

$$\text{NOISE MARGIN : } \min(V_{NH}, V_{NL}) \\ = \underline{2.175V} \leftarrow$$

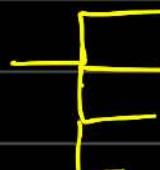
# This noise voltage can be tolerated for both input and output voltages.

FANOUT: The maximum number of logic inputs (of the same logic family) that an output can drive reliably is called maximum fanout.

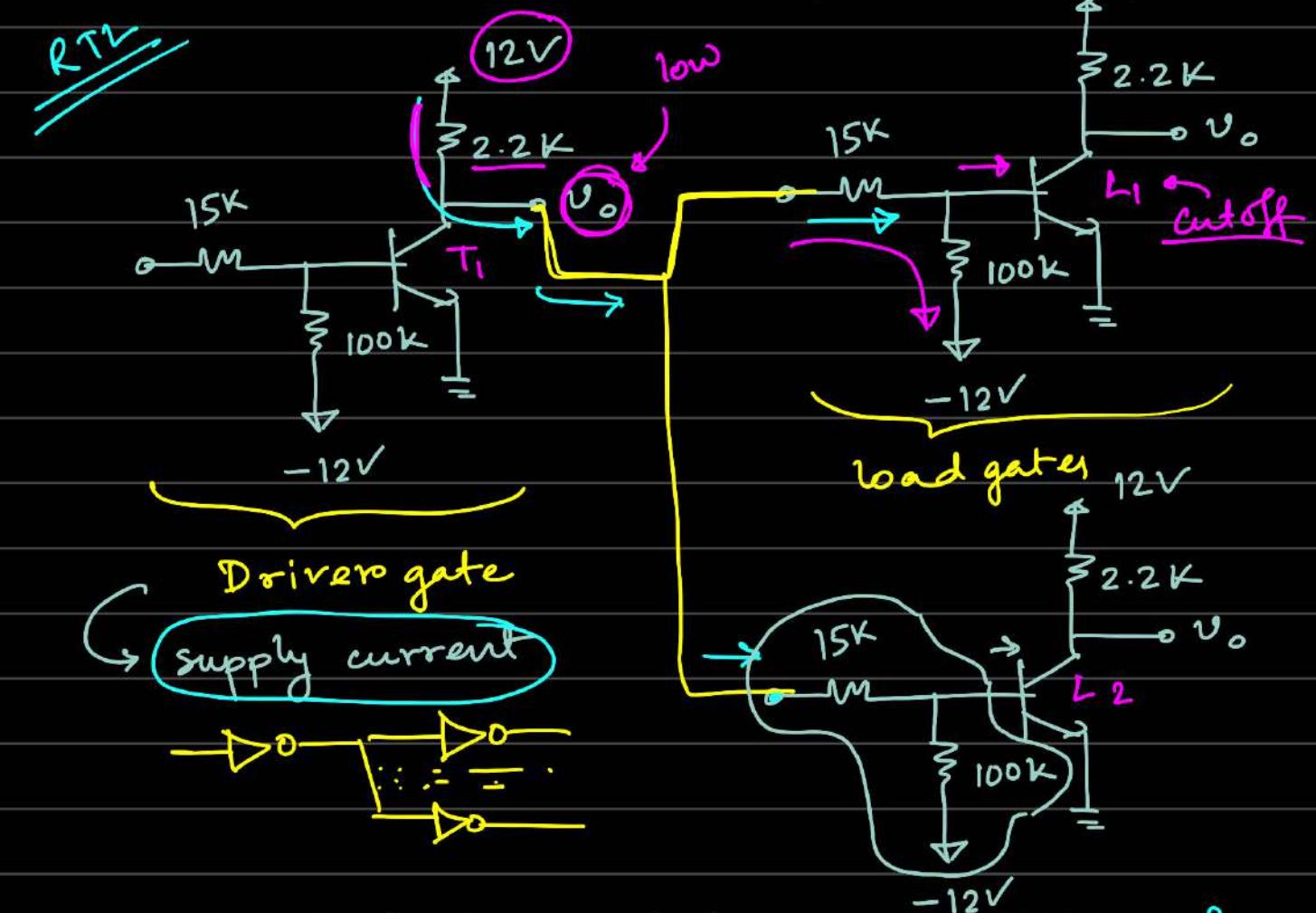
calculate

\* fanout  $\rightarrow$  maximum fanout

\* fanout = 5  $\leftarrow$  not "maximum"



Example: Calculate the fanout of this RTL circuit. Assume  $V_{OH} = 10V$ .



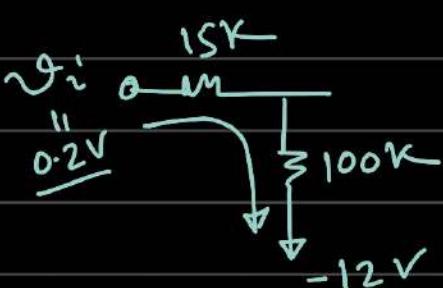
- # individual demand (current) from each load circuit/gate.
- # the maximum current that can be supplied from driver circuit.

Case (1): When output voltage at the driver is 10V.  
 $V_{OL} = 0.2V$

$$* \text{ Maximum total supply} = \frac{12 - 0.2}{2.2k} = 5.3636 \text{ mA}$$

$$* \text{ individual load current demand} = \frac{0.2 - (-12)}{115k}$$

(in this case load circuit's transistors are in cutoff mode) = 0.106mA

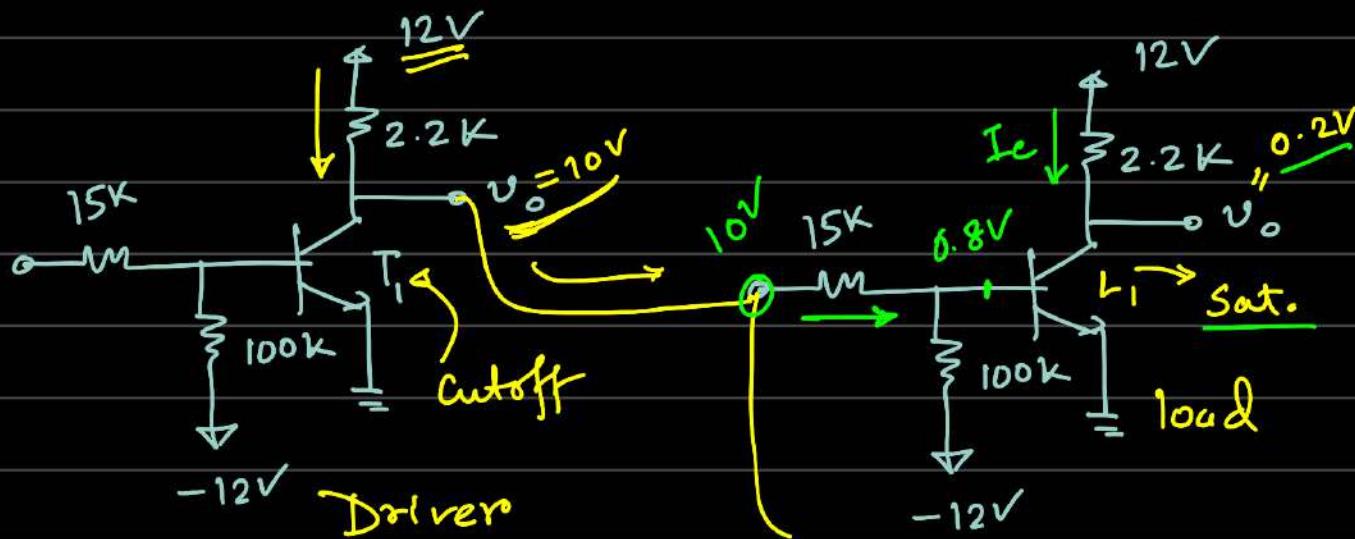


maximum number of load circuits that we can afford, fanout

$$= \left\lfloor \frac{5.3636}{0.106} \right\rfloor = \left\lfloor 50.6 \right\rfloor = 50 \leftarrow \text{floor } f^n$$

Case ② : When output voltage of the driver circuit is high.  $V_{OH} = 10V$ .

\* Maximum supply current =  $\frac{12-10}{2.2K} = 0.909mA$



Load transistors are in saturation mode in this case.  $V_{BE} = 0.8V$ ,  $V_{CE} = 0.2V$

\* Driver transistor,  $T_1 \rightarrow$  cutoff, load circuit's transistors  $T_1 \downarrow$  Sat.

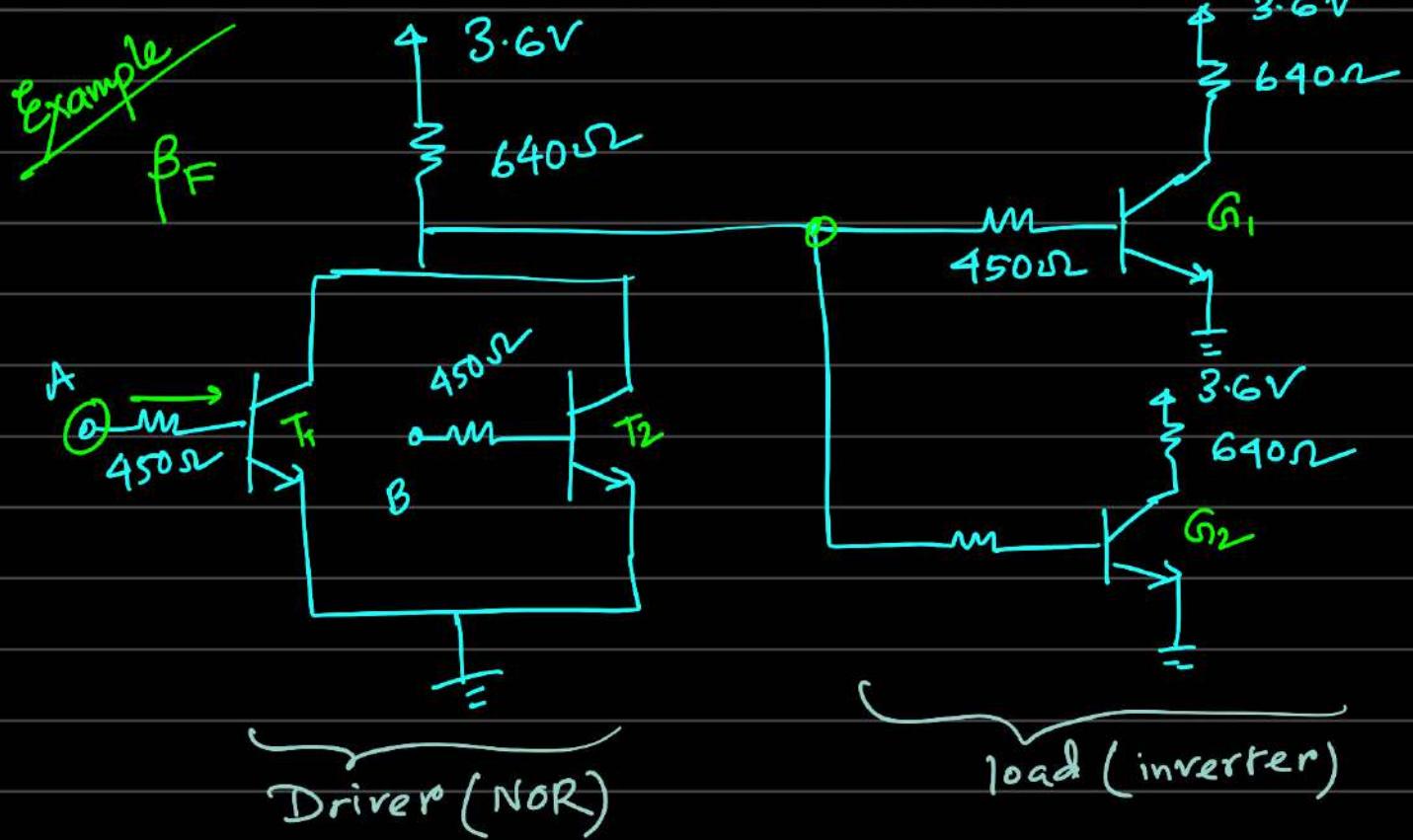
\* Maximum supply current =  $\frac{12-10}{2.2K \cdot 2} = 0.909mA$  Sat.

\* Individual load current,  $I_L = \frac{10-0.8}{15K} = 0.6133mA$

\* Maximum fanout for this case.  $= \left\lfloor \frac{0.909}{0.6133} \right\rfloor = \lfloor 1.48 \rfloor = 1$

④ Overall maximum fanout must be calculated by considering worst case scenario. To prevent malfunction of driver circuit, we need to take the minimum of the two cases.

④ Maximum fanout,  $= \min(50, 1) = 1$



\* There would be resistors connected to input terminal and the resistor is connected to the transistor. (RTL circuit)

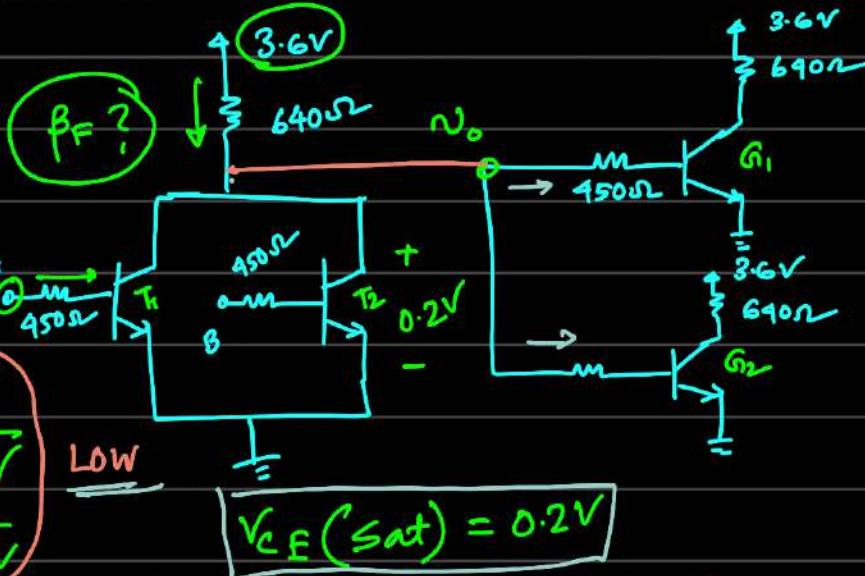
\* If the input voltage  $V_A$  is high, you can assume switching transistor is operating in saturation, or if the input voltage is low, transistor is operating in cutoff mode.

\* Question: If the number of fanout is 5. Find the (minimum) value of  $\beta_F$ , so that these circuits operate as NOR gate. Assume all transistors have same value of  $\beta$ .

# Lecture 5 : INTRODUCTION TO DTL CIRCUIT

## RTL NOR GATE :

A	B	T <sub>1</sub>	T <sub>2</sub>	V <sub>o</sub>
3.6	3.6	S	S	0.2V
3.6	0V	S	C	0.2V
0V	3.6	C	S	0.2V
0V	0V	C	C	3.6V



↑ WITHOUT CONNECTING TO THE LOAD CIRCUITS

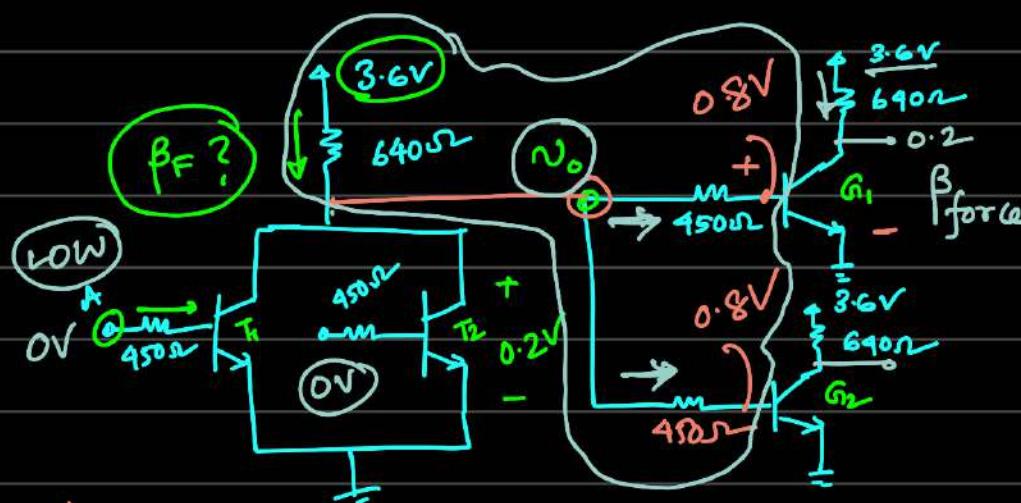
\* If we add load circuits, then for low voltage output at the driver output terminal would not change because it is determined from  $V_{CE}(\text{saturation}) = 0.2V$ .

\* If we add load circuits for high voltage driver output, load circuits will draw current thus reduce the voltage high output.

④ T<sub>1</sub> and T<sub>2</sub> both are in cutoff.

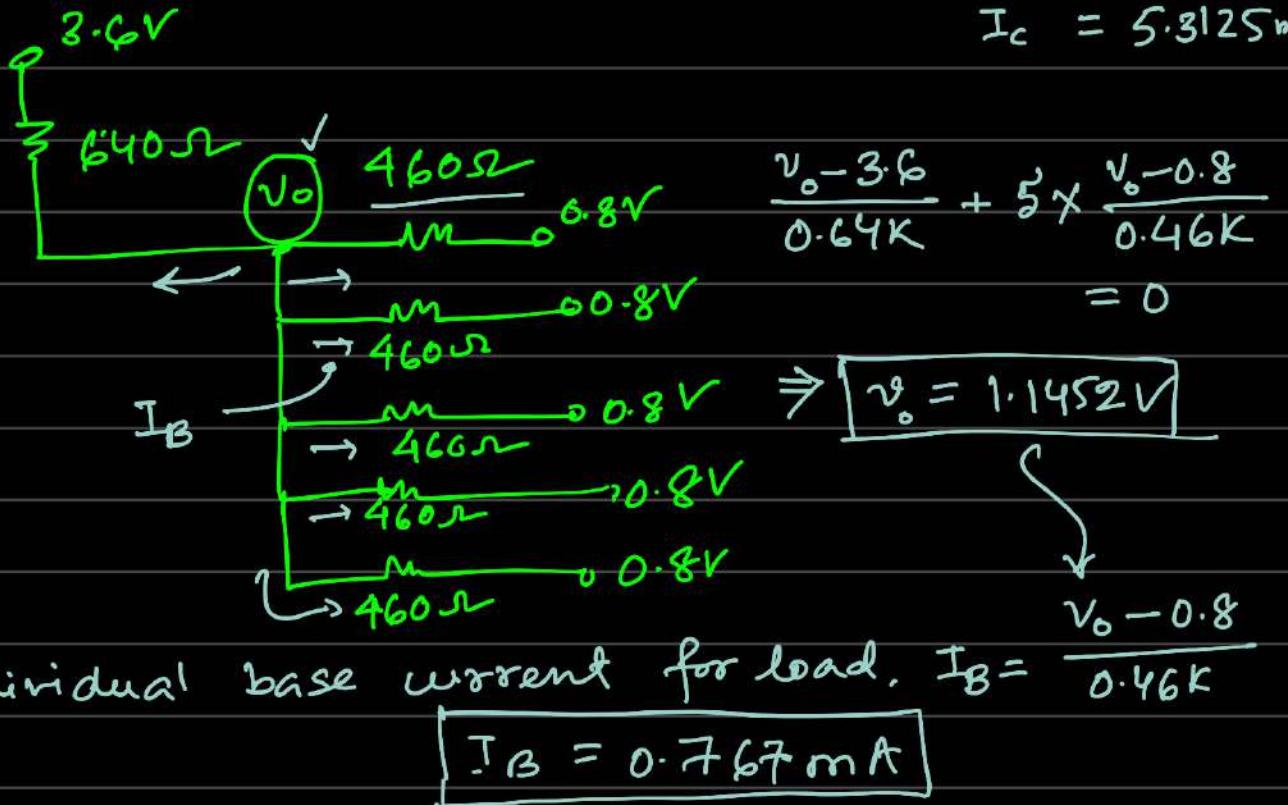
④ FANOUT = 5

④ All the load circuits would be in saturation mode.  $V_{BE}(\text{sat.}) = 0.8V$



\* Collector current in load circuits.  $I_c = \frac{3.6 - 0.2}{0.64K}$

$$I_c = 5.3125 \text{ mA}$$



individual base current for load.  $I_B = \frac{v_o - 0.8}{0.46K}$

$$I_B = 0.767 \text{ mA}$$

$$\therefore \beta_{\text{forced}} = \frac{I_c}{I_B} (\text{load}) = \frac{53125}{0.767} = 6.9263$$

# Load circuits will remain in saturation if their  $\beta_F \geq \beta_{\text{forced}}$ .

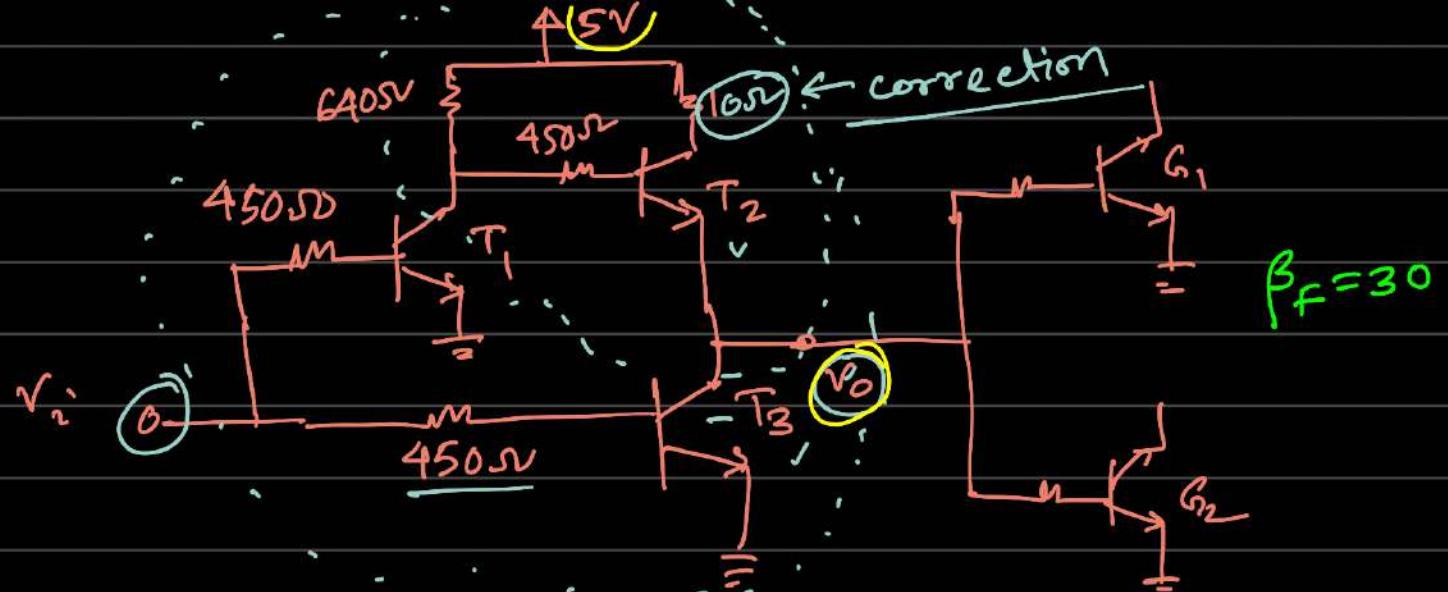
# Load circuits must have  $\beta_F$  at least equal to  $\beta_{\text{forced}} = 6.92693$  or greater than this value to maintain correct operating mode.

# Thus.  $\beta_{\text{min}} = \beta_{\text{forced}} = 6.92693$

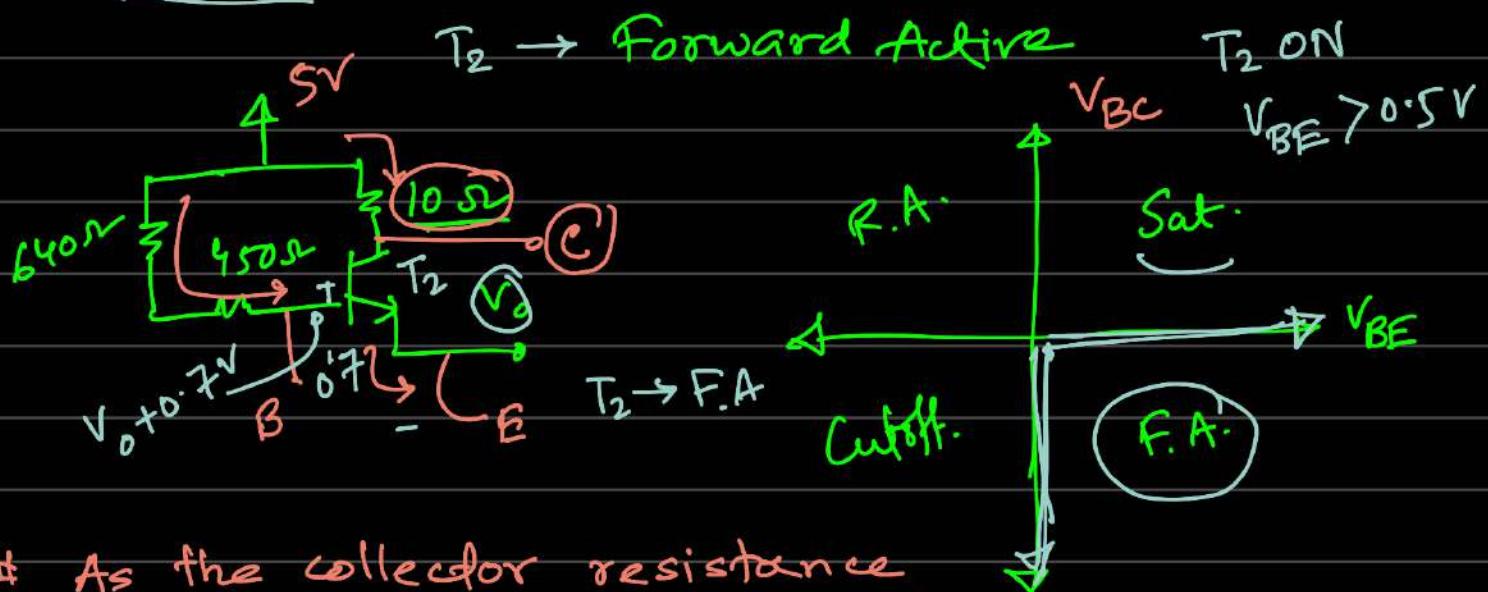
Homework 2.5 (Quiz/Mid Exam)

Remarks : This circuit boosts the value of maximum FANOUT for regular RTL inverters.

Buffer circuit.



~~hints.~~ 
$$v_i = 0V, T_3 \rightarrow \text{cutoff}, T_1 \rightarrow \text{cutoff mode}$$



# As the collector resistance ↓ is very small then collector voltage would be close to 5V.

However, base voltage will not be that higher.

$$\text{so } v_c > v_B \Rightarrow v_B - v_c < 0 \Rightarrow v_{BC} < 0$$

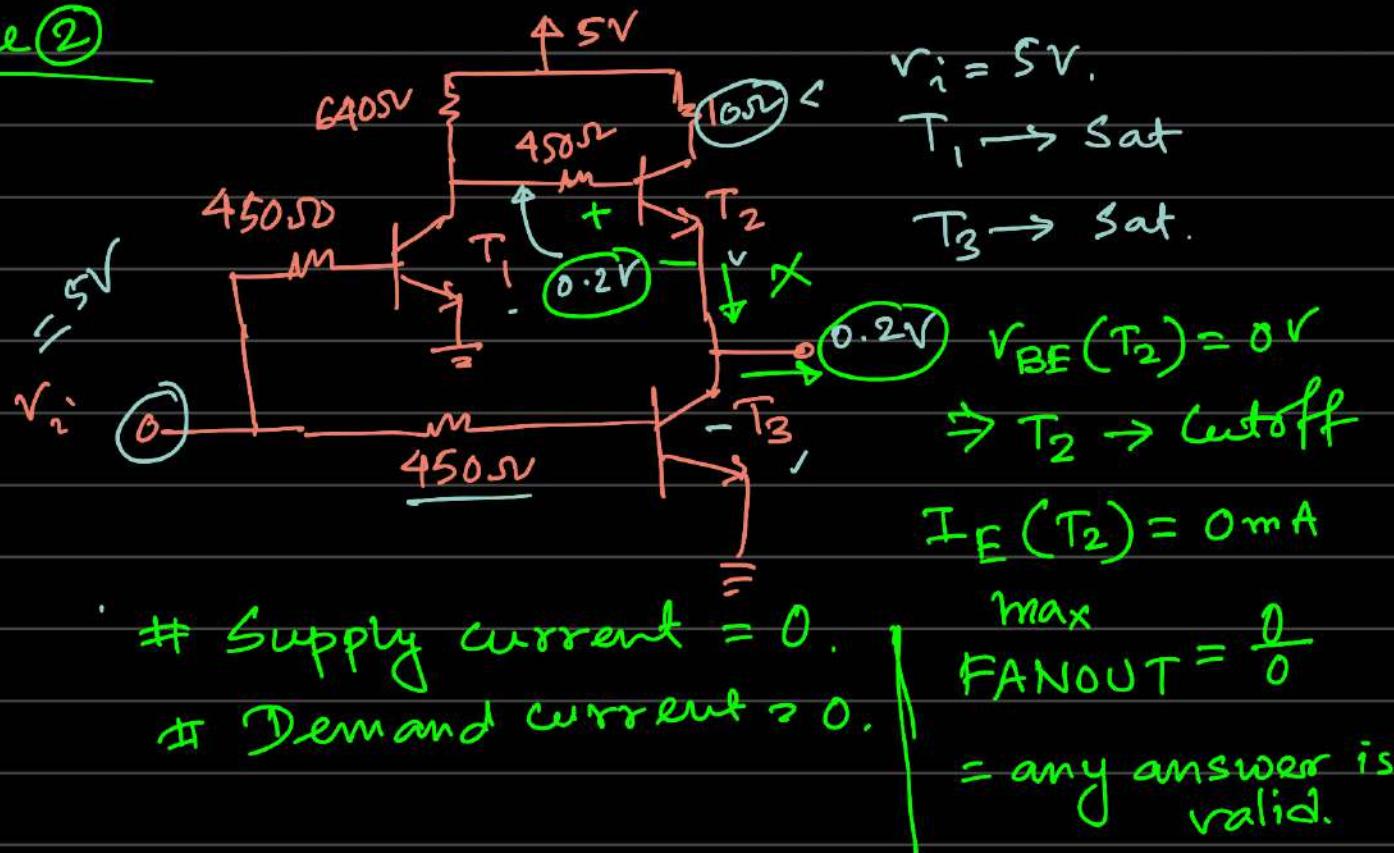
∴ Therefore,  $T_2$  might be operating in forward active mode.

$$\# \quad I_B = \beta_F I_C, \quad I_E = (I_B + I_C) = (\beta + 1) I_B$$

$$I_B = \frac{5 - (V_0 + 0.7)}{640 + 450}, \quad I_E = (\beta + 1)I_B = \text{supply current.}$$

... (Do it yourself) ✓

## Case 2

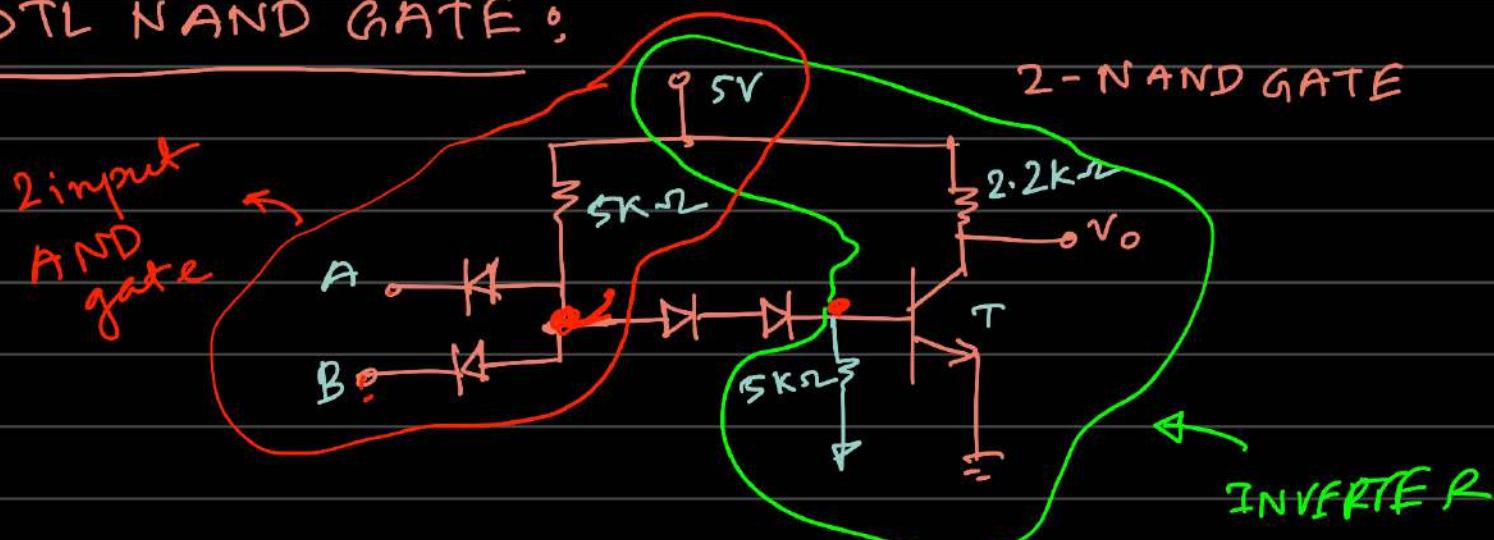


## # DTL (Diode Transistor Logic)

\* Bipolar  $\rightarrow$  Saturated (switching) transistor will be operating in cutoff or saturation.

\* [Input terminals connected through diodes to the transistor's base terminal. switching]

## DTL NAND GATE:



## BASIC OPERATION:



This is the basic structure.

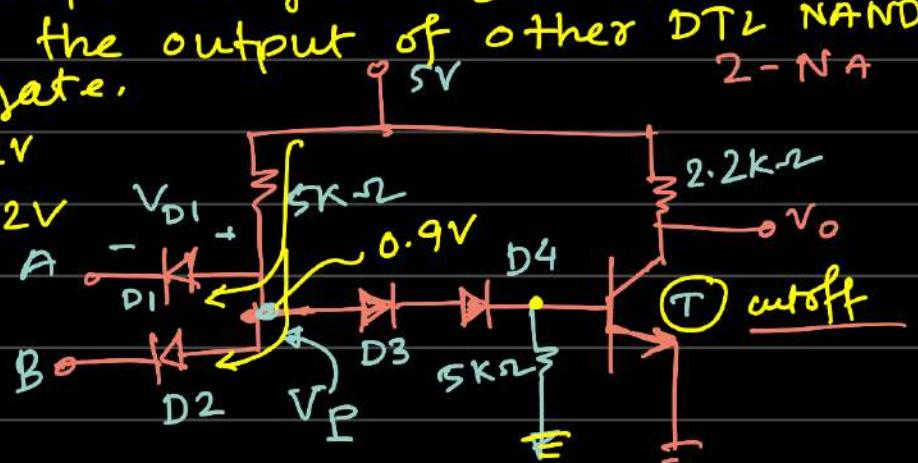
# Calculate the currents and node voltages for the following DTL gate. Verify it is a NAND gate. Input stages might be

Ans: Connected to the output of other DTL NAND gate.  $Q_{SV}$   $2-NA$

Case ①.  $V_A = \text{low} = 0.2V$

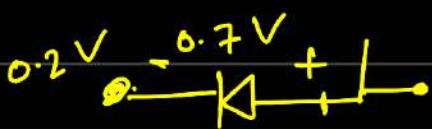
Case ①.  $V_A = \text{low} = 0.2V$   
 $V_B = \text{low} = 0.2V$

Assume, L  
the anode voltage  
 $V_p$  might be higher



than the cathode voltages of  $D_1$  and  $D_2$  diode.

So,  $D_1$  and  $D_2$  are conducting. Thus.  $V_{D_1} = 0.7V$



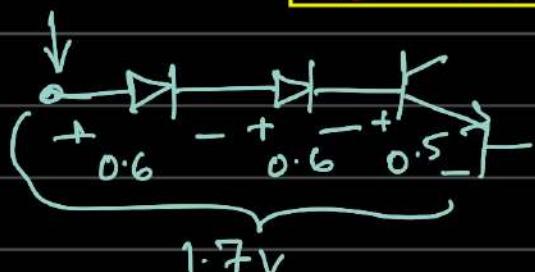
Therefore, according to the assumption  $V_p = 0.2 + 0.7 = 0.9V$

④ In order for T transistor to turn on

We need to have  $V_{BE} \approx 0.5V$  (cut-in voltage of

transistors), we also need to have  $V_{D3} = V_{D4} \approx 0.6V$  (cut-in voltage for diodes). As a total we

require  $V_{D3} + V_{D4} + V_{BE} \approx 1.7V$  at P node to



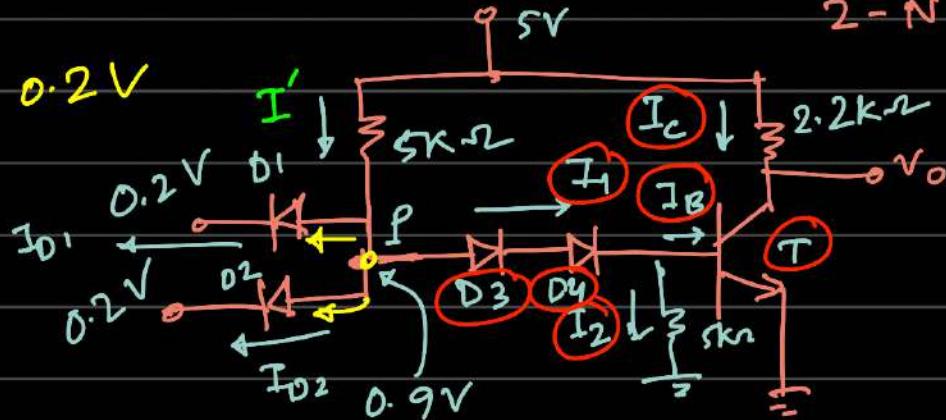
turn on the right side of the circuit.

If  $V_p = 0.9V$ , then T could not turn on. This justifies our assumption.

Now we can calculate the current and voltages.

Case ①

$$V_A = V_B = 0.2V$$

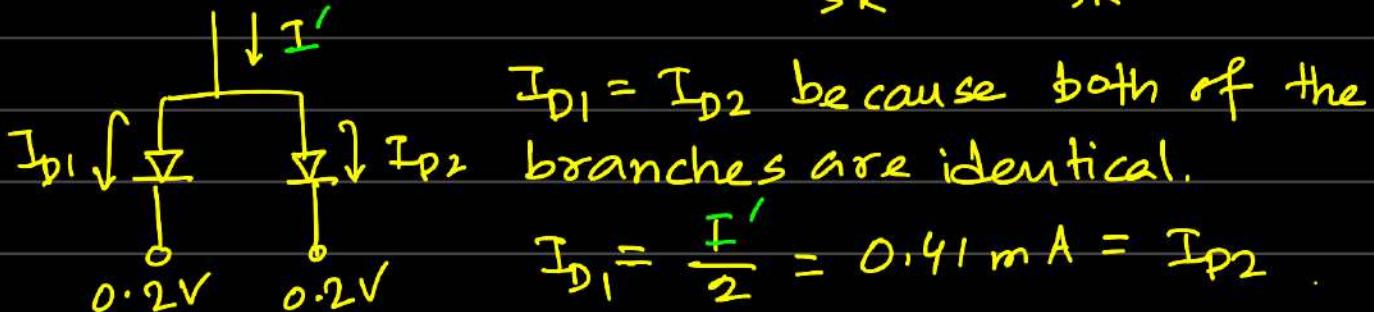


2-NA

$T \rightarrow \text{on}$ .  $D1, D2 \rightarrow \text{conducting}$ .  $D3, D4 \rightarrow \text{off}$

$$V_p = 0.9V. \quad I_c = I_B = 0. \Rightarrow V_o = 5V$$

$$I_1 = 0, I_2 = 0, \quad I' = \frac{5 - 0.9}{5K\Omega} = \frac{4.1}{5K} = 0.82mA$$



$$\begin{array}{c} \text{Case ②} \\ \begin{array}{c|c} V_A = 0.2V & V_B = 0.2V \\ \hline V_B = 5V & V_A = 5V \end{array} \end{array} \quad \text{Similarly.}$$

Assume,  $D1$  is conducting and  $D2$  is off.

This implies.

$$V_p = 0.9V$$

# we need at least  $V_p \geq 1.7V$  to turn on  $T$

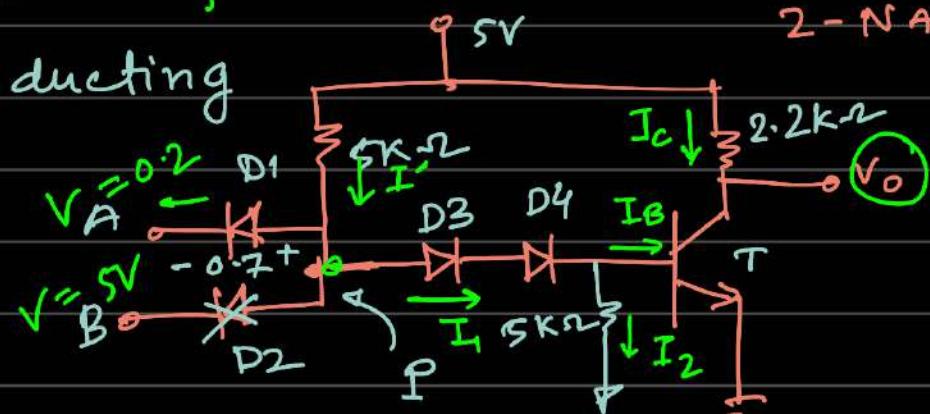
transistor. It again justifies our assumption

#

$$I_c = I_B = I_1 = I_2 = 0mA,$$

$$I' = 0.82mA$$

$$I_{D2} = 0mA, \quad I_{D1} = 0.82mA, \quad V_o = 5V, \quad V_B = 0V$$



2-NA

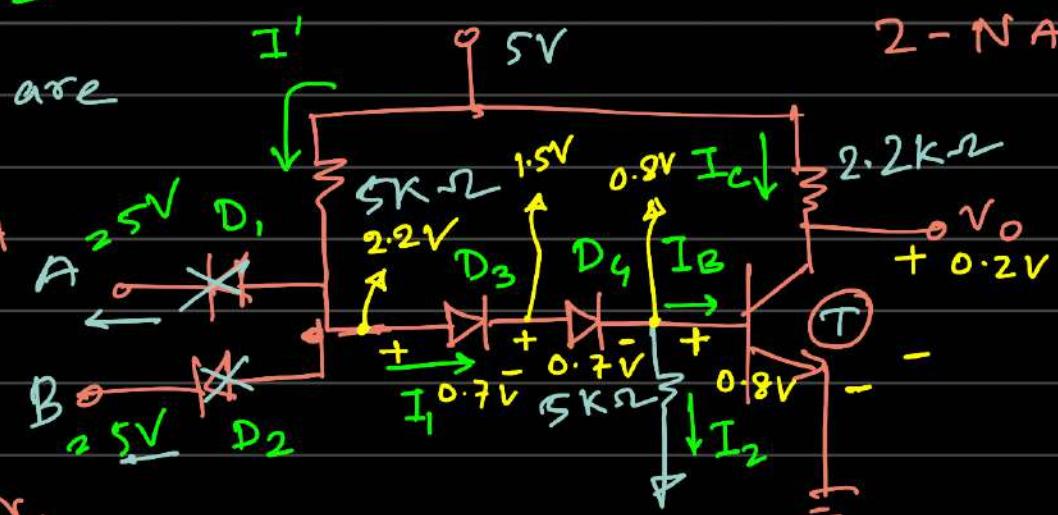
Case 3  $V_A = V_B = 5V$

Assume  $D_1, D_2$  are off.

$$I_{D1} = I_{D2} = 0 \text{ mA}$$

Therefore,

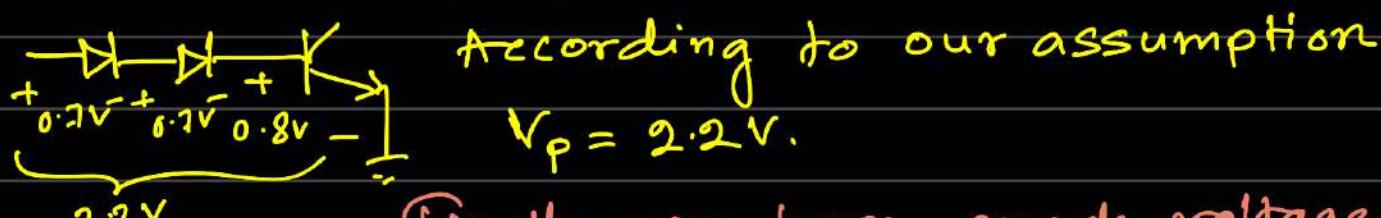
$D_3, D_4$  and



T must be ON.

Because it is a DTL circuit. The switching transistor must operate in saturation mode when it is turned on.  $V_{CE} = 0.2V$ ,  $V_{BE} = 0.8V$

$$V_{D3} = V_{D4} = \underline{0.7V} \quad [\text{Conduction voltage of diode}]$$



According to our assumption  
 $V_P = 2.2V$ .  
 Finally we have anode voltage of  $D_1$  and  $D_2$  is smaller than cathode voltage. This justifies our assumption.

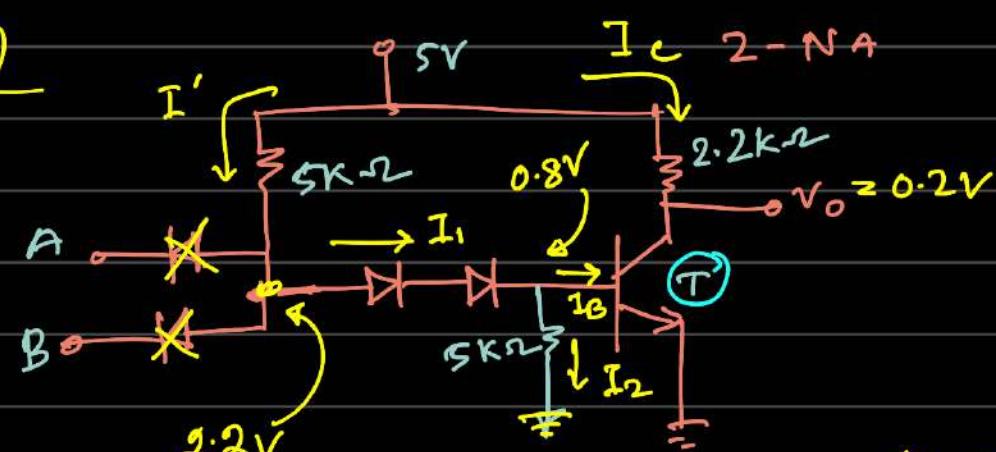
# Current calculation :-

$$I' = \frac{(5 - 2.2)}{5k} = 0.56 \text{ mA}$$

$$I_1 = 0.56 \text{ mA}$$

$$I_2 = \frac{0.8 - 0}{5k} = 0.16 \text{ mA}$$

$$I_B = I_1 - I_2 = 0.4 \text{ mA}, \quad I_C = \frac{5 - 0.2}{2.2} = 2.182 \text{ mA}$$



From analyzing the cases we can clearly conclude this circuit is a NAND gate.

Lecture 6: DTL Noise margin, Fanout and modified DTL and HTL circuits.

$\beta_{min}$  = the minimum value of  $\beta_F$  of the switching transistor T, that will keep the circuit operation error free.

# Case ① and ② will not help us to determine the  $\beta_{min}$ , because in both of those cases transistor is turn off.

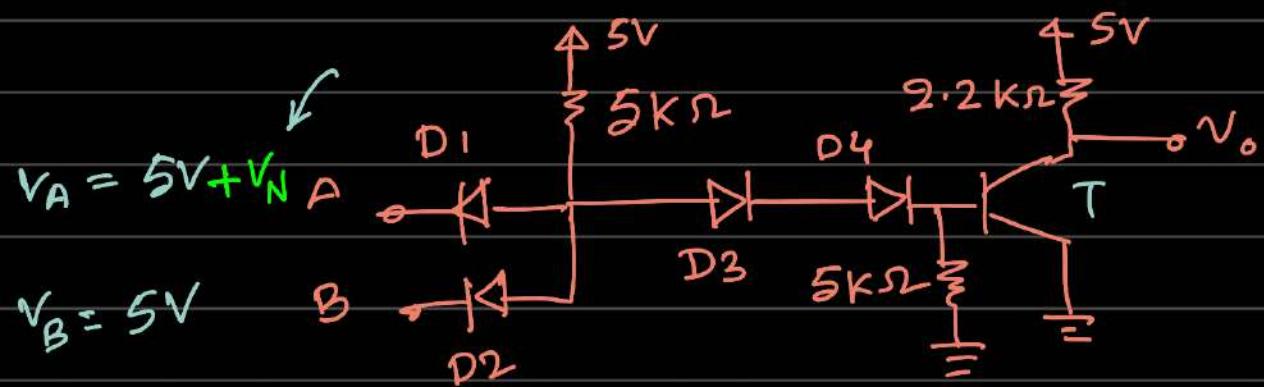
However, for case ③, transistor is on and operates in saturation mode. Therefore, to maintain correct operating we must choose a value of  $\beta_F$  that is higher than  $\beta_{forced}$ .

minimum value allowed for  $\beta_F = \beta_{forced} = \beta_{min}$

$$\beta_{min} = \frac{I_c}{I_B} (\text{sat}) = \frac{2.182}{0.4} = 5.46$$

Noise margin Calculation:

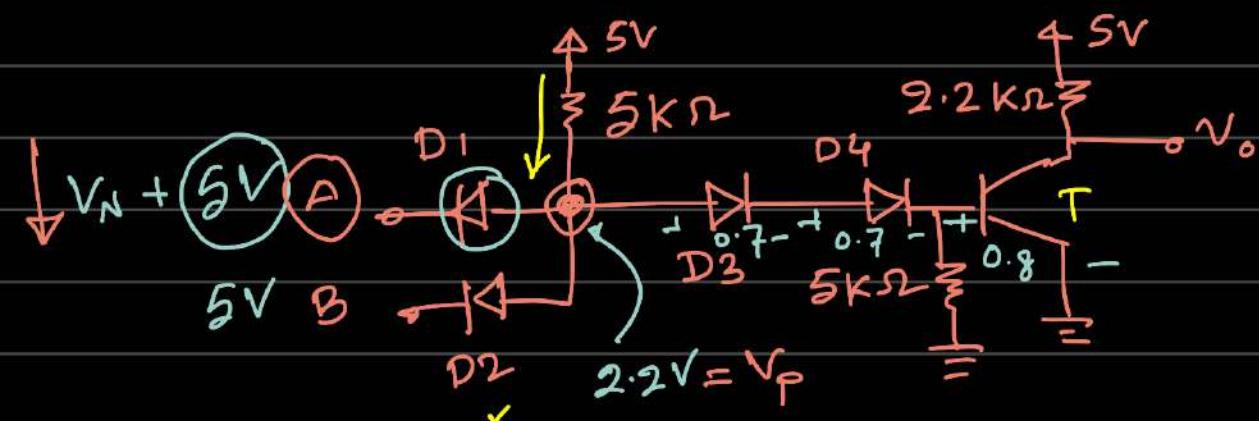
\* NM calculation for DTL is not similar to the RTL circuit.



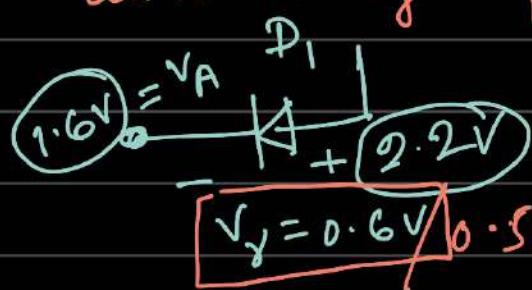
Q5: If all the inputs are high, what is the magnitude of noise voltage which will cause the gate to malfunction?

Noise voltage can be positive or negative

# If D1 and D2 start conducting, they will have precedence over D3, D4 and T because of lower resistance at that direction.



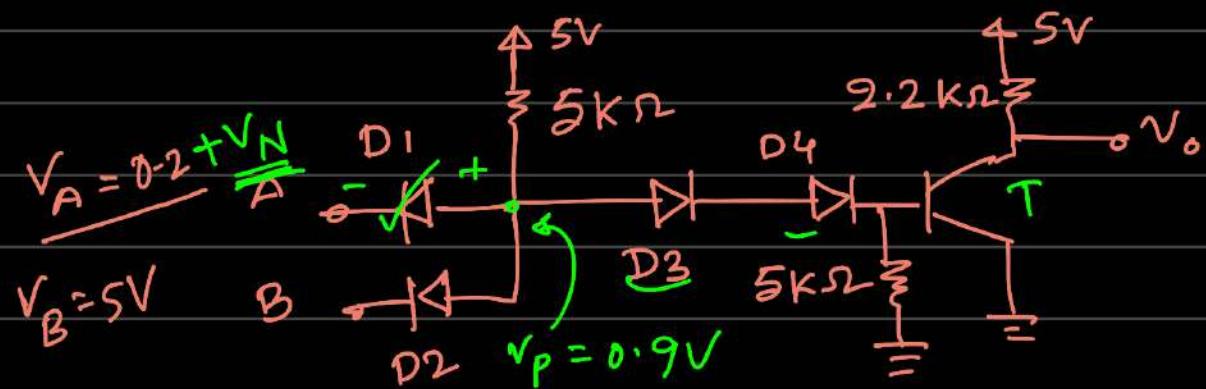
# So the circuit will malfunction when the voltage difference  $V_A$  and  $V_P$  is equal to cut-in voltage of diode.



If  $r_p = 1.6V$ , then anode voltage of D1 will have enough voltage to start conducting. Hence, circuit will malfunction.

$$V_N + 5 = 1.6 \Rightarrow V_N = -3.4V, \quad V_N = |3.4|V = 3.4V = V_{NH}$$

Q: If one of the inputs is low and others are high, then what magnitude of noise voltage at low input terminal will cause the transistor to malfunction?



# Valid operation: Case②.  $D_1$  on,  $D_2$ ,  $D_3$ ,  $D_4$ ,  $T$  off.

# The circuit will malfunction if  $D_3, D_4$  and T start conducting or turned on.

\* As long as  $D_1$  is on any increment in noise voltage at node A will also increase the voltage at  $V_P$ . Because, the difference between anode and cathode terminal should be  $0.7V$  for conducting diode  $D_1$ .

# If we increase  $V_P$  upto 1.7V, then P3, P4 and T will turn on.

$$V_P + V_N = 1.7 \Rightarrow V_N = 1.7 - 0.9 = 0.8 \text{ V}$$

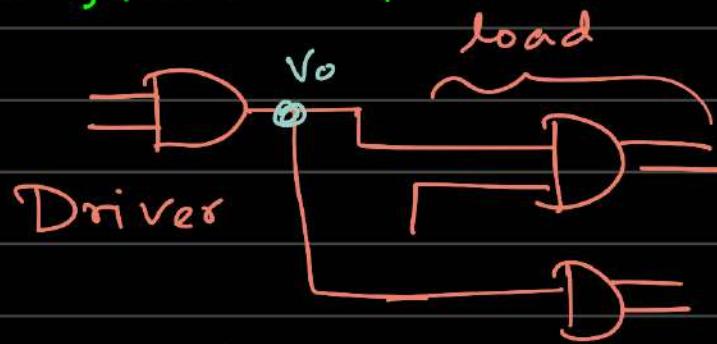
Low noise margin =  $0.8V$ .

Finally, total noise margin,  $NM = \min(NM_L, NM_F)$   
 $= \min(0.8, 3.4)$

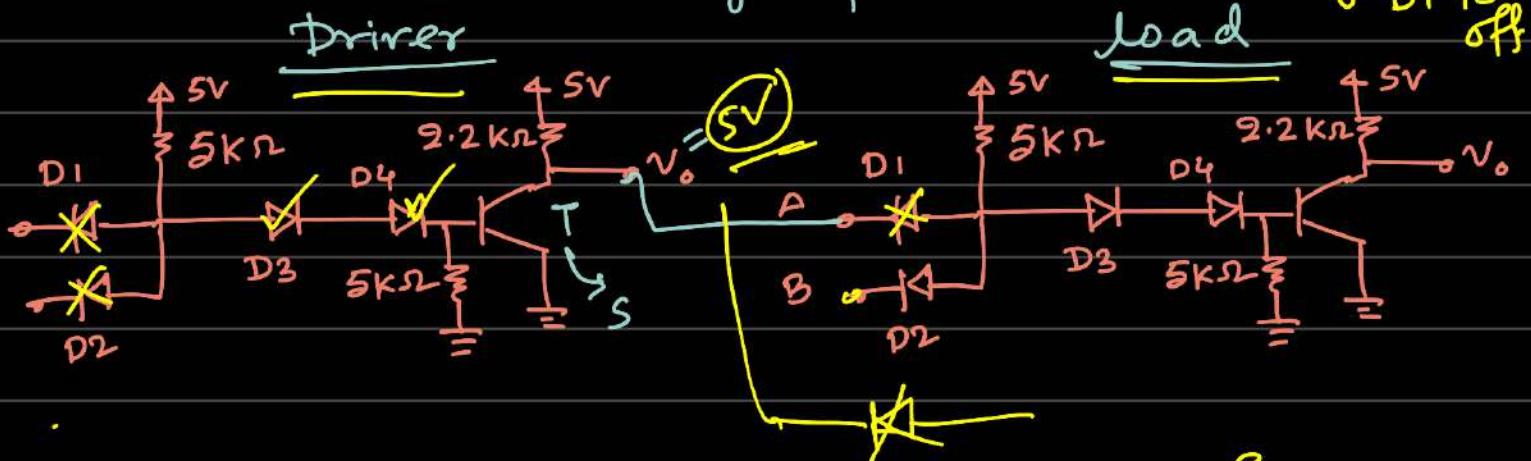
$$NM = 0.8 V$$

## Fanout Calculation:

② Different from RTL.



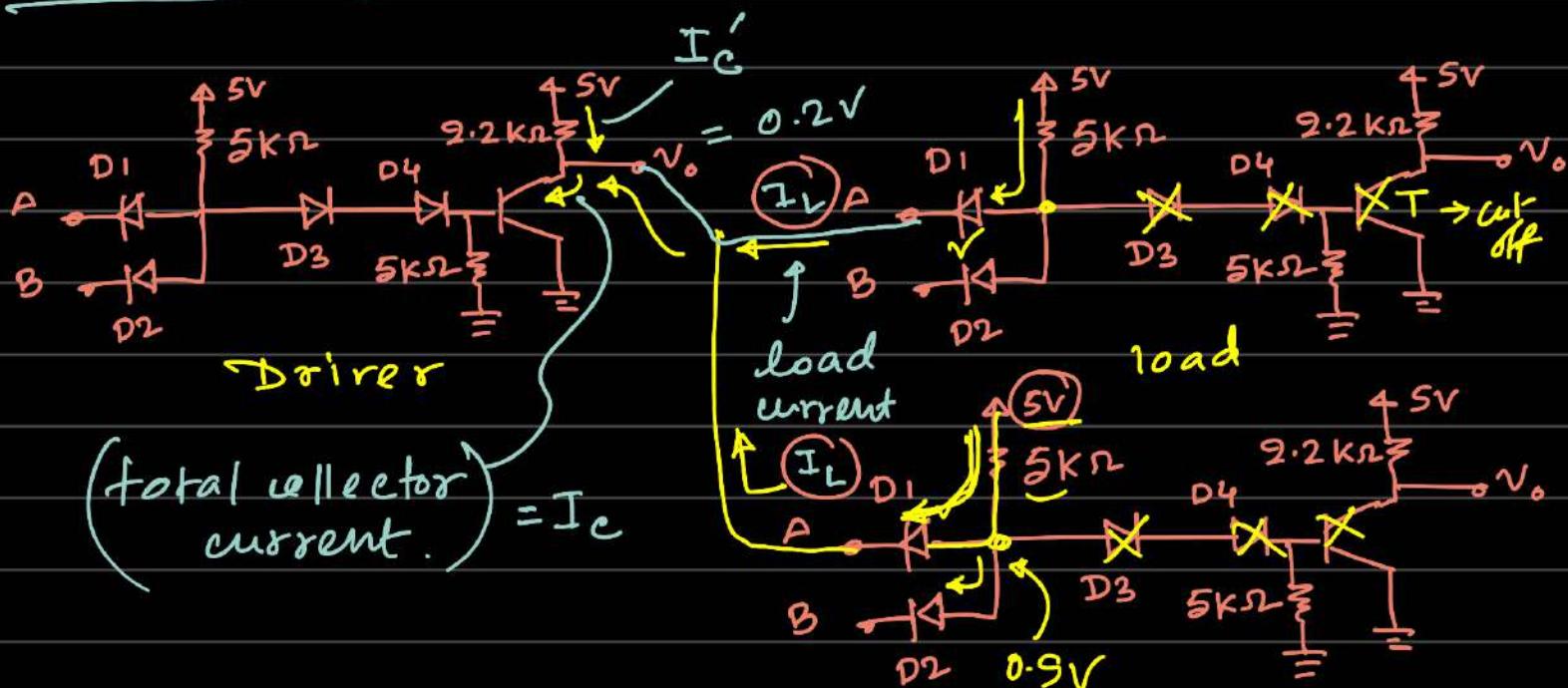
Case ① Output voltage of drivers is high, load  $D_1$  is off.



If  $V_o = 5V$ , then the demand current of the load circuit is zero. Therefore, we can connect as many load circuit as we wish for this case.

$$\text{maximum Fanout} = \infty$$

Case ②  $V_o = 0.2V$



individual load circuit delivers  $I_L$  current.

$I_L$  = standard load

$I_c'$  = no-load collector current

$I_c$  = total collector current.

If the number of fanout =  $N$ ,

total collector current  $I_c = I_c' + N I_L$

Constraint: Since the transistor T in driver circuit in saturation mode, the collector current can not cross a certain value.

That will push the transistor T from saturation to forward active mode.

~~⊗~~  $\beta_{\text{forced}} > \beta_F$  [Not in saturation]

①  $\beta_{\text{forced}} \approx \beta_F$  (Edge of sat. and F.A.).

$$I_{c,\max} = \beta_F \times I_B \quad \left[ \beta_{\text{forced}} \approx \frac{I_c}{I_B} \leq \beta_F \right]$$
$$= 30 \times 0.4 \quad I_c' = 2.182 \text{ mA}$$
$$= 12 \text{ mA}$$

$$I_{c,\max} = I_c' + N \times I_L \quad \left[ N = \max_{\text{fanout}} \right]$$

Standard load,  $\frac{5-0.9}{5 \text{ k}\Omega} = 0.82 \text{ mA}$

$$12 = 2.182 + N \times 0.82$$

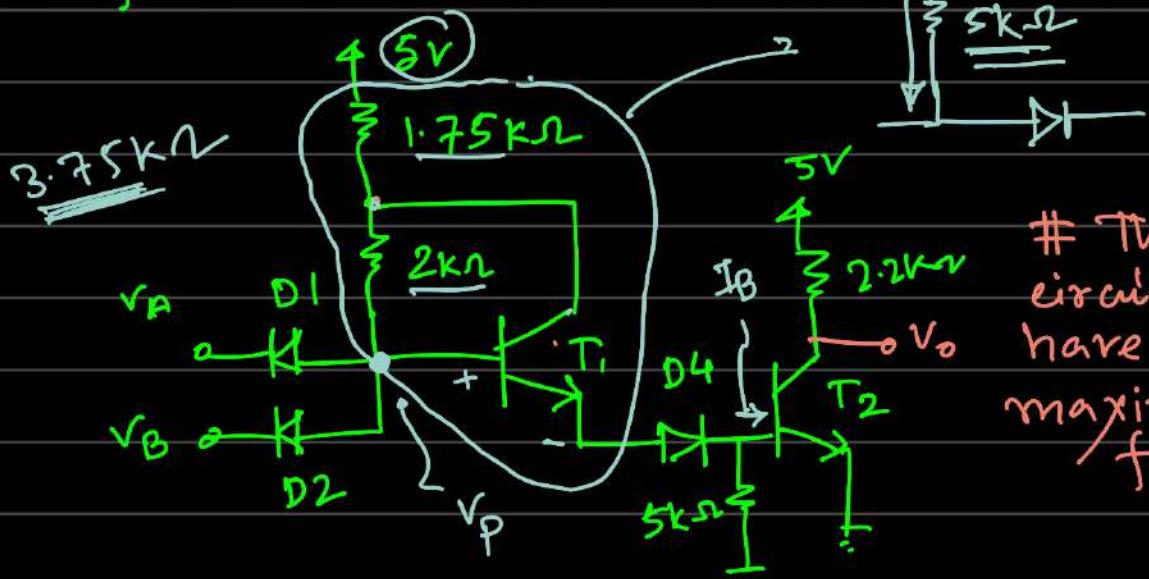
$$\Rightarrow N = 11.97 \approx \cancel{12}$$

We can not choose 12, because in that case collector current will overflow and make Transistor T to operate in F.A.

So maximum fanout  $\lfloor 11.97 \rfloor = 11$

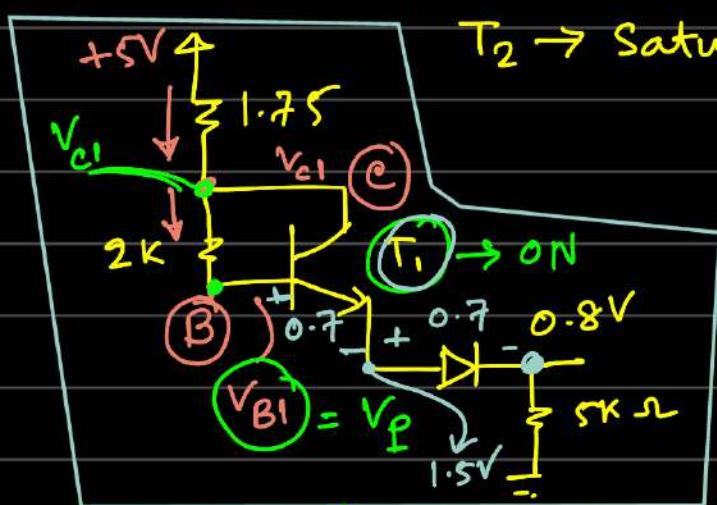
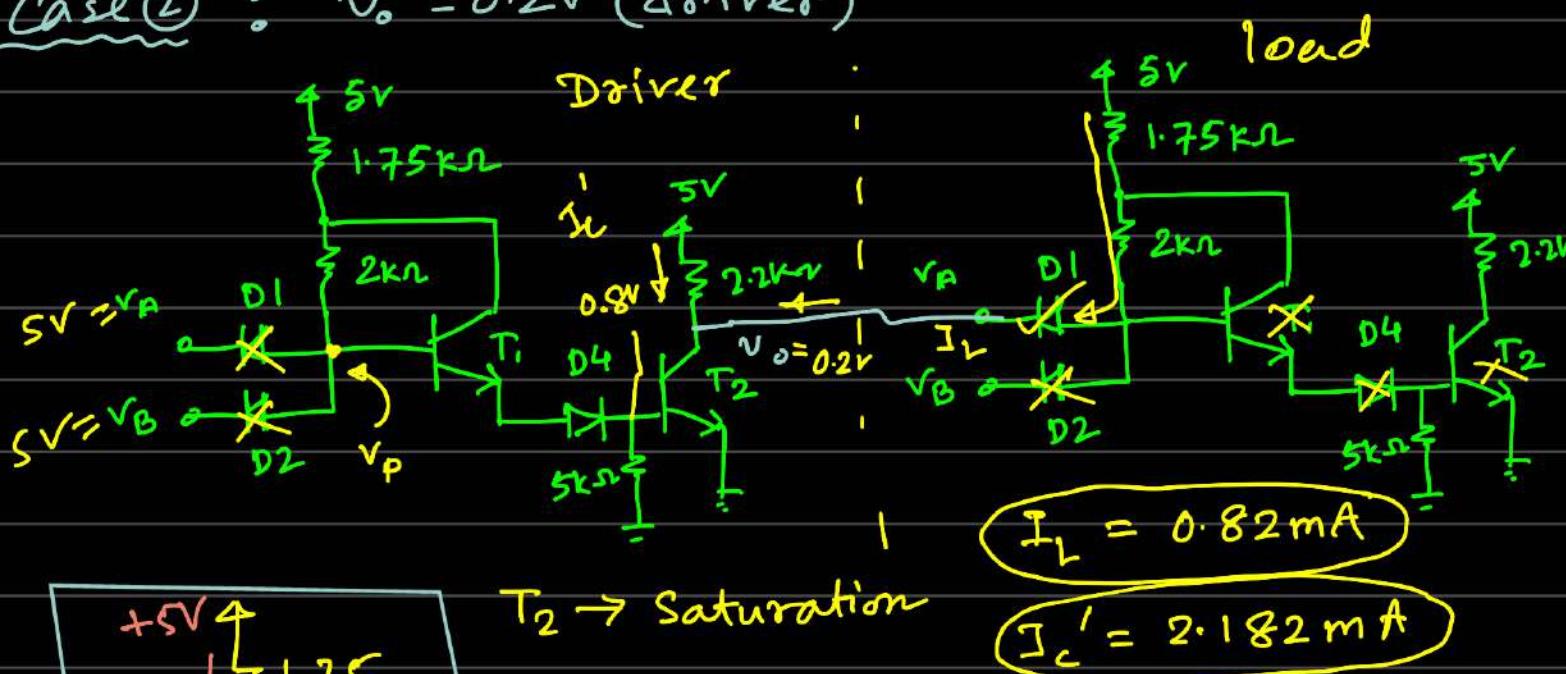
Finally, maximum fanout,  $\min(11, \infty)$   
 $= 11$ .

# Modified DTL circuit. :



Case ①: Trivial.  $V_o = 5V$  (driver circuit). Fanout =  $\infty$ .

Case ② :  $V_o = 0.2V$  (driver)



# Current will flow from higher voltage to lower voltage.

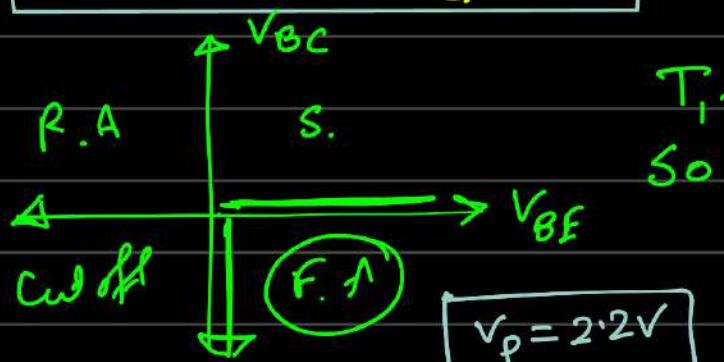
Therefore.  $V_{C1} > V_{B1}$

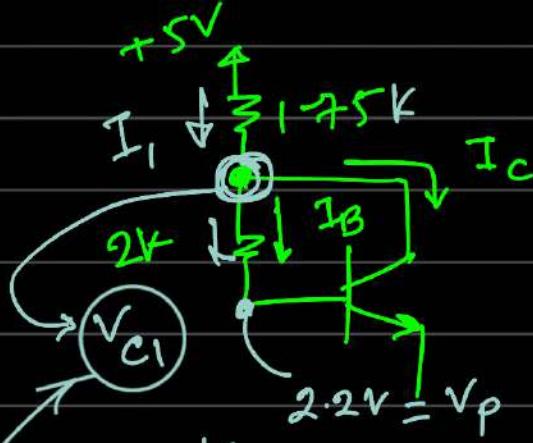
$$\Rightarrow V_{B1} - V_{C1} < 0$$

$$\Rightarrow V_{BC1} < 0$$

$T_1 \rightarrow \text{ON} \Rightarrow V_{BE1} > 0.5V$   
So  $T_1$  must be in forward active.

$$V_{BE} = 0.7V \quad (\text{for forward active})$$





$$I_C + I_B = I_I$$

$$\Rightarrow I_E = (\beta + 1) I_B = I_I$$

$$I_I = \frac{5 - V_{c1}}{1.75k}, \quad I_B = \frac{V_{c1} - V_p}{2k}$$

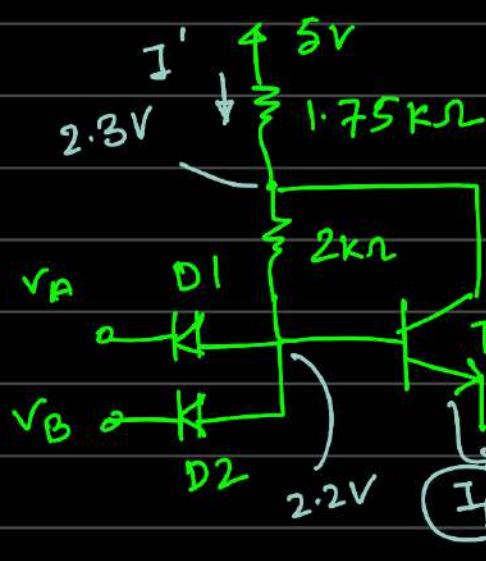
$$\Rightarrow (\beta + 1) I_B = I_I$$

$$\Rightarrow (30 + 1) \times \frac{V_{c1} - 2.2}{2k} = \frac{5 - V_u}{1.75}$$

$$\Rightarrow V_{c1} = 2.3V$$

$$I_B = \frac{2.3 - 2.2}{2k}$$

$$= 0.05mA$$



$$I_E = (\beta + 1) I_B$$

$$= 31 \times 0.05$$

$$= 1.55mA$$

$$I_2 = \frac{0.8}{5k}$$

$$= 0.16mA$$

$$I_B = I_E - I_2 = 1.39mA$$

fanout

$$I_{c,max} = \beta_F \times I_B = \underbrace{I_{c1}}_{\substack{\text{no load} \\ \text{collector current}}} + N \times I_L$$

standard load

$$1.39 \times 30 = 2.182 + N \times 0.82$$

$$\lfloor N \rfloor = \lfloor 35. \dots \rfloor$$

Maximum fanout = 35.

Q

## Lecture 6 : HTL circuit, Introduction to TTL circuit.

Power dissipation for DTL circuit:

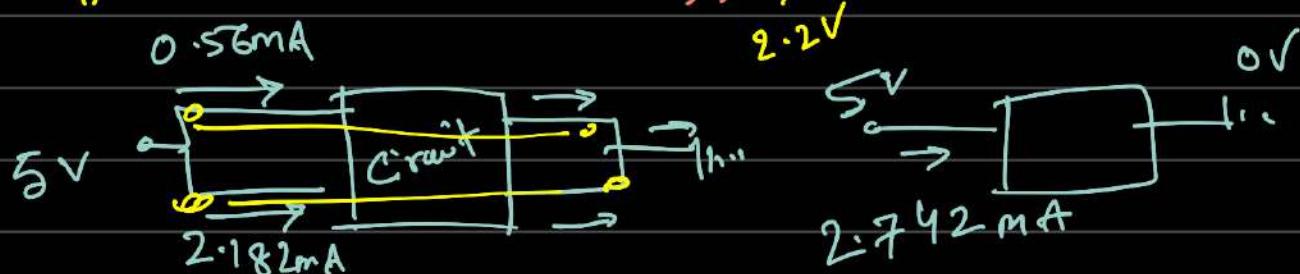
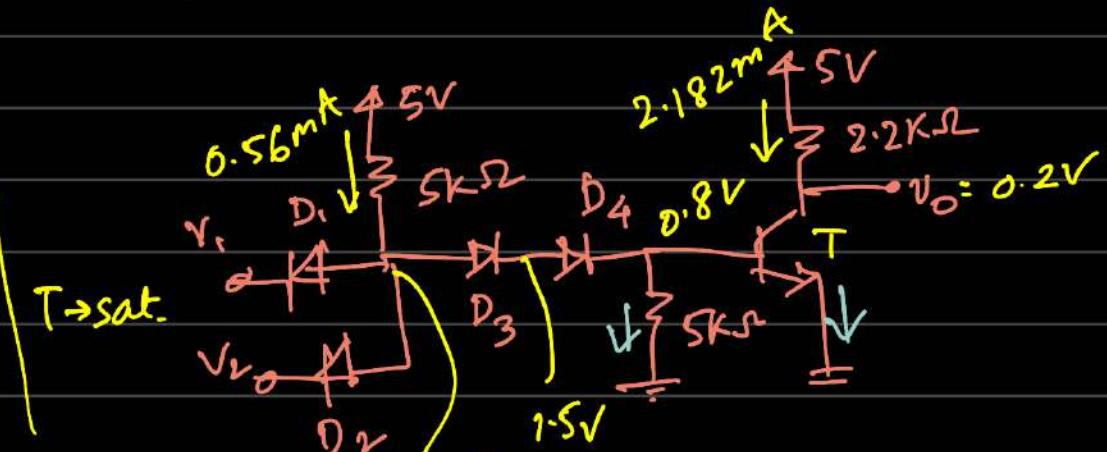
Case ① :

$$V_o = 0.2V$$

$$V_1 = V_2 = 5V$$

$D_1, D_2 \rightarrow \text{OFF}$

$D_3, D_4, T \rightarrow \text{ON}$



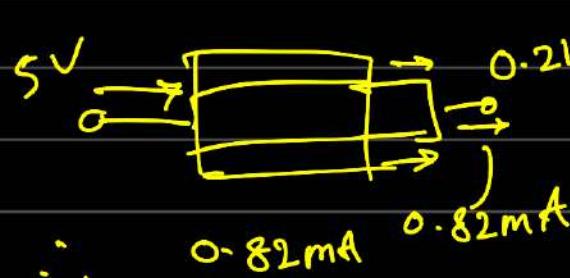
$$\text{Power dissipation} : \Delta V \times I = (5 - 0) \times 2.742$$

$$= 13.71 \text{ mW}$$

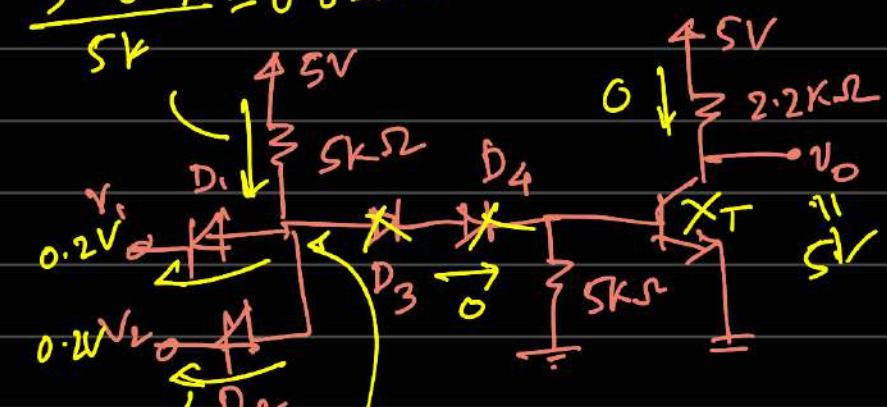
Case ②  $V_o = 5V$

$$\frac{5 - 0.9}{5V} = 0.82 \text{ mA}$$

$$V_1 = 0.2V, V_2 = 0.2V$$



$$I_{D2} = 0.41 \text{ mA} = I_{D1}$$

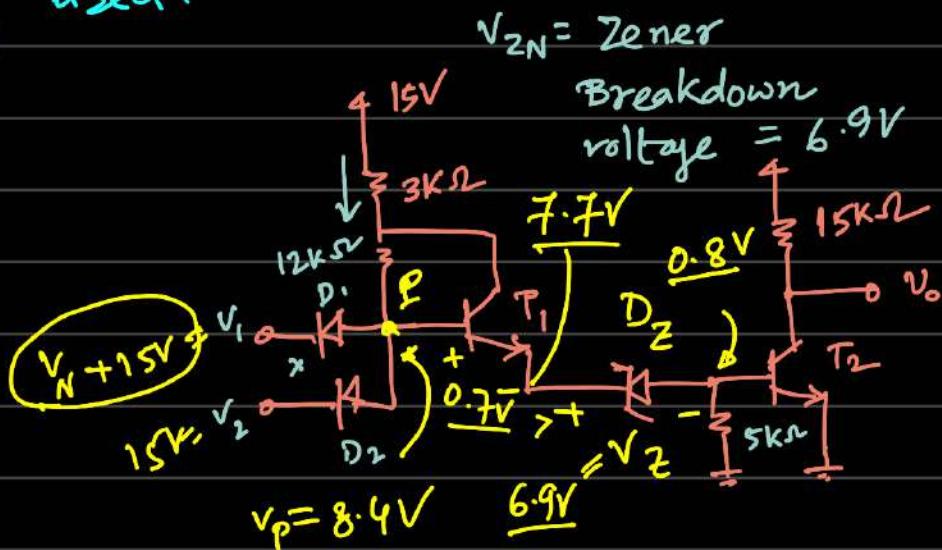
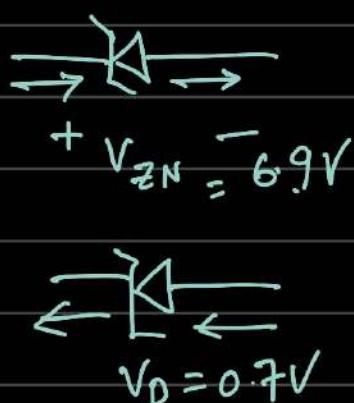


$$\text{Power dissipation here.} \quad \frac{(5 - 0.2) \times 0.41}{3.936 \text{ mW}}$$

HTL circuit:

High Threshold Logic circuit.

We want to improve the Noise margin, thus HTL circuits are being used.



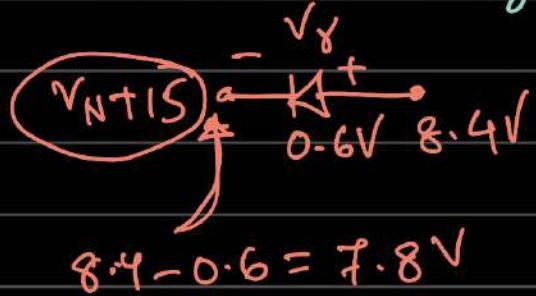
Q: If all the inputs are high, what is the magnitude of noise voltage which will cause the gate to malfunction?

$$\sqrt{N_H} = ?$$

Ans: Regular operation:  $v_N = 0$ ,  $D_1, D_2$  off.

$T_1, T_2$ ,  $T_2 \rightarrow \text{on}$ ,  $T_1 \rightarrow \text{forward active}$ ,  $T_2 \rightarrow \text{sat}$

$V_p = 8.4V$ . Circuit will malfunction if  $V_N + 15$  will reduce as much that  $D_1$  turn on and all the current through  $T_1$  bypass through  $D_1$ .



If  $V_N + 1.5 = 7.8$ , then the voltage across  $D_1$  diode is high enough to turn it ON.

$$\text{Therefore, } |V_{NH}| = |7.8 - 15| = 7.2 \text{ V}$$

Q: If one of the inputs are low, and rest of are high what is the magnitude of noise voltage at the low output terminal which will cause the gate to malfunction?

Ans:

Normal operation:

$D_1, D_2 \rightarrow \text{ON}$

$T_1, D_2, T_2 \rightarrow \text{OFF}$

If  $T_1, D_2$  and  $T_2$  turn on, then the

gafe malfunctions.

$V_\gamma$  (transistor) = 0.5V

$V_{ZN} = 6.9V$

$V_p = 0.9V$

↓

$V_p = 7.9V$

$$V_p = 0.2 + V_N \rightarrow V_p = 0.9 + V_N$$

The noise in  $V_i$  node will increase the voltage in  $V_p$  node in same manner.

Thus, the required noise voltage is.

$$0.9 + V_N = 7.9V \Rightarrow V_{N2} = 7V$$

Therefore, the noise margin.  $NM = \min(7.9, 7) = 7V$

Ques ②

Transistor-Transistor Logic:

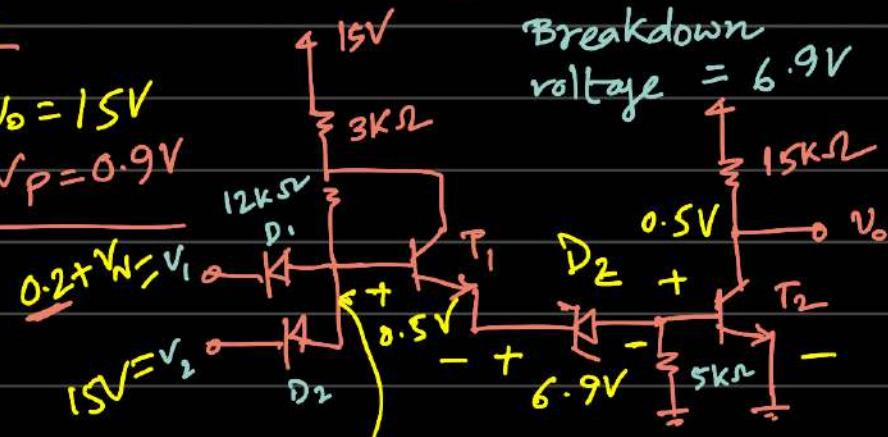
# Bipolar  $\rightarrow$  Saturated / Faster switching time compared to DTL.

# 74-series IC's are made using TTL circuits.

$V_{ZN}$  = Zener

Breakdown

voltage = 6.9V

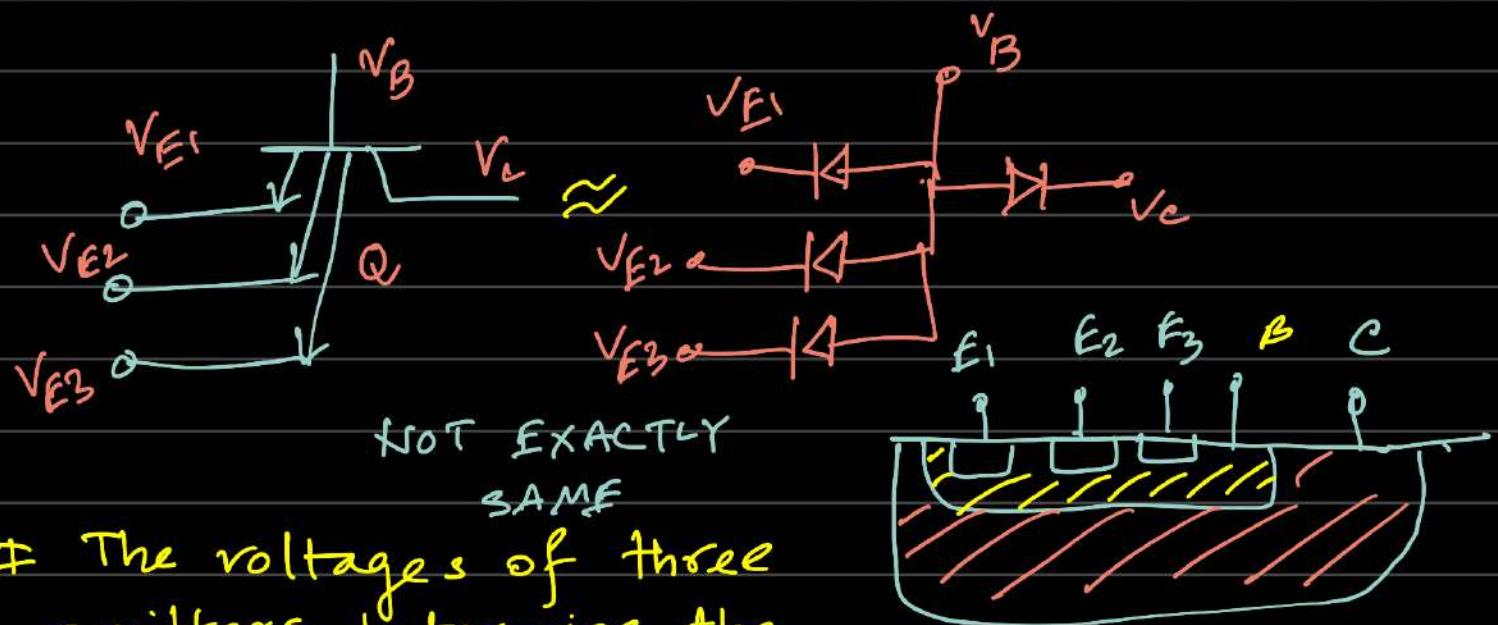


$$V_p = 0.2 + V_N = 0.9 + V_N = 7.9V$$

If  $V_p = 7.9$ , then  $T_1, D_2, T_2$  will turn on.

Turn on condition for the right side of the circuit

# Multiemitter transistor circuit:



# The voltages of three emitters determine the operating mode of multiemitter transistor.

## Basic operation:

# Q: Find the current, voltages of the following TTL circuit

Case: ①  $V_X = V_Y = 0.2V$

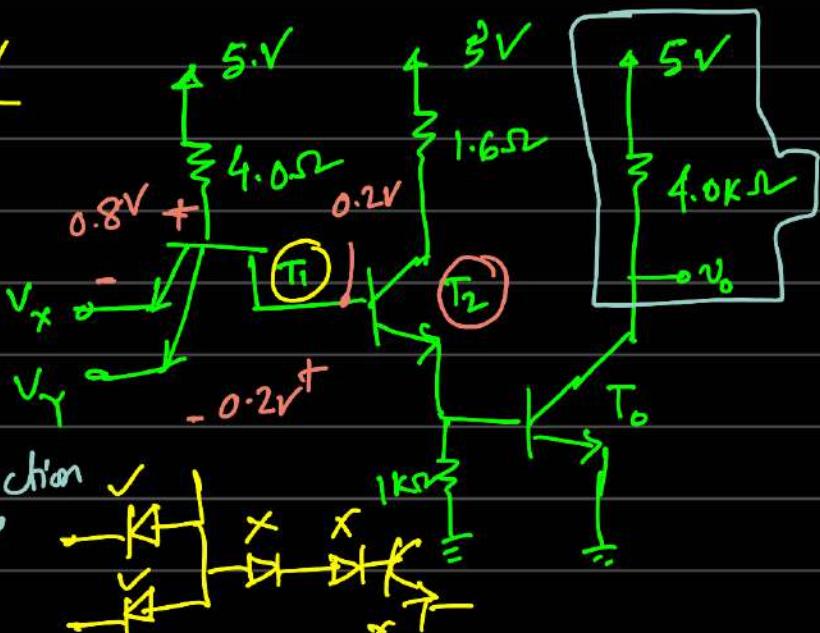
exactly like DTL.

$T_2, T_0 \rightarrow$  will cutoff.

In this case

BC junction and BE junction

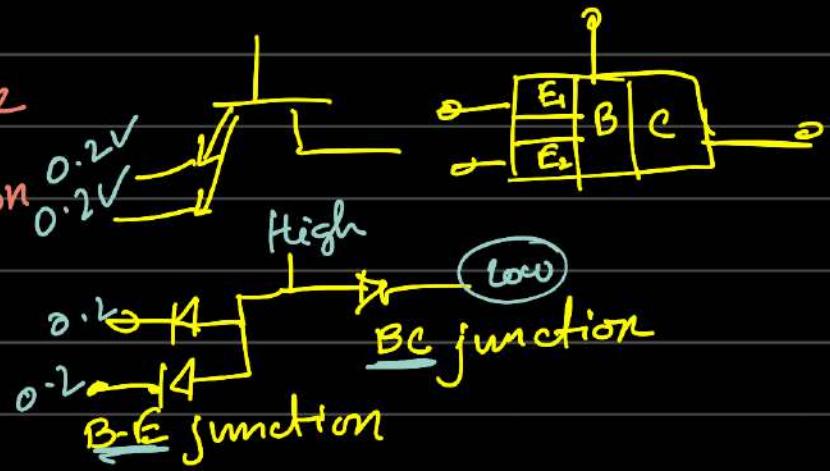
of  $T_1$  transistor "may" operate in forward active mode.



Therefore we can assume

$T_1$  is operating in saturation mode.

$$V_{CE}(T_1) = 0.2V$$



$V_{BE}(T_1) = 0.8V$ . So base voltage at  $T_2$  transistor is just  $0.2V$  which is not high enough to turn the  $T_2$  transistor. Thus our assumption is valid.

$T_0, T_2 \rightarrow$  cutoff

$T_1 \rightarrow$  saturation.

$$i_{C1} = 0 \text{ mA}$$

$$i_1 = i_2 = 0 \text{ mA}$$

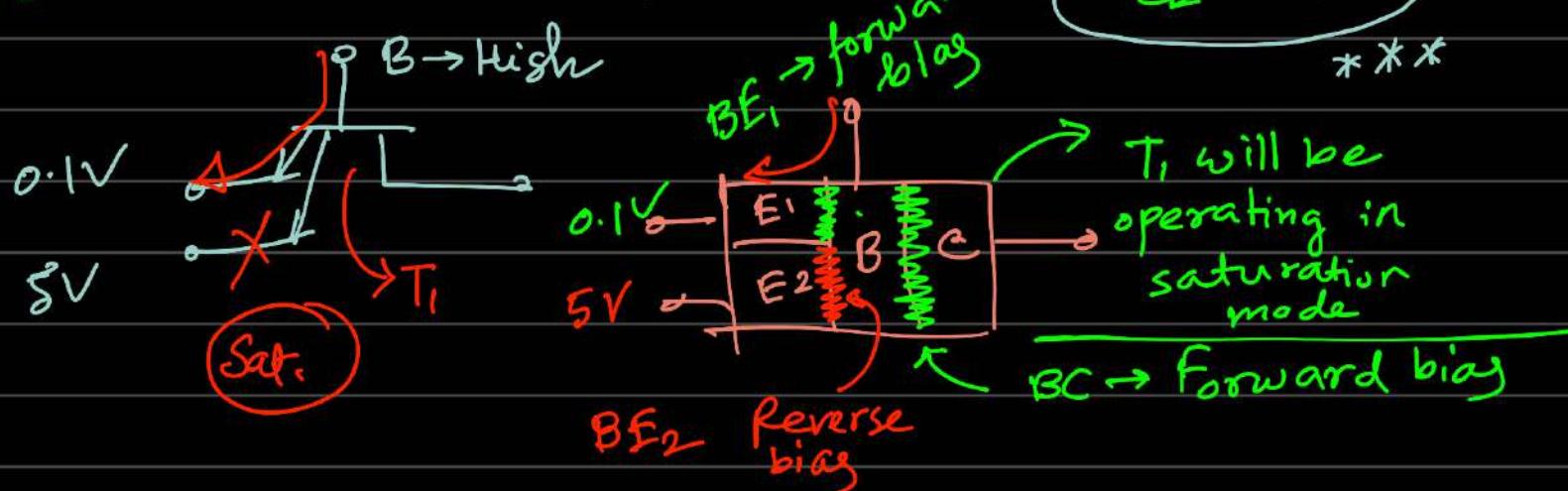
$$V_P = (0.2 + 0.8)V \\ = 1V$$

$$i_{B1} = i_3 = \frac{3-1}{4} = 1 \text{ mA}, \quad i_{EX} = i_{EY} = \frac{i_3}{2} = 0.5 \text{ mA}$$

$$\beta_{\text{forced}}(T_1) = \frac{i_c}{i_B} = \frac{0}{1} < \beta_F = 30$$

Case ②.  $V_X = 0.1V, V_Y = 5V$

[TTL  $\rightarrow$  Neaman]  
 $V_{CE} = 0.1V$

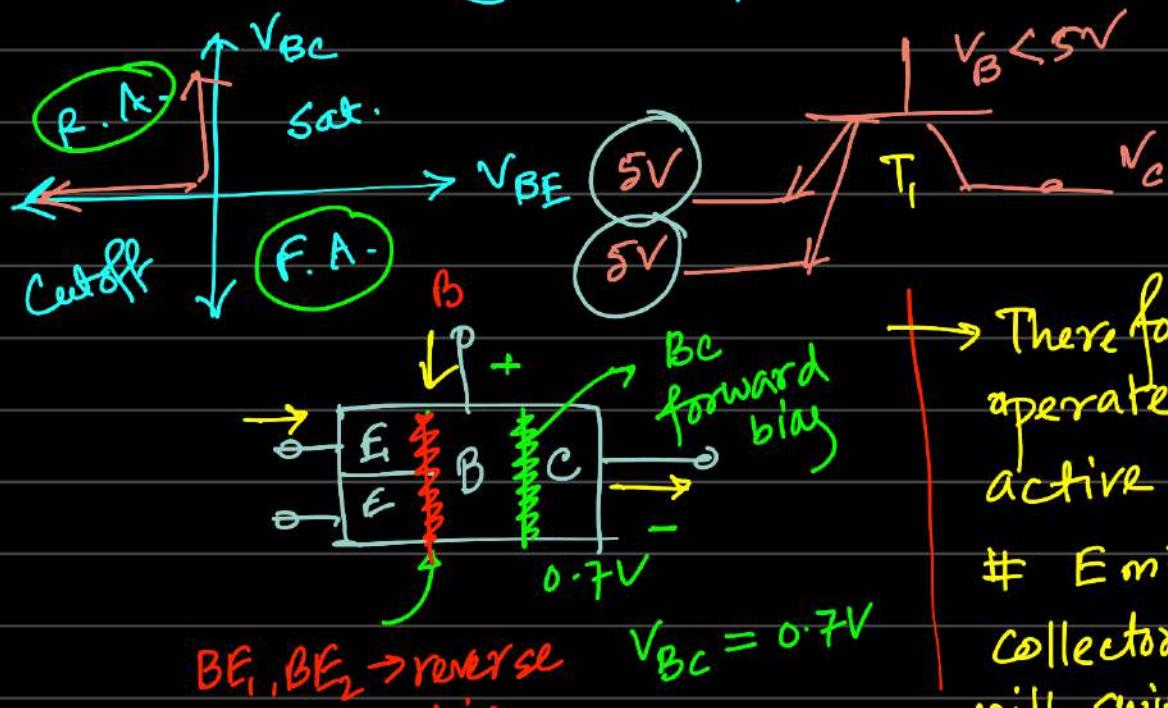


$$i_1 = i_2 = 0 \text{ mA}, \quad i_3 = 1 \text{ mA}, \quad i_{EY} = 0 \text{ mA}, \quad i_{EX} = 1 \text{ mA}$$

$$V_P = 0.9V \\ V_1 = 0.2V$$

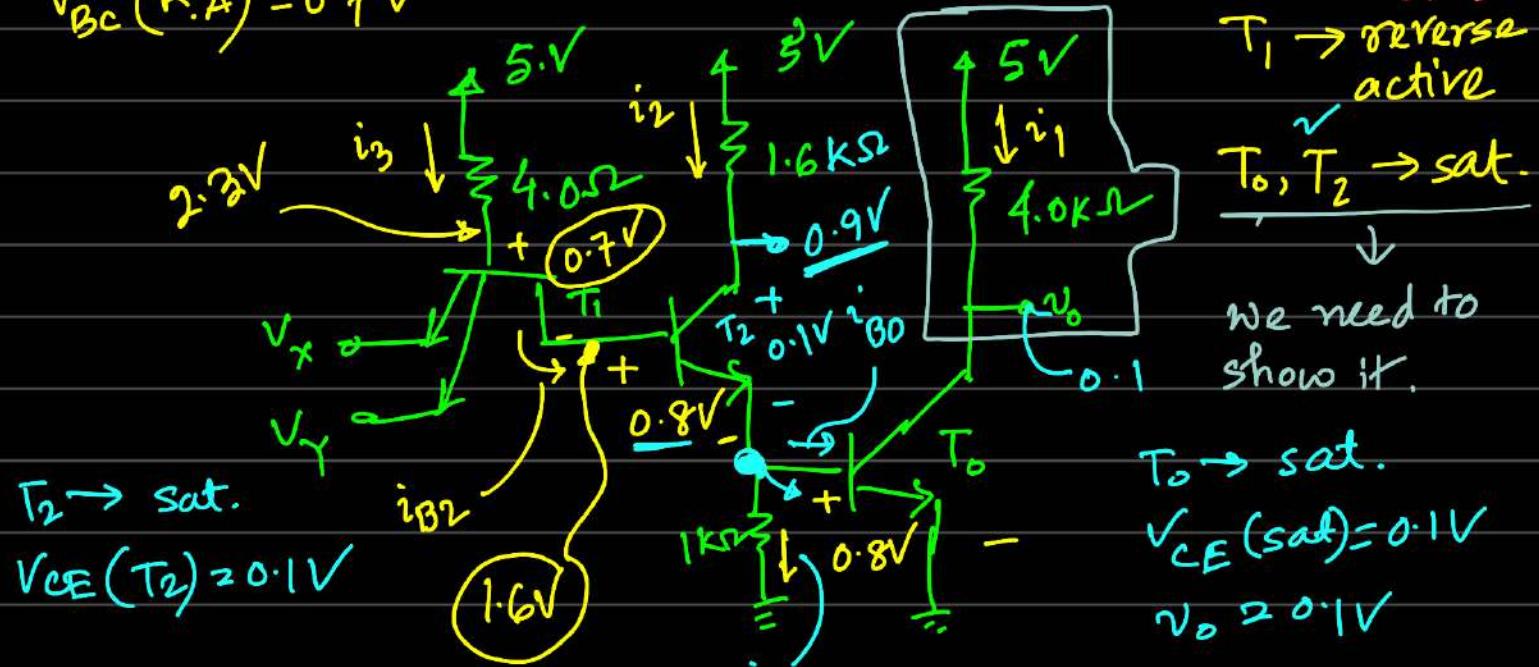
$V_0 = 5V, \quad$  [Case ② is similar to case ①.]

Case ③  $V_X = V_Y = 5V$  | "Reverse active"



$$\beta_R = \frac{\dot{i}_{EX}}{\dot{i}_B} = \frac{\dot{i}_{FY}}{\dot{i}_B} = \beta_R$$

$V_{BC}(R.A) = 0.7V$  → Because B-C junction is in forward bias.

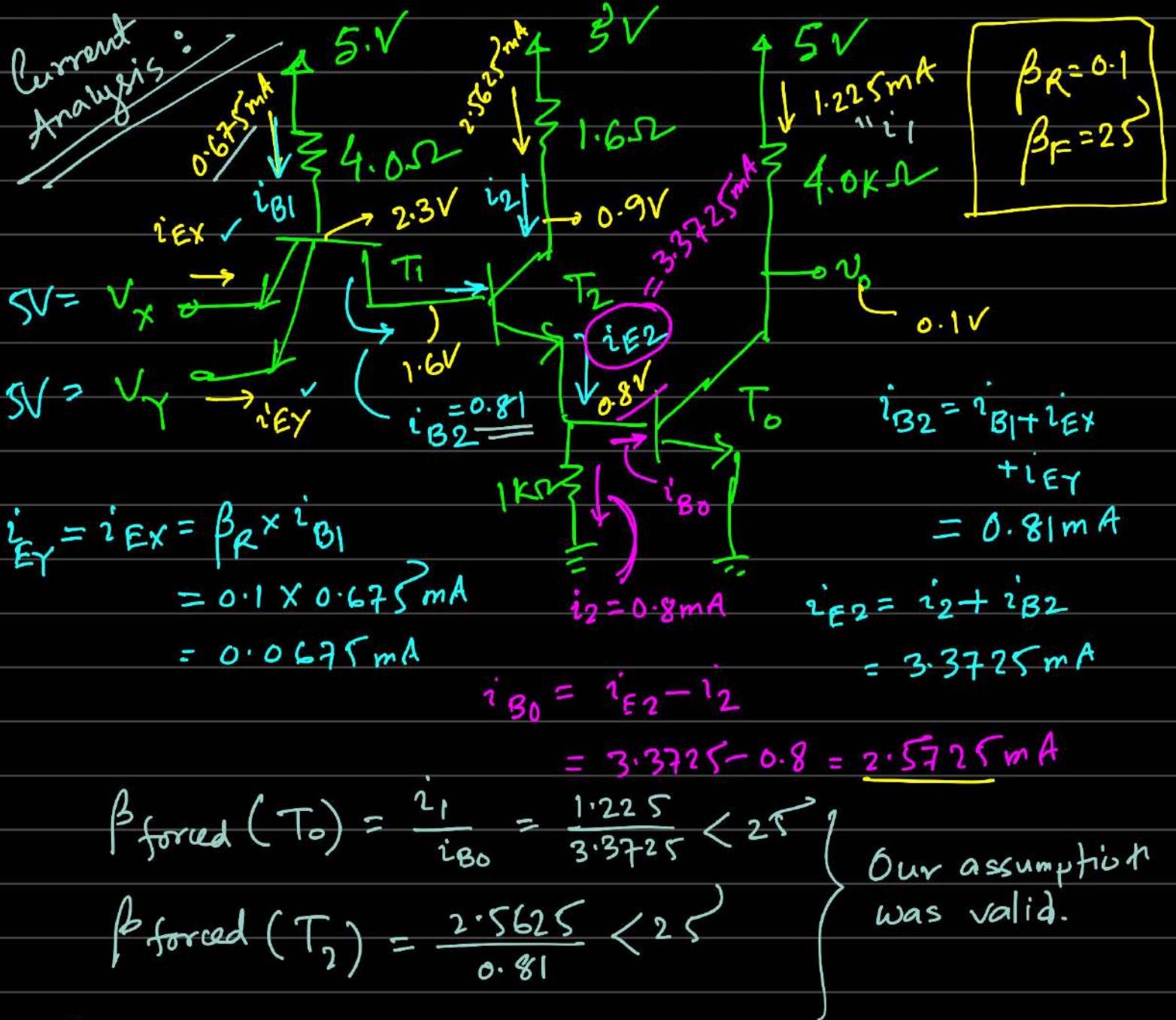


$$i_1 = \frac{5 - 0.1}{4K} = 1.225 \text{ mA}, \quad i_2 = \frac{5 - 0.9}{1.6K} = 2.5625 \text{ mA}$$

$$i_3 = \frac{5 - 2.3}{4K} = 0.675 \text{ mA}$$

$$V_{CE}(\text{sat}) = 0.1V$$

$$V_o = 0.1V$$

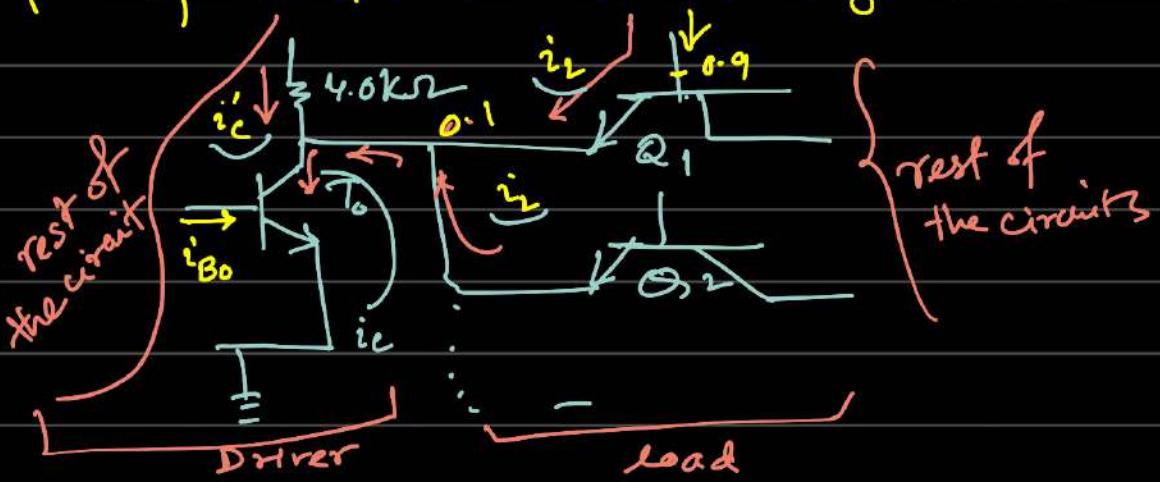


## Lecture 8 TTL circuit (continued)

Maximum fanout calculation of TTL NAND gate:

Given:  $V_{CE} = 0.1 \text{ V}$ ,  $\beta_F = 25$ ,  $\beta_R = 0.1$ ,  $V_{OH} = 34$ .

Case ① Output of the driver is at low logic level.



$i_C'$  → no load collector current = 1.225 mA

$$i_1 \rightarrow \text{individual load current} = \frac{5-0.9}{4} = 1.025 \text{ mA}$$

$$i_{B_0} \rightarrow \text{base current} = 2.5725 \text{ mA}$$

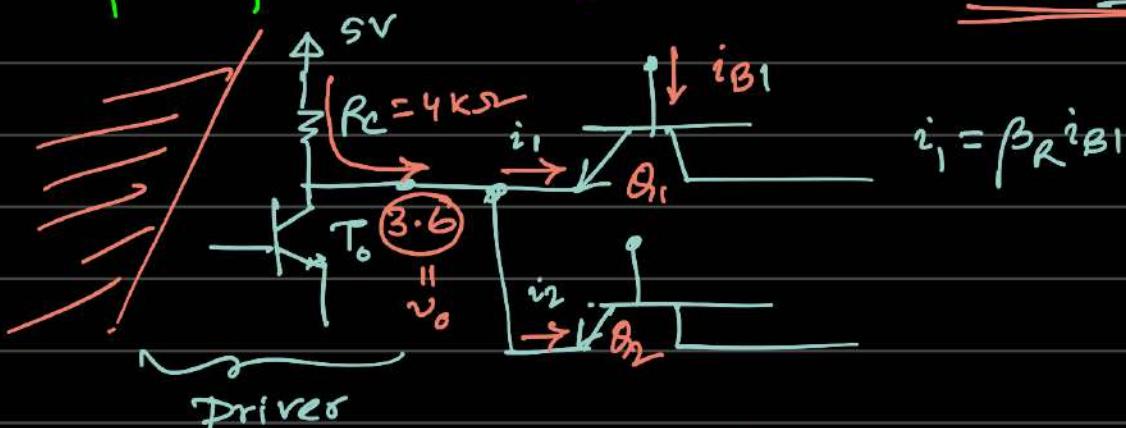
$N \rightarrow$  number of famouts to be determined.

$$i_{c,\max} = \beta_F \times i_{BD} = i_c' + N i_L$$

$$\Rightarrow 25 \times 2.5725 = 1.225 + N \times 1.025$$

$$N = \left[ 61, 35 \right] = 61 \leftarrow \text{maximum number of fanoout when } V_o = 0.1V$$

Case ②: Output of driver circuit could be  $V_{OH} = 3.6V$ .



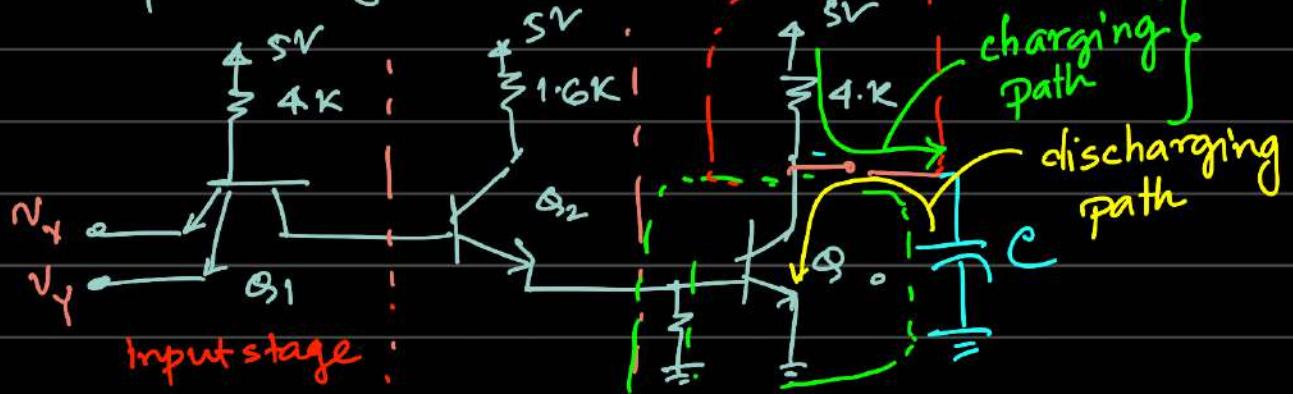
$$\text{Maximum supply current} = \frac{5 - 3.6}{4 \times 2} = 0.4 \text{ mA}$$

$$\# \text{ Individual demand current} = \beta_R \times i_{B1} \\ = 0.0675 \text{ mA}$$

$$\# \text{ Maximum fanout} = \left\lfloor \frac{0.4}{0.0675} \right\rfloor = \lfloor 5.92 \rfloor = 5$$

Combining these two cases we get maximum fanout. =  $\min(5, 61)$

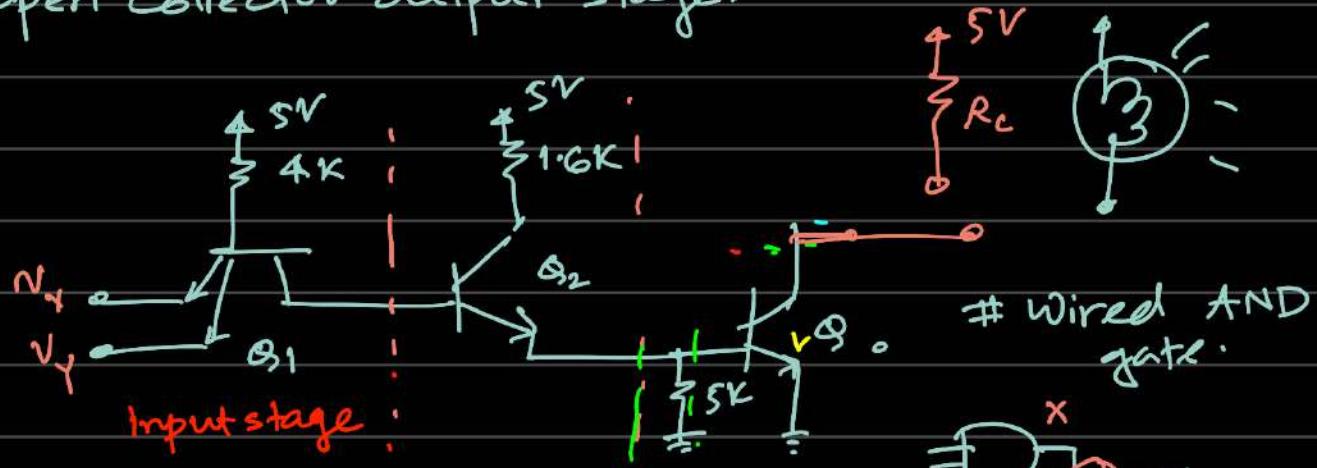
## TTL Output Stage:



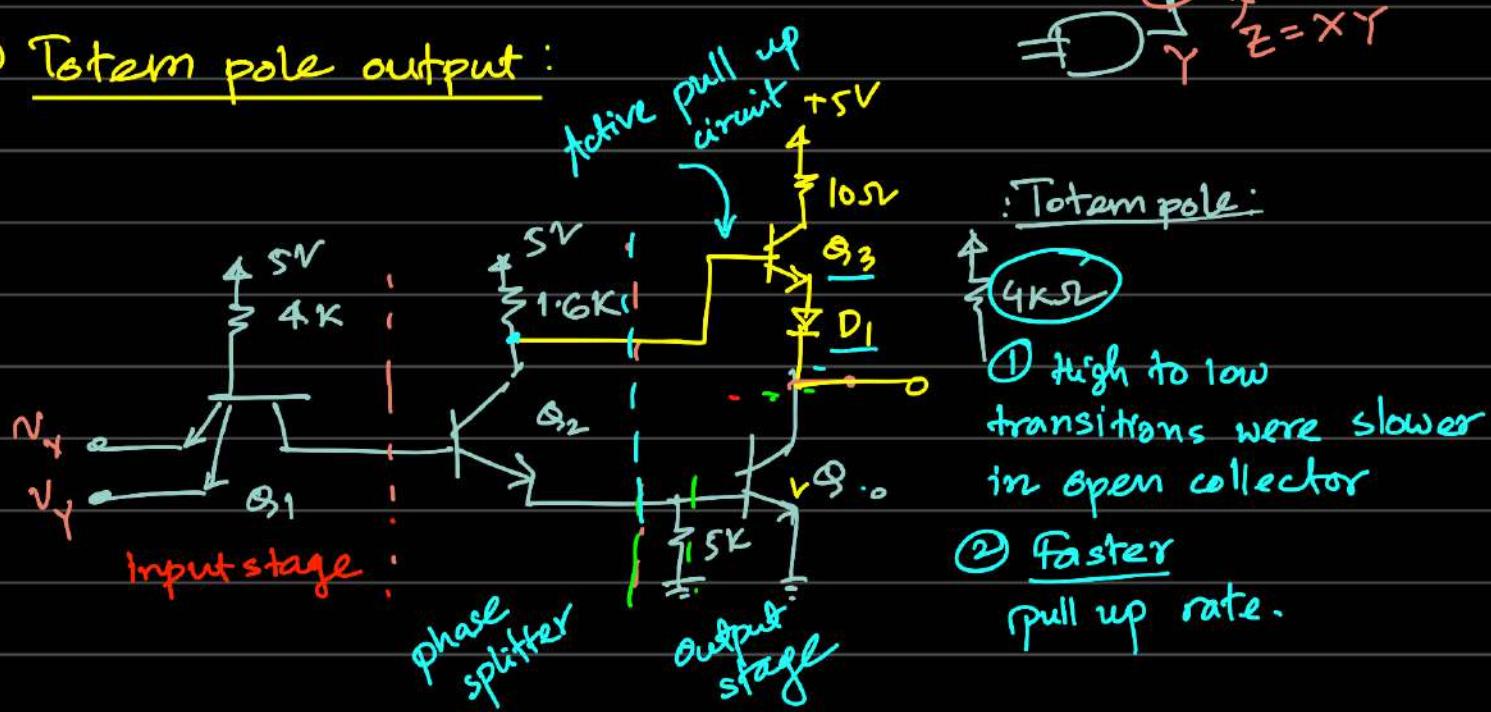
- # There is an effective capacitance connected to the output stage of the TTL circuit.
- # When changing output voltages, we need to draw or deliver current. That causes capacitor  $C$  to charge or discharge.
- # Pull up network pull up the output voltage to high value as well as charge the capacitor.
- # Pull down reduces the voltage at the output
- # TTL circuits are classified based on the output stages into three categories.

- ① Open collector output
- ② Totem-pole output stage
- ③ Tristate output stage.

### ① Open collector output stage:



### ② Totem pole output:



### ③ Tristate output:

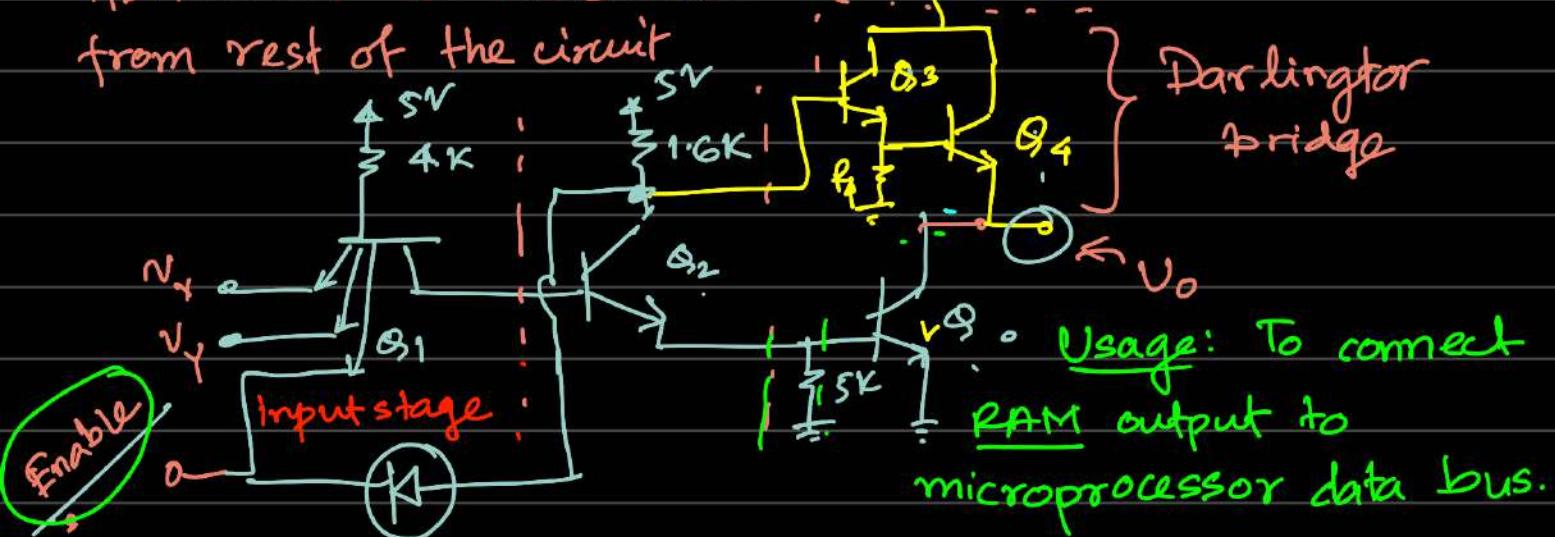
3 stages of output : logical high, logical low, high impedance ( $Z$ )

# Cause for  $Z$  output: open circuit.

# if we put 0 in enable pin

all the transistors other than  $Q_1$  would go to cutoff mode. That will cause the  $V_o$  output terminal to disconnect.

from rest of the circuit

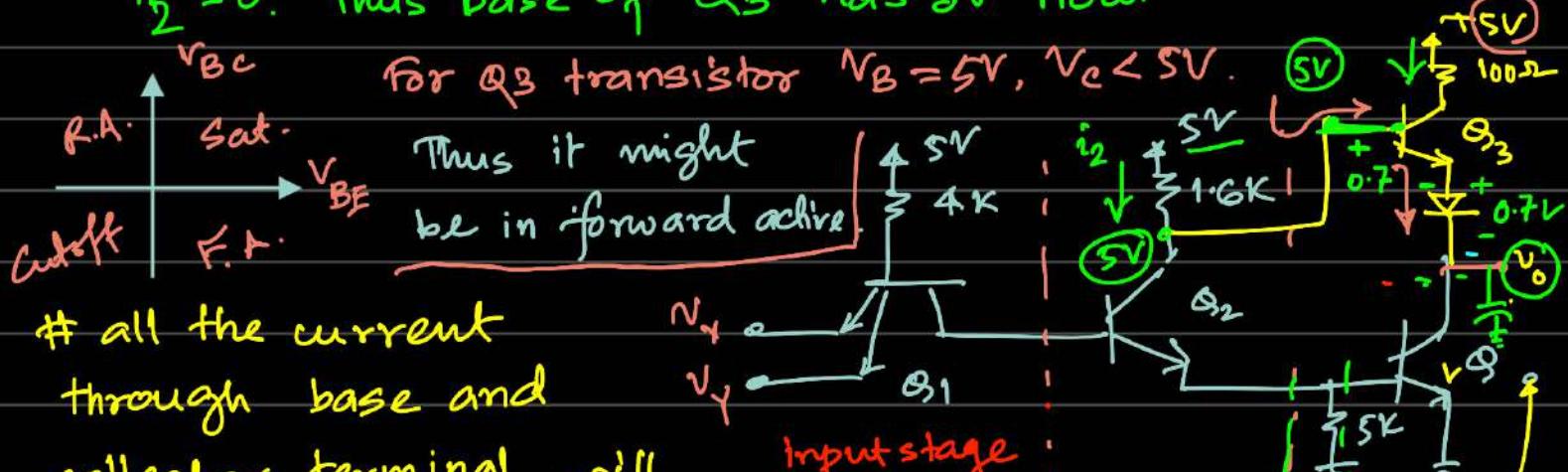


Usage: To connect RAM output to microprocessor data bus.

### # Totem pole basic operation:

① Case 1: Any of the input terminal is low.

Therefore, we  $Q_1 \rightarrow$  saturation.  $Q_2, Q_3 \rightarrow$  cutoff.  $i_2 = 0$ . Thus base of  $Q_3$  has 5V now.



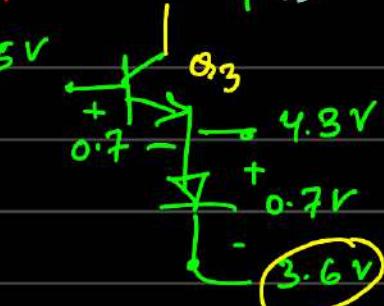
# all the current through base and

collector terminal will

charge the capacitor initially.

# Therefore the capacitor can charge up to 3.6V maximum.

Input stage :



# The charging of the capacitor will stop eventually.

∴  $i_{B3} = i_{C3} = 0 \text{ mA}$  (when steady state arrives).

Bonus: Does the state of transistor Q<sub>3</sub> change?

Ans: No. voltage differences freezed out and  $i_{C3} = \beta i_{E3}$ .

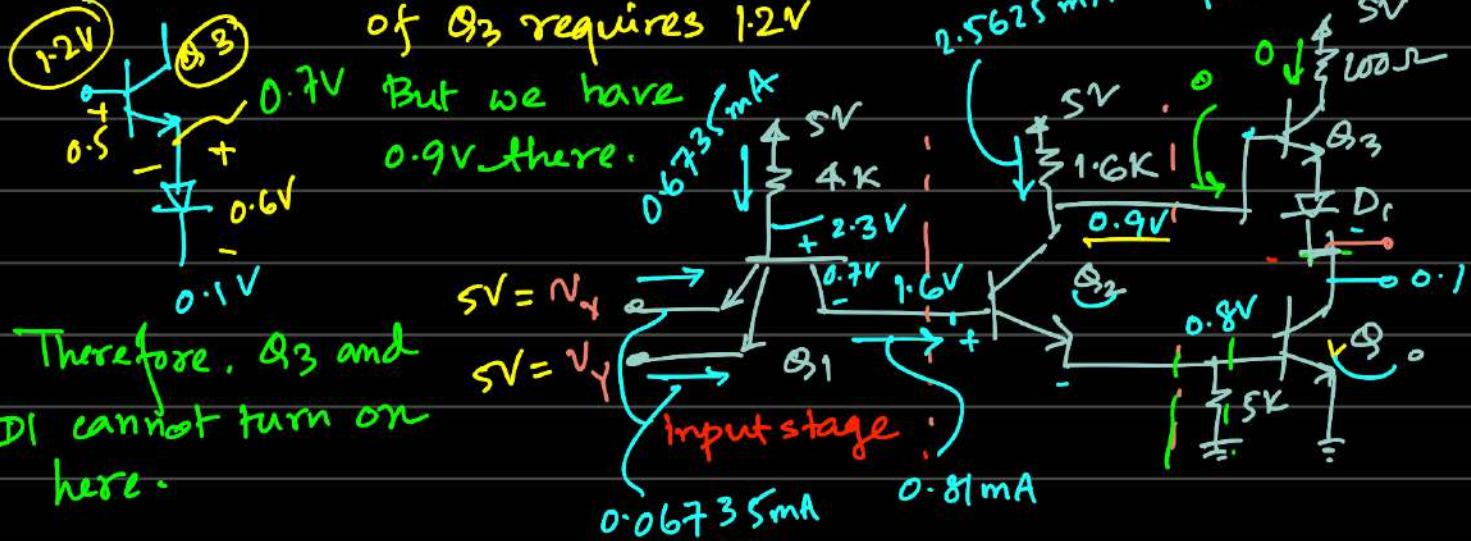
# Rest of the voltages and currents are same as open collector/ basic TTL circuits.

Case: ②.  $v_x = v_y = 5V$

$Q_1 \rightarrow$  Reverse active,  $Q_2, Q_0 \rightarrow$  saturation.

$\theta_{33} \rightarrow$  cutoff mode?

Suppose  $Q_3$  and  $D_1$  is ON. Then base terminal  $\beta_R = 0.1$

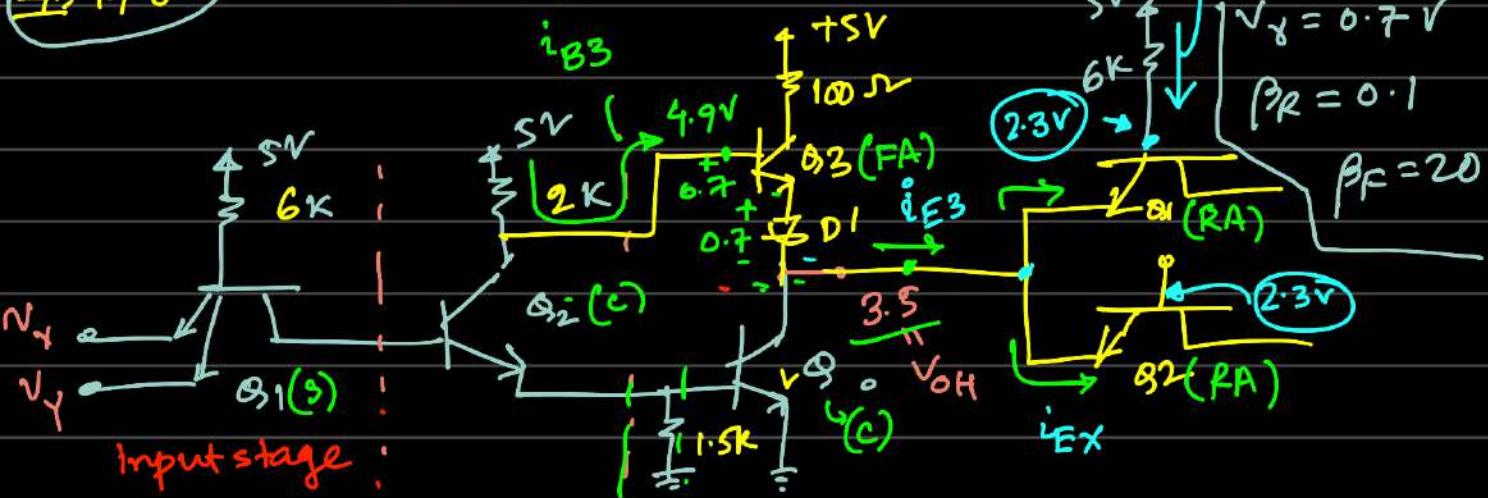


## # Maximum fanout calculation :-

由 Case ①: driver output is High.

Q: Assume  $v_o$  is allowed to decrease by  $0.1V$  from no load condition. Then find the maximum fanout.

Ex: 17.30



$$\text{If } i_{B3} = \frac{5-4.9}{2k} = 0.05 \text{ mA,}$$

$$\# \quad i_E3 = (\beta + 1) i_{B3} = 1.05 \text{ mA} \quad [ \text{Total supply current available} ]$$

$$\# \text{ Br} = (5 - 2 \cdot 3) / 6k = 0.45 \text{ mA}$$

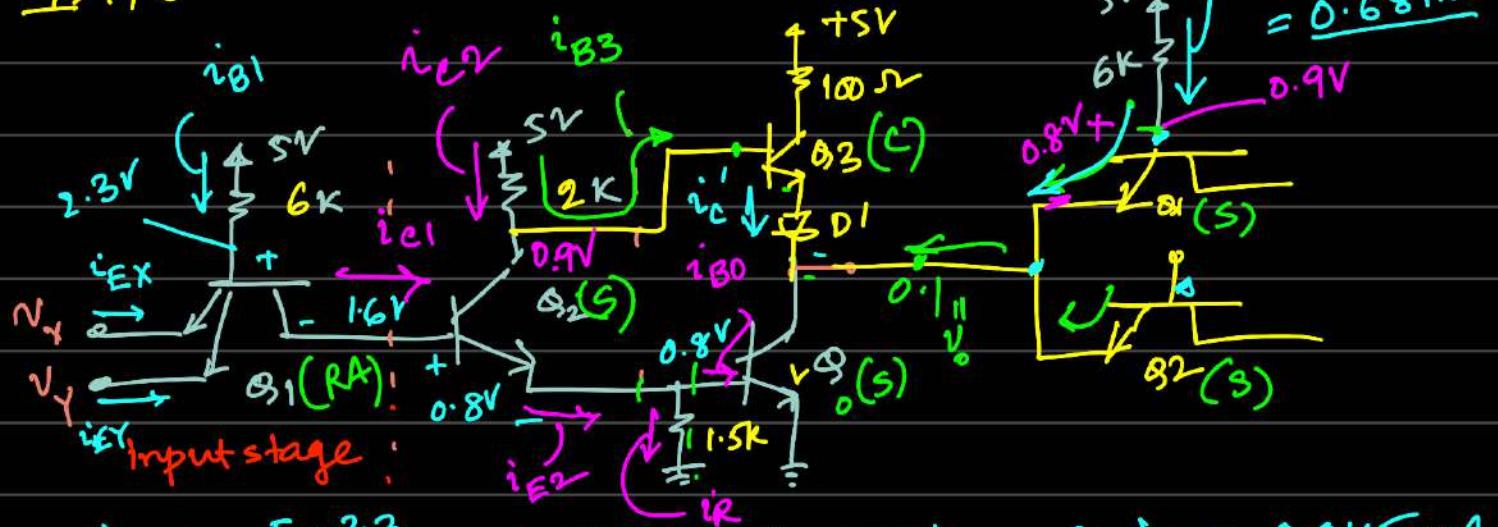
$$\text{at } i_{\text{Ex}} = \beta_R \cdot i_{\mathcal{B}1} = 0.045 \text{ mA. (individual demand)}$$

Finally, maximum famous =  $\left\lfloor \frac{\text{Supply current}}{\text{Demand current}} \right\rfloor$

$$= 23$$

由 if the driver output is low:

Ex: 17.30



$$i_{B1} = \frac{5 - 2 \cdot 3}{6k} = 0.45 \text{ mA}, \quad i_{Ex} = i_{Ey} = \beta_R i_{B1} = 0.045 \text{ mA}$$

$$i_{C1} = i_{B1} + i_{Ex} + i_{Ey} = 0.54 \text{ mA}, \quad i_{e2} = \frac{5 - 0.9}{2k} = 2.05 \text{ mA}$$

$$i_{E2} = i_{c1} + i_{c2} = 2.59mA, i_R = \frac{0.8 - 0}{1.5K} = 0.53mA$$

$$i_{QD} = 2.59 - 0.53 = 2.06 \text{ mA}$$

∴  $\beta_3$  is in cut-off  $i_0' = 0$ . Thus

$$i_{c, \text{max}} = \beta_F \times i_{B0} = N \times i_L$$

$$\Rightarrow 20 \times 2.06 = N \times 0.68$$

$$N = |60| = 60$$

# Finally maximum fanout =  $\min(50, 23)$

-723

## Lecture 9: Introduction to ECL logic family.

Power dissipation in Driver circuit in TTL:

Q: Calculate the power

dissipation in the driver

circuit for  $V_x = V_y = 5V$ , when

fanout = 10.  $\beta_F = 25, \beta_R = 0.1$

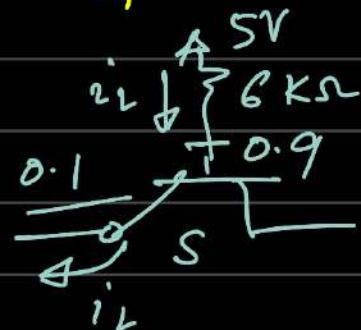
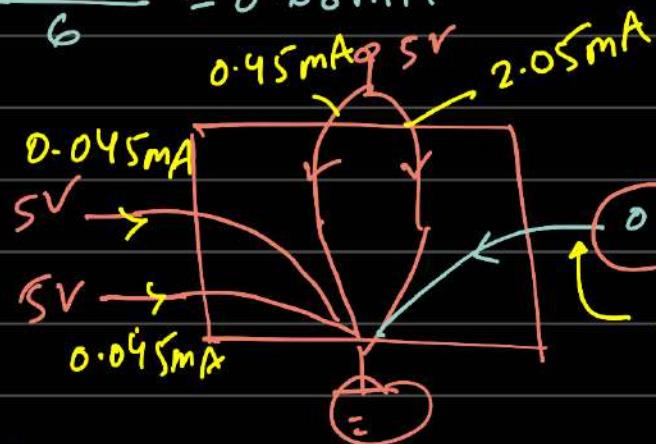
Soln:

When  $V_x = V_y = 5V$ ,

$Q_1 \rightarrow$  reverse active,  $Q_2 \rightarrow$  sat,  $Q_3 \rightarrow$  sat,  
 $Q_4 \rightarrow$  cutoff.

On the other hand, the input of the load circuit is at low voltage. Thus,  $Q_1$  would be in saturation for load circuit.

$$i_L = \frac{5 - 0.9}{6} = 0.68 \text{ mA}$$



$$10i_L = 6.8 \text{ mA}$$

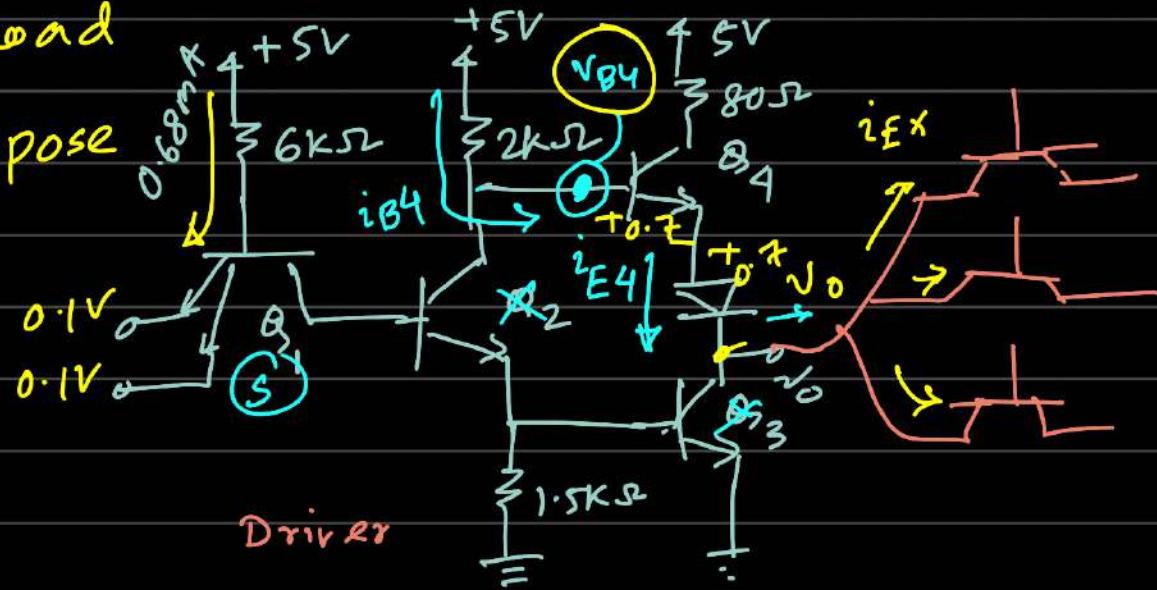
$$P = (5 - 0) \times (2.05 + 0.45 + 0.045 \times 2) + (0.1 - 0) \times 6.8$$

$$= 13.63 \text{ mW.}$$

Question: Calculate the power dissipation in the driver for  $V_x = V_y = 0.1V$  and fanout = 10.

Ans: In driver circuit we have  $Q_1 \rightarrow$  saturation,  $Q_2, Q_3 \rightarrow$  cutoff,  $Q_4 \rightarrow$  forward active mode.

Again, for load circuits suppose all the input voltages are high.

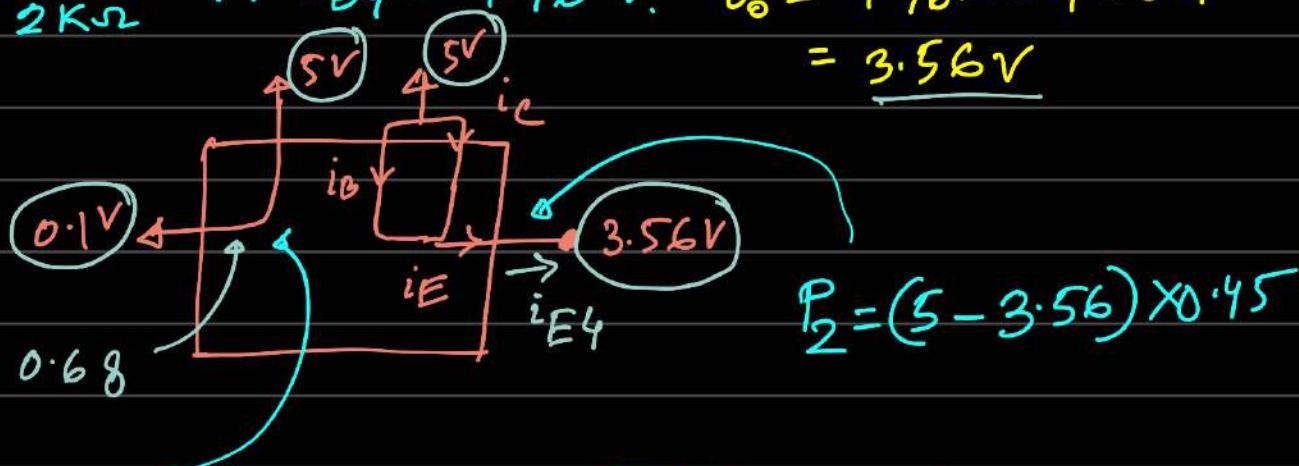


Each load circuit would draw about  $i_{EX} = 0.045\text{mA}$  load current. Total load current would be

$$10 \times i_{EX} = 0.45\text{mA} = i_{E4} \text{ (emitter current of Q4)}$$

$$i_{B4} = i_{E4} / (\beta_f + 1) = 0.45 / (25 + 1) = 0.02\text{mA}$$

$$i_{B4} = \frac{5 - V_{B4}}{2\text{k}\Omega} \therefore V_{B4} = 4.96\text{V. } V_o = 4.96 - 0.7 - 0.7 = 3.56\text{V}$$



$$P_1 = (5 - 0.1) \times 0.68$$

Total power dissipation.

$$P_{\text{tot}} = P_1 + P_2 = 3.94\text{mW}$$

Homework: 4.3 . "Modified Totem pole" (7400 NAND)

Recommended Practice problem:

Neaman's book. Chapter 17: (DTL, TTL)

17.20, 17.21, 17.23, 17.25, 17.28, 17.32

Midterm syllabus

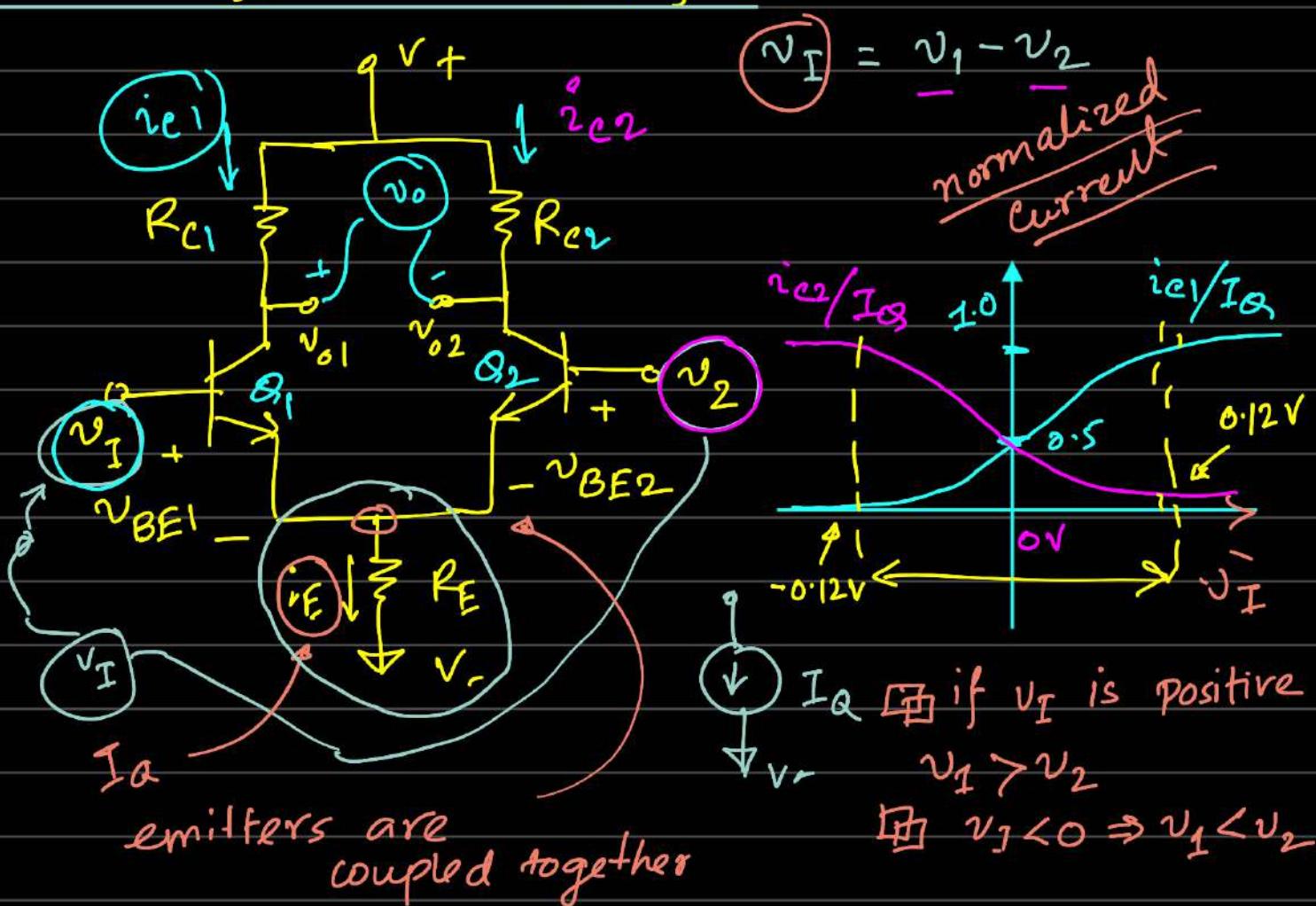
## Emitter Coupled Logic Family

→ Bipolar → Unsaturated logic family.

# logic transistors never goes to saturation mode. They will operate within cutoff and forward active mode.

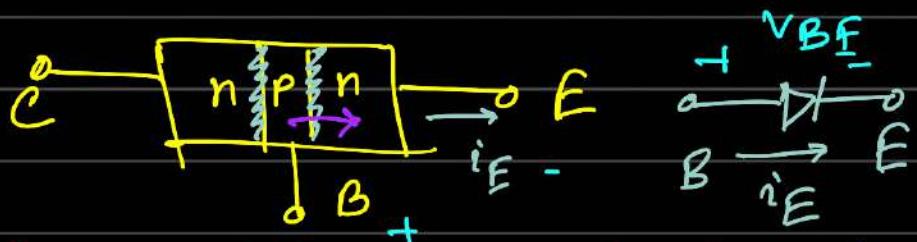
▪ This will allow transistors to reduce storage time in transistors. Therefore, the switching speeds gets faster.

## Basic differential Amplifiers:



# Remarks: sometimes  $R_E$  transistor is replaced using a constant current source with current  $I_Q$ .

## # Switching behavior of ECL circuit:



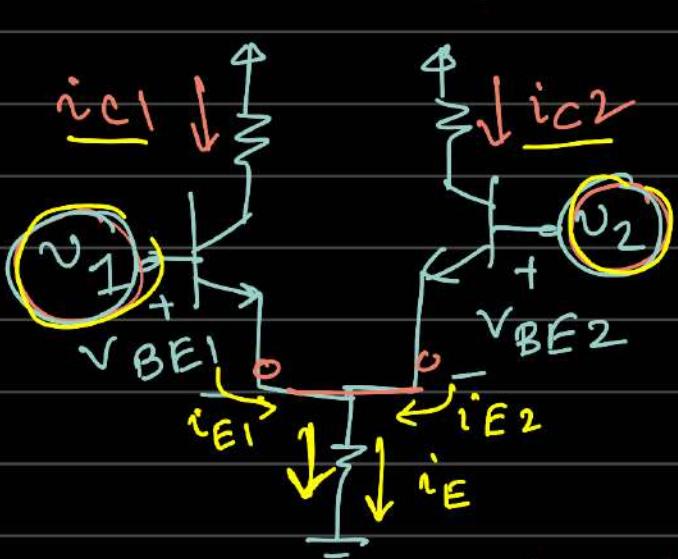
$$i_E = I_S \exp\left(\frac{V_{BE}}{V_T}\right)$$

$i_E$  = emitter current = junction current

$V_{BE}$  = base-emitter voltage.

$I_S$  = reverse saturation current

$V_T$  = thermal voltage.  $T = 300K$ ,  $V_T = 25.9mV$   
 $= 0.0259V$



$$V_I = V_1 - V_2$$

$$= V_{BE1} - V_{BE2}$$

$$[(V_{B1} - V_{E1}) - (V_{B2} - V_{E2})]$$

$$V_{B1} - V_{B2}$$

$$\frac{i_{E1}}{i_{E2}} = \frac{I_S \exp\left(\frac{V_{BE1}}{V_T}\right)}{I_S \exp\left(\frac{V_{BE2}}{V_T}\right)}$$

$$i_{E1} = I_S \exp\left(\frac{V_{BE1}}{V_T}\right) \quad \text{--- (1)} \quad = \exp\left(\frac{V_{BE1}}{V_T} - \frac{V_{BE2}}{V_T}\right)$$

$$i_{E2} = I_S \exp\left(\frac{V_{BE2}}{V_T}\right) \quad \text{--- (2)}$$

$$\left[ \frac{e^a}{e^b} = e^{a-b} \right]$$

Therefore,  $\left( \frac{i_{E1}}{i_{E2}} = \exp\left(\frac{V_{BE1} - V_{BE2}}{V_T}\right) \right)$

$$\left( \frac{i_{E1}}{i_{E2}} = \exp\left(\frac{V_I}{V_T}\right) \right)$$

$$i_{E1} + i_{E2} = i_E = \text{almost constant}$$

$$\textcircled{1} \quad \frac{i_{E1}}{i_{E2}} \gg 1 \quad \therefore \quad i_{E1} \approx i_E \quad \text{and} \quad i_{E2} \approx 0$$

$$\textcircled{2} \quad \frac{i_{E1}}{i_{E2}} \ll 1 \quad , \quad i_{E2} \approx i_E \quad \text{and} \quad i_{E1} \approx 0.$$

$$\frac{i_{E1} + i_{E2}}{i_{F2}} = \frac{i_E}{i_{F2}} \Rightarrow \frac{i_{E1}}{i_{E2}} + 1 = \frac{i_E}{i_{F2}} \Rightarrow i_{E1} \approx i_E$$

We can take for case ①.  $i_{E1} \approx 100 i_{E2}$

$$\text{Then } 100 = \exp\left(\frac{v_I}{v_T}\right) \Rightarrow v_I = v_T \ln(100) = 0.025 \times \ln(100) \Rightarrow v_1 - v_2 = 0.12V$$

† ECL circuits are designed in such a way that if any transistor is on, it operates in forward active mode  $\beta_F \gg 1$ . Therefore we can ignore base current if it is not mandated by the question.

Because of this we can write  $i_C \approx i_E$  in ECL circuits.

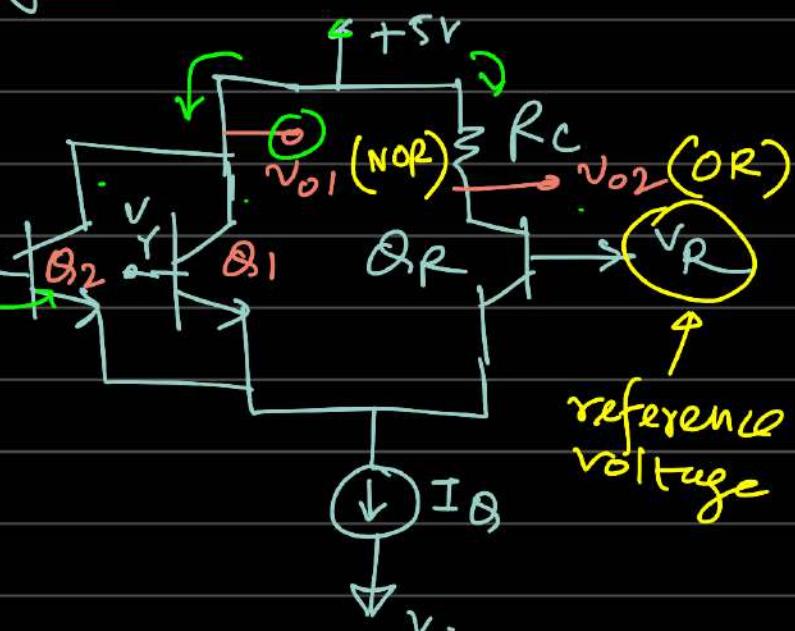
Basic ECL NOR gate:

Logic 1:  $v_X, v_Y > v_R$

Logic 0:  $v_X, v_Y < v_R$

$v_Y$	$v_X$	$Q_1$	$Q_2$	$Q_R$	$v_{o1}$	$v_{o2}$
L	L	C	C	FA	H	L
L	H	FA	C	C	L	H
H	L	C	FA	C	L	H
H	H	FA	FA	C	L	H

NOR gate      OR gate



reference voltage

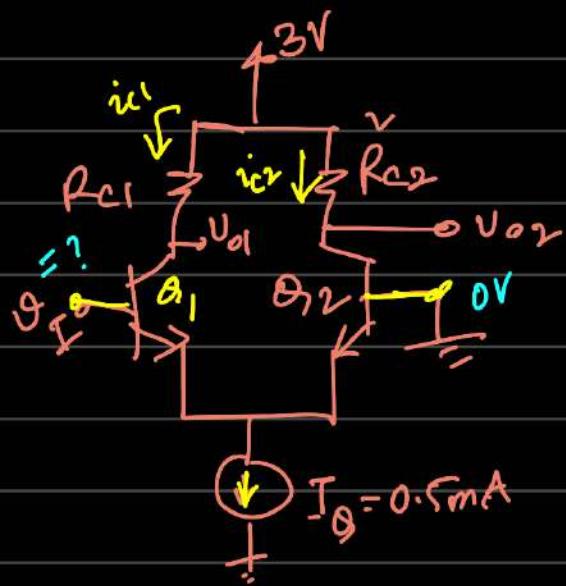
## lec10: Midterm Review

17.3] Neglect base current in the following circuit

(a) Determine the value of  $R_{C2}$  such that the minimum value of  $v_{o2} = 0$ .

(b) Determine the value of  $R_{C1}$  such that  $v_{o1} = 1V$  when  $v_I = 1V$ .

(c) Determine the value of  $v_I$  so  $i_{C2} = 0.4mA$ ,  $i_{C1} = 0.1mA$



(a) We will get minimum value of  $v_{o2}$  when Q2 transistor is F.A. and maximum amount of current is flowing through  $R_{C2}$  resistor.

So maximum amount current could flow through  $R_{C2}$  is  $I_Q = 0.5mA$ .

$$i_{C2} = \frac{3 - 0}{R_{C2}} = 0.5mA \Rightarrow R_{C2} = 6k\Omega$$

(b) When  $v_I = 1V$ , then  $v_I - 0 > 0.12V$ . Thus Q1 is F.A. and Q2 is cut off.  $i_{C1} \approx I_Q$  and  $i_{C2} \approx 0V$ .

$$\therefore v_{o1} = 1V. \quad i_{C1} = 0.5mA = \frac{3 - 1}{R_{C1}} \Rightarrow R_{C1} = 4k\Omega$$

(c)  $v_I = ?$   $i_{C1} = 0.1mA$ ,  $i_{C2} = 0.4mA$ .

Because the base current is negligible,  $i_{E1} \approx i_{C1}$ .

$$i_{E2} \propto i_{C2}. \quad i_{E1} = I_S \exp\left(\frac{V_{BE1}}{V_T}\right), \quad i_{E2} = I_S \exp\left(\frac{V_{BE2}}{V_T}\right)$$

$$\frac{i_{C2}}{i_{C1}} = \frac{i_{E2}}{i_{E1}} = \exp\left(\frac{V_{BE2} - V_{BE1}}{V_T}\right) \Rightarrow \exp\left(\frac{0 - V_I}{V_T}\right)$$

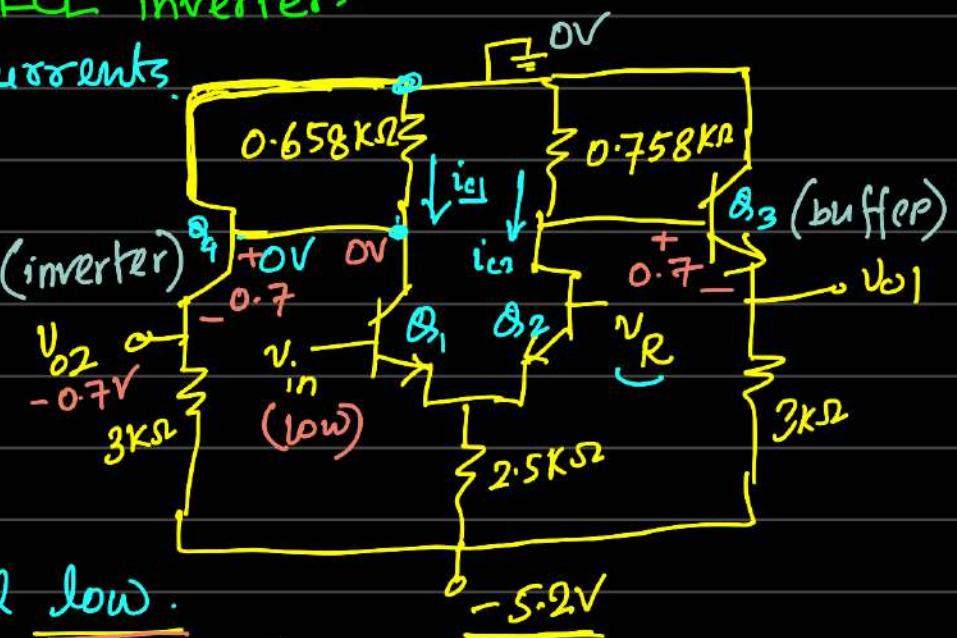
$$\Rightarrow \frac{0.4}{0.1} = \exp\left(-\frac{V_I}{V_T}\right) \Rightarrow V_I = -V_T \ln(4) = -0.0359V$$

$$\boxed{\frac{1}{V_T} = 0.0259}$$

# find the logical low voltage and logical high voltage for the following ECL inverter.

# Ignore all base currents.

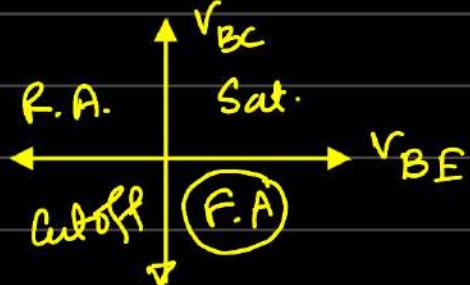
$V_{in}$	$V_R$	$\theta_1$	$\theta_2$	$V_{o1}$	$V_{o2}$
-1.4	-1.35	cut off	F.A.	-1.7	-0.7
-0.7	-1.35	F.A	cut off	-0.7	1.7



(a) If  $v_{in}$  is logical low.

[That means  $V_{in}$  has much smaller voltage than  $V_R$ ] It implies that  $\theta_1$  is in cutoff and  $\theta_2$  would be in forward active. Thus,  $i_Q = 0$ .

The base voltage of  $\text{Q}_4$  should be 0V.



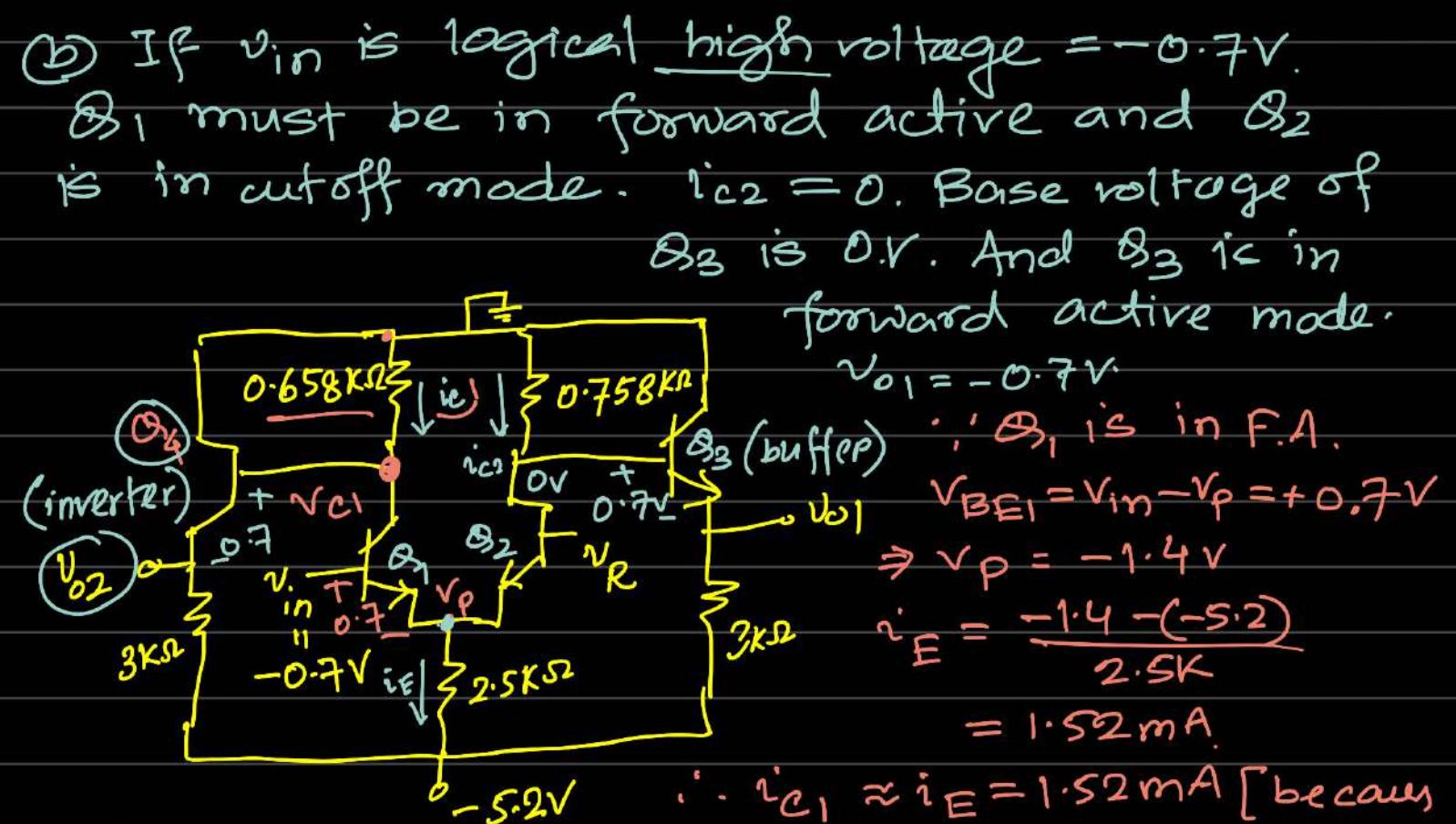
#  $Q_4/Q_3$  's collector terminal is connected to zero. But their base terminals are connected to  $V_B$  with a resistor. Therefore,

∴ We find that base emitter voltage of  $Q_1$  is  $0.7V$ . Hence,  $V_{O2} = -0.7V$ . This is the inverter output voltage when input is low.

This implies  $-0.7V$  is the logical low output voltage.

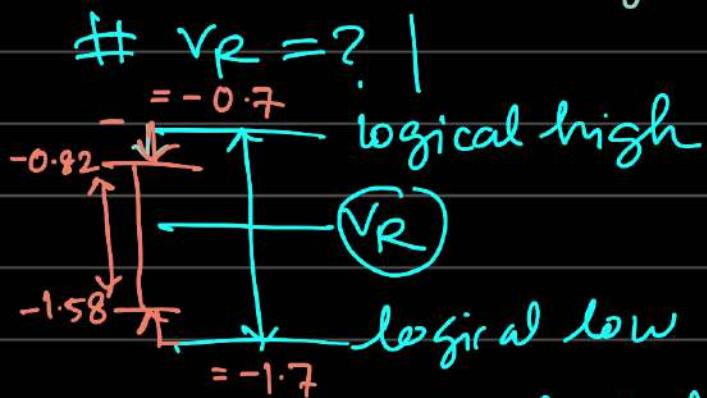
## Rule of thumb for ECL circuits:-

Within ECL logic families we will take logical high/low voltages same for inputs and outputs. Thus, logical high input =  $-0.7\text{ V}$ .



Because of  $\text{Q}_4$  is in forward active mode.  $v_{BE4} = 0.7V \Rightarrow -1 - v_{o2} = 0.7V \Rightarrow v_{o2} = -1.7V$

$\therefore$  Therefore  $v_{o2} = -1.7V$  is the logical output low and logical input low.



We want a symmetry between logical high and low voltages. To achieve that we will choose  $v_R$  midway between two voltages

$$v_R = \frac{\text{logical high} + \text{logical low}}{2}$$

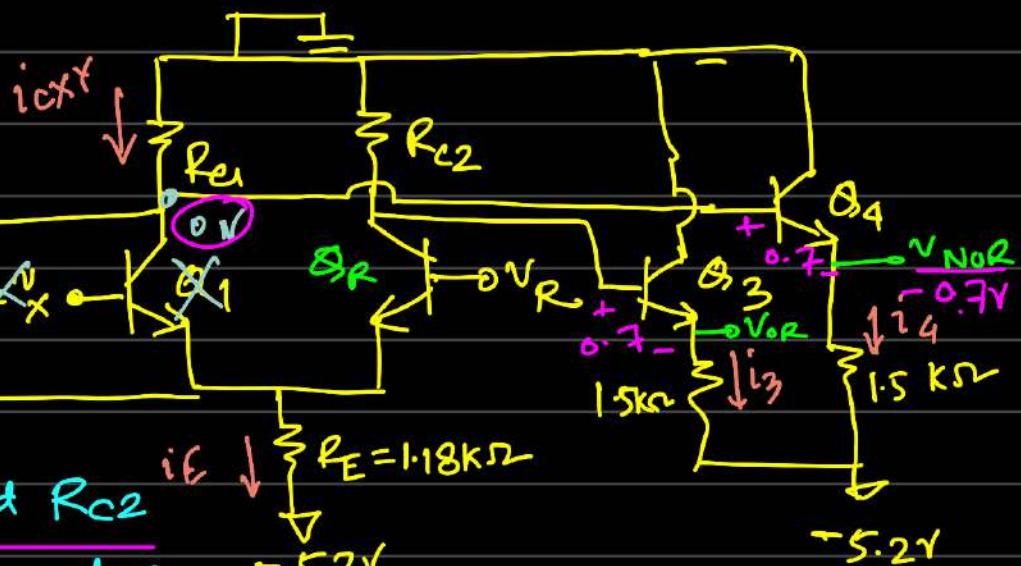
$$= \frac{-0.7 - 1.7}{2} = -1.35V = v_R$$

$$-0.82 < v_R < -1.58$$

## Lecture 11: Reference circuit design, power dissipation and maximum fanout for ECL

Example: 17.2.

Calculate current, resistors and logical value of  $v_Y$  for the basic ECL gate.



are conducting, the B-C voltages are zero.

Solution:  $V_{BC} = 0$  when  $Q_1$  and  $Q_2$  are conducting.

If  $V_x$  and  $V_y$  are logical high, then  $V_{BC} = 0$ .

We can take  $V_x$  and  $V_y$  are logical low, then  $V_{NOR} =$  logical high.  $i_{cx-c} = 0$ .

Remarks:  $Q_4$  and  $Q_3$  is always in forward active. Because assuming transistors are ON, collector voltage is greater than base voltage.

thus we find  $V_{NOR} = -0.7V$  = logical high voltage  
finally, we conclude that  $V_X = V_Y = -0.7V$  = logical  
 high  $V_{BC} = 0V \Rightarrow V_B = V_C = -0.7V = V_X = V_Y$

[Because  $V_x$  and  $V_y$  are base voltages]

$$\text{Then } V_{NOR} = \text{logical low} = -0.7 - 0.7 = -1.4V$$

This implies. logical high =  $-0.7V$ , logical low =  $-1.4V$ .

finally, the reference voltage.  $V_R = \frac{(-0.7) + (-1.4)}{2} = -1.05V$

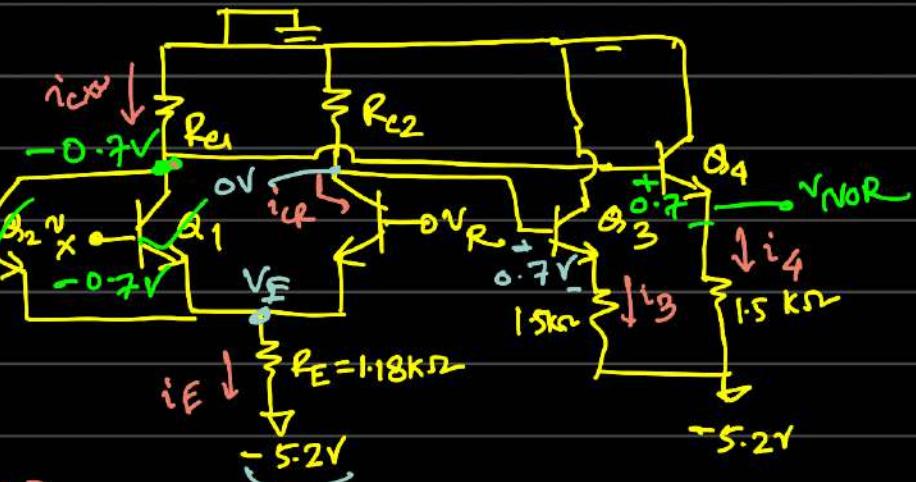
When  $Q_1$  and  $Q_2$  are ON, they operate in forward active mode.

$$V_{BE} = 0.7V$$

$$\Rightarrow V_E = -0.7 - 0.7 = -1.4 \text{ V}$$

Then

$$i_E = \frac{-1.4 - (-5.2)}{1.18 \text{ k}\Omega} = 0.71$$



This current will flow

through the  $R_C$  resistor. Hence,  $i_{CXY} = i_E = 3.22\text{mA}$ .

$$\text{Finally, } R_{C1} = \frac{0 - (-0.7)}{3.22 \text{ mA}} = 0.217 \text{ k}\Omega$$

$$V_{NOR} = -1.4V. \text{ So, } i_4 = \frac{-1.4 - (-5.2)}{1.5K} = 2.53 \text{ mA}$$

$i_{CR} = 0 \text{ mA}$  because all of the current flows through  $R_{CR}$

$$\text{Now, } V_{OR} = -0.7V = \text{logical high, } i_3 = \frac{-0.7 - (-5.2)}{1.5k}$$

If all of the inputs are = 3mA.

logical (ow)

$\Theta_1, \Theta_2 \rightarrow \text{morph}$

$Q_R \rightarrow$  Forward active

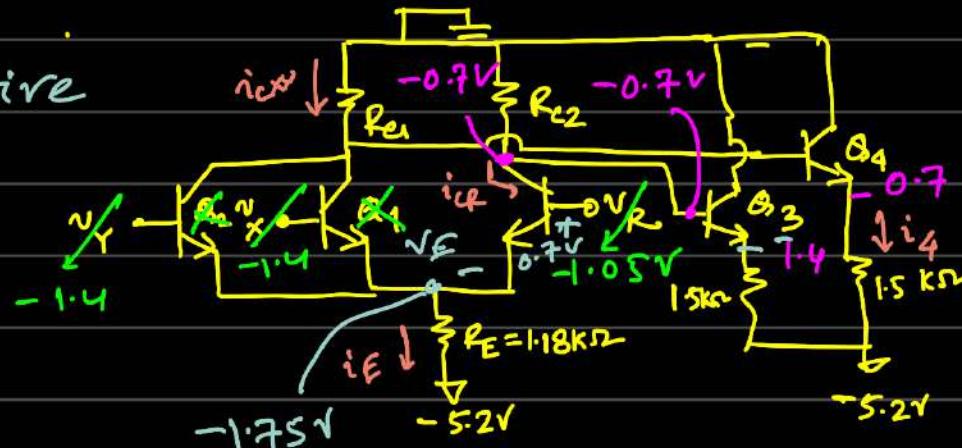
$$S_0. \quad v_F = -1.78 \text{ v.}$$

$$2'E = \frac{-1.75 - (-5.2)}{1.18k}$$

$$= 2.92 \text{ mA}$$

$$i_{cxy} = 0 \text{ mA}$$

$$i_{CR} = i_E = 2.92 \text{ mA}$$



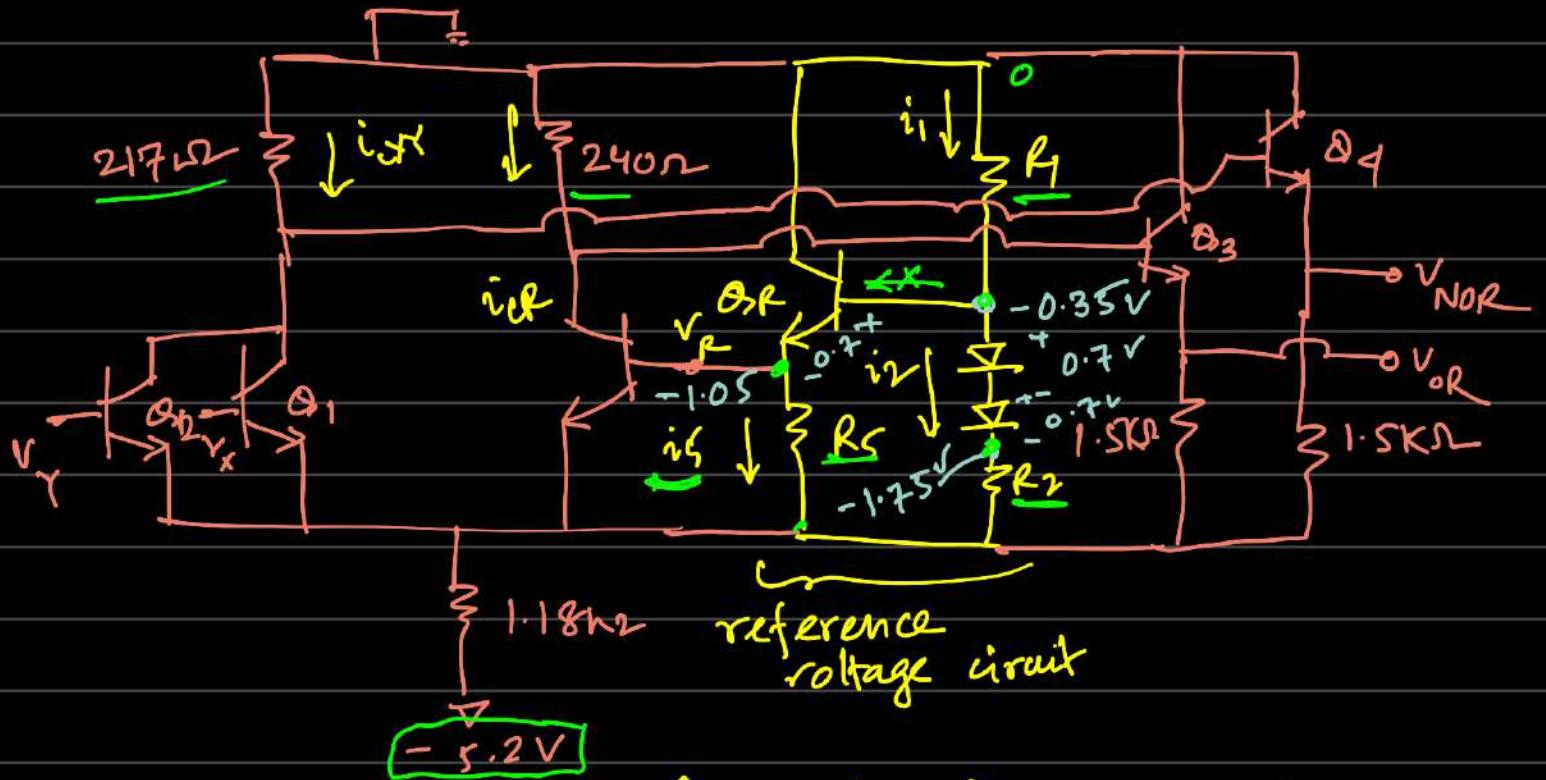
Because the inputs are low.  $V_{NOR} = \text{logical high} = -0.7V$

$V_{OR} = \text{logical low} = -1.4 \text{ V}$ . So the collector voltage of  $Q_2$  transistor must be  $-0.7 \text{ V}$ . [ $Q_3 \rightarrow \text{Forward Active}$ ]

$$2.92 \text{ mA} \downarrow \begin{cases} 0^{\circ} \\ R_{e2} \\ -0.7 \text{ V} \end{cases} \quad \therefore R_{e2} = \frac{0 - (-0.7)}{2.92 \text{ mA}} = 0.24 \text{ k}\Omega$$

# Design the reference voltage circuit.

Given reference circuit find reference voltage.



$V_R = -1.05V$ ,  $Q_R \rightarrow$  forward active, collector voltage  $>$  base voltage.

$$\text{Suppose. } R_1 = 250\Omega \cdot i_1 = \frac{0 - (-0.35)}{0.25k} = 1.4\text{mA} = i_2$$

$$R_2 = \frac{-1.75 - (-5.2)}{1.4\text{mA}} = 2.46\text{k}\Omega.$$

$$\text{Suppose. } i_5 = i_1 \quad R_5 = \frac{-1.05 - (-5.2)}{1.4\text{mA}} = 2.96\text{k}\Omega$$

# Calculate the power dissipation for the following case.

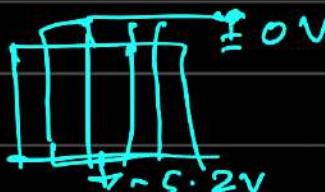
$$V_x = V_r = \text{logic 1} = -0.7V$$

$$\text{So. } Q_1, Q_2 \rightarrow \text{F.A.} \quad V_E = -0.7 - 0.7 = -1.4V. \quad i_E = \frac{-1.4 - (-5.2)}{1.18k}$$

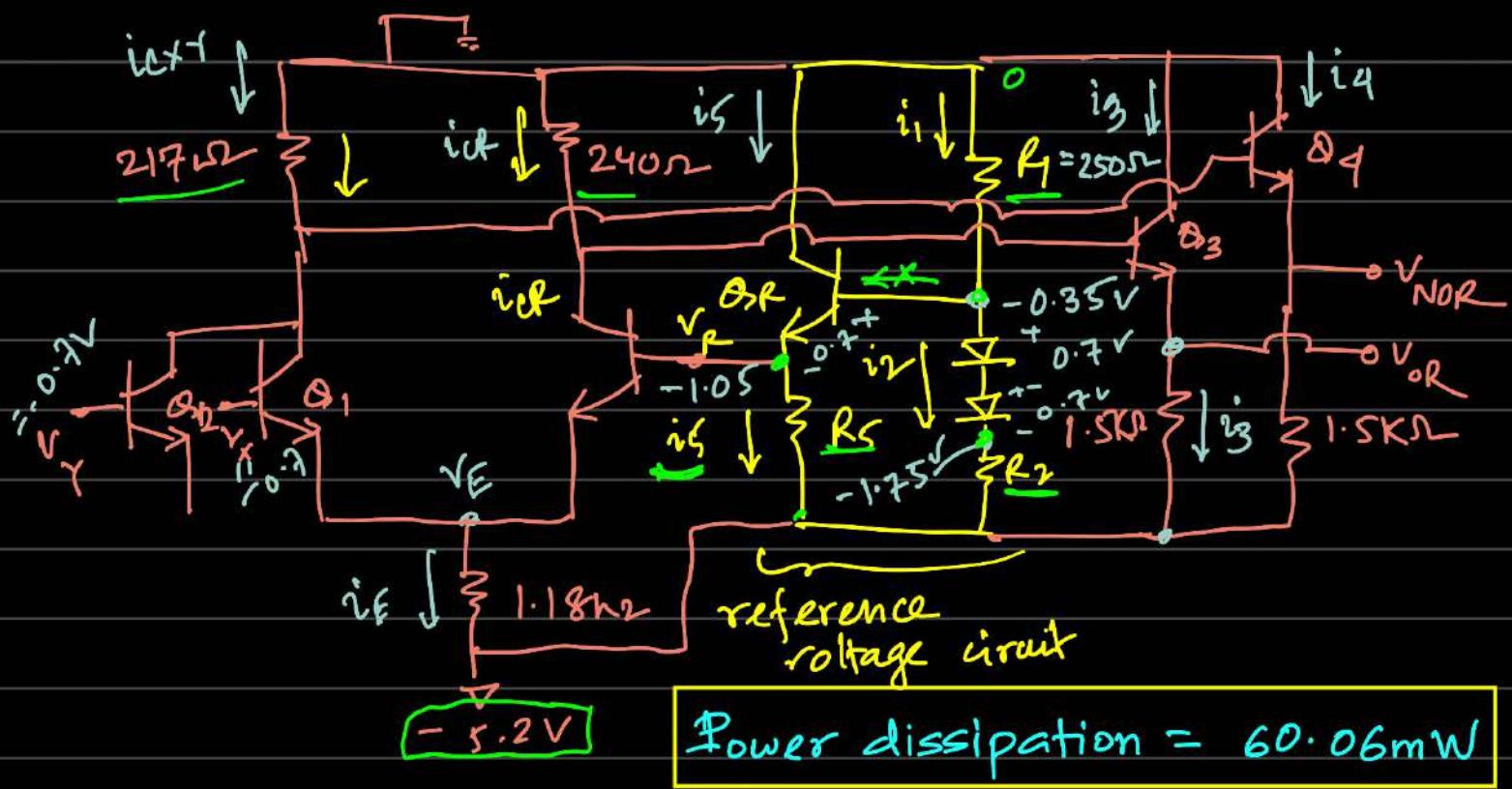
$$i_E = 3.22\text{mA}, \quad i_{CXY} = i_E = 3.22\text{mA}, \quad i_{CR} = 0\text{mA}$$

$$V_{NOR} = -1.4V, \quad V_{OR} = -0.7V, \quad i_3 = \frac{-0.7 + 5.2}{1.5k\Omega} = 3.00\text{mA}$$

$$i_4 = \frac{-1.4 + 5.2}{1.5k\Omega} = 2.53\text{mA}, \quad i_1 = 1.4\text{mA} = i_5$$



$$\begin{aligned} P &= (\Delta V) \cdot (i_{CXY} + i_{CR} + i_5 + i_1 + i_3 + i_4) \\ &= (0 - (-5.2)) (3.22 + 0 + 1.4 \times 2 + 2.53 + 3) \end{aligned}$$



## Fanout calculation: (Example 17.5)

Calculate the maximum fanout based on DC loading effect.

↳ If add load circuits to any output terminal then the voltage at that terminal declines. This is called loading effect.

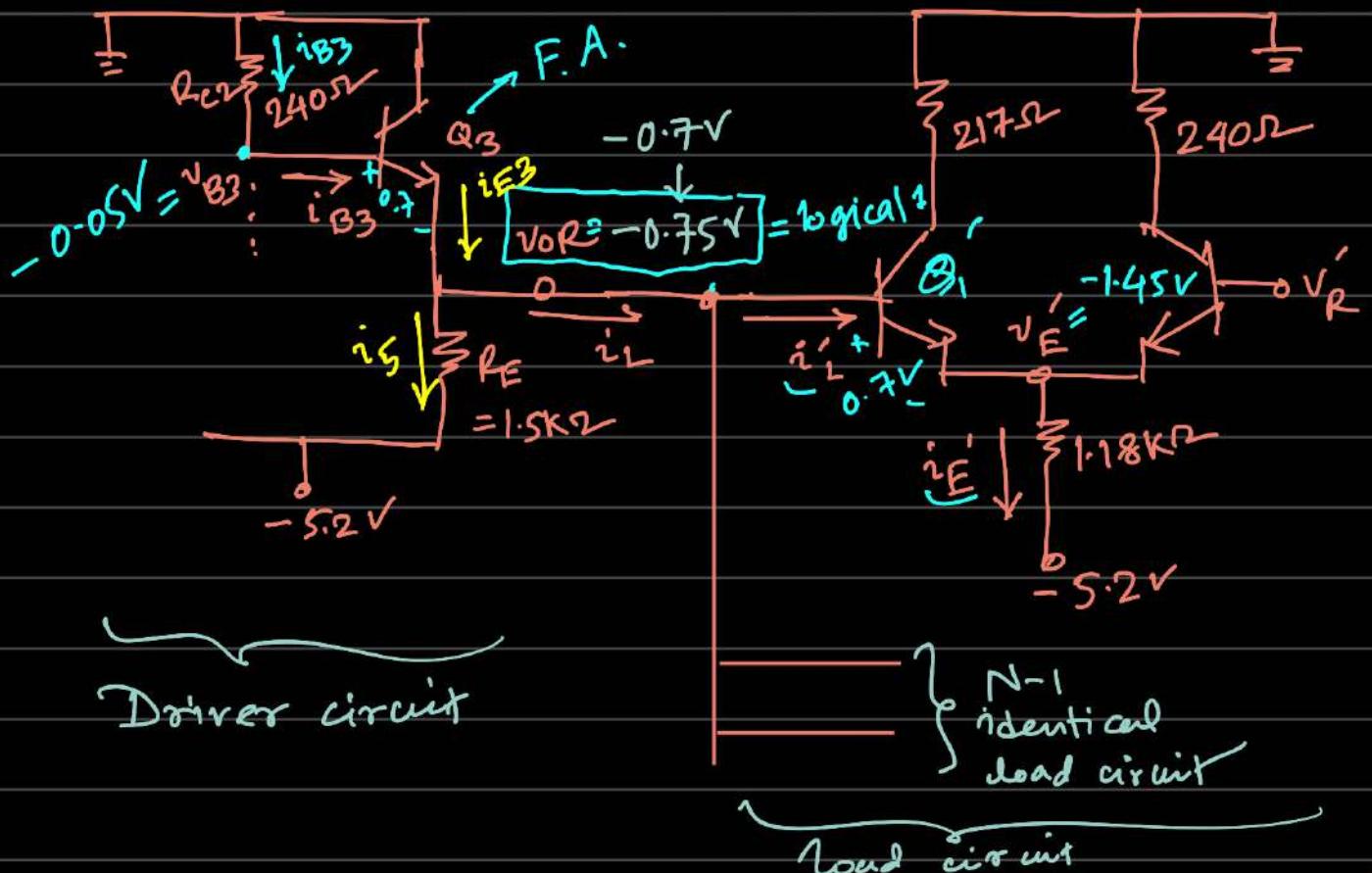
\* Assume the current gain of the transistor is  $\beta = 50$ , which is the worst case scenario. Also assume that the logic level 1 is allowed to decrease by  $50\text{mV}$  at most from a value of  $-0.7V$  to  $-0.75V$ .

Solution: first we calculate the supply current.

$$i_{B3} = \frac{0 - (-0.05)}{0.24\text{K}\Omega} = 0.208\text{mA}$$

$$i_{E3} = (\beta + 1) i_{B3} = 10.625\text{mA}, i_5 = \frac{V_{OR} - (-5.2)}{1.5\text{k}} = 2.967\text{mA}$$

Total supply current,  $i_L = i_{E3} - i_5 = 7.658\text{mA}$



Next we want to calculate individual demand current  $i_1'$   $\rightarrow$  F.A. So.  $i_1' = \frac{-1.45 + 5.2}{1.18k} = 3.118 \text{ mA}$

$$i'_1 = i_{B'} = \frac{i_E'}{\beta + 1} = \frac{3118}{51} = 62.35 \mu A = 0.06235 \text{mA}$$

Individual demand current = 0.06235 mA

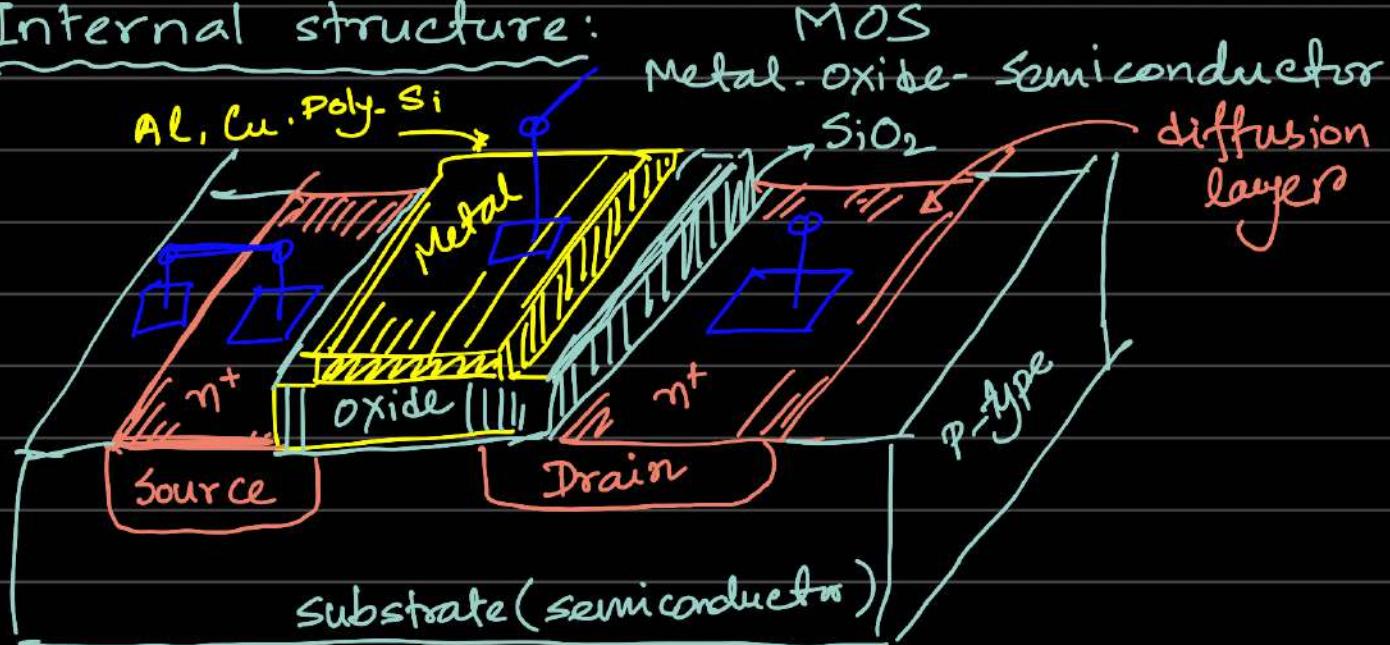
$$\text{Maximum fanout} = \left\lfloor \frac{\text{Supply current}}{\text{Demand current}} \right\rfloor = \left\lfloor \frac{7.658}{0.06235} \right\rfloor = 122.$$

# only ECL circuits would be in Quiz 3 syllabus.

## Lecture 12: MOS logic family

Unipolar logic family : where the current conduction is done by only one type of charge carrier. e.g. electron or hole.

## Internal structure:

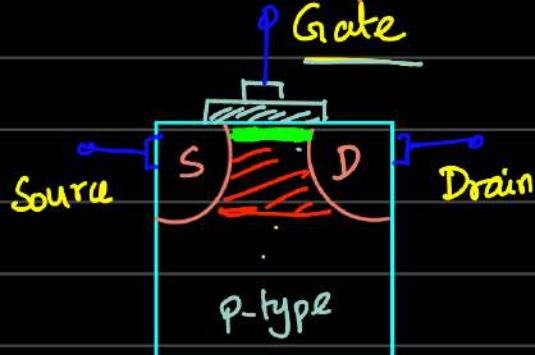


n/p type substrates are usually connected to the lowest voltage terminal in the circuit.  
highest

# substrates - p type. diffusion layer n<sup>+</sup>/p<sup>+</sup> → n channel MOSFET

Basic operation: (n-channel MOS)

# What happens when we change gate voltage  
# If we apply negative voltage to n-MOS gate  
holes will accumulate underneath the oxide layer.  
→ **Accumulation**

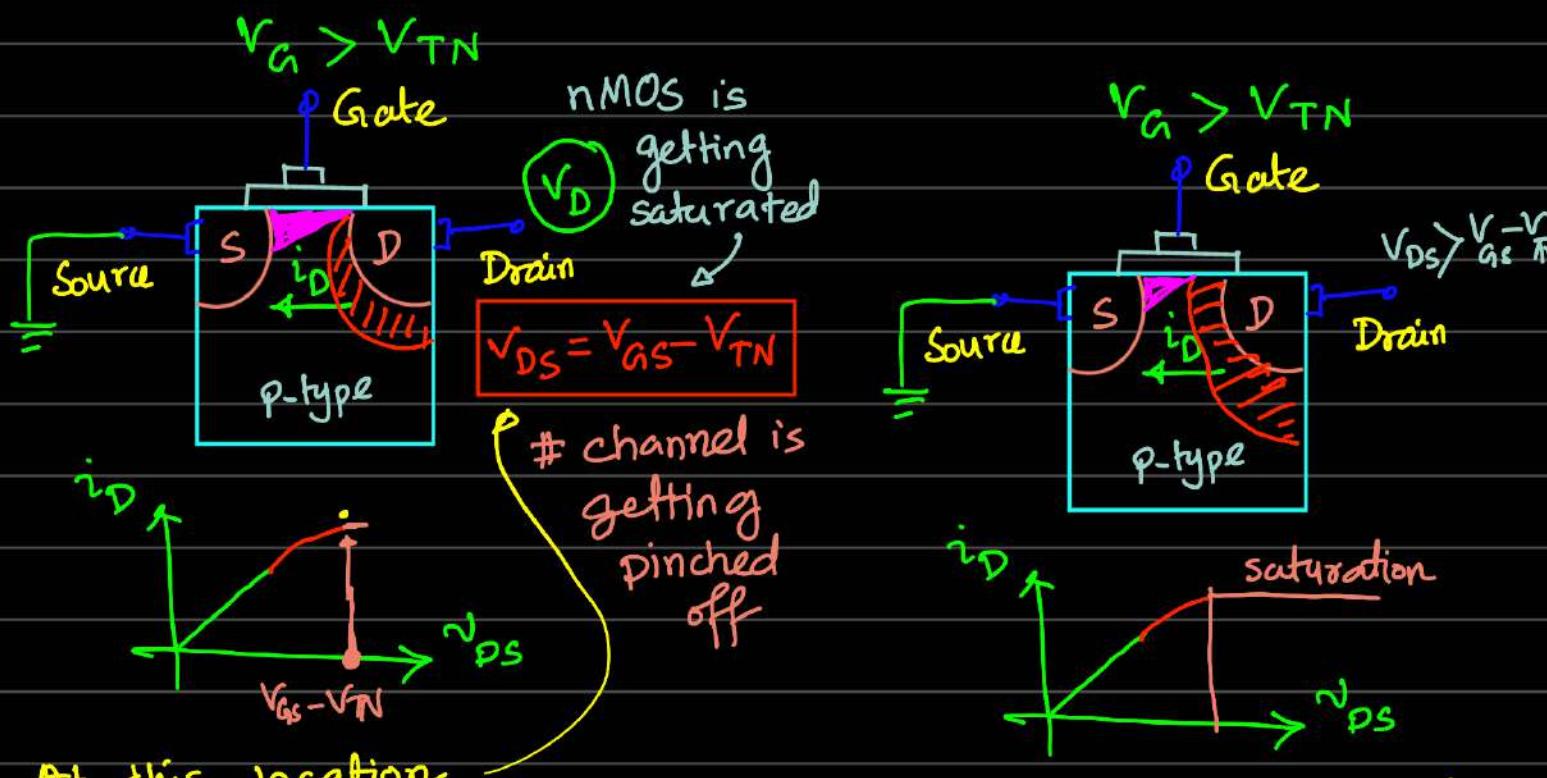
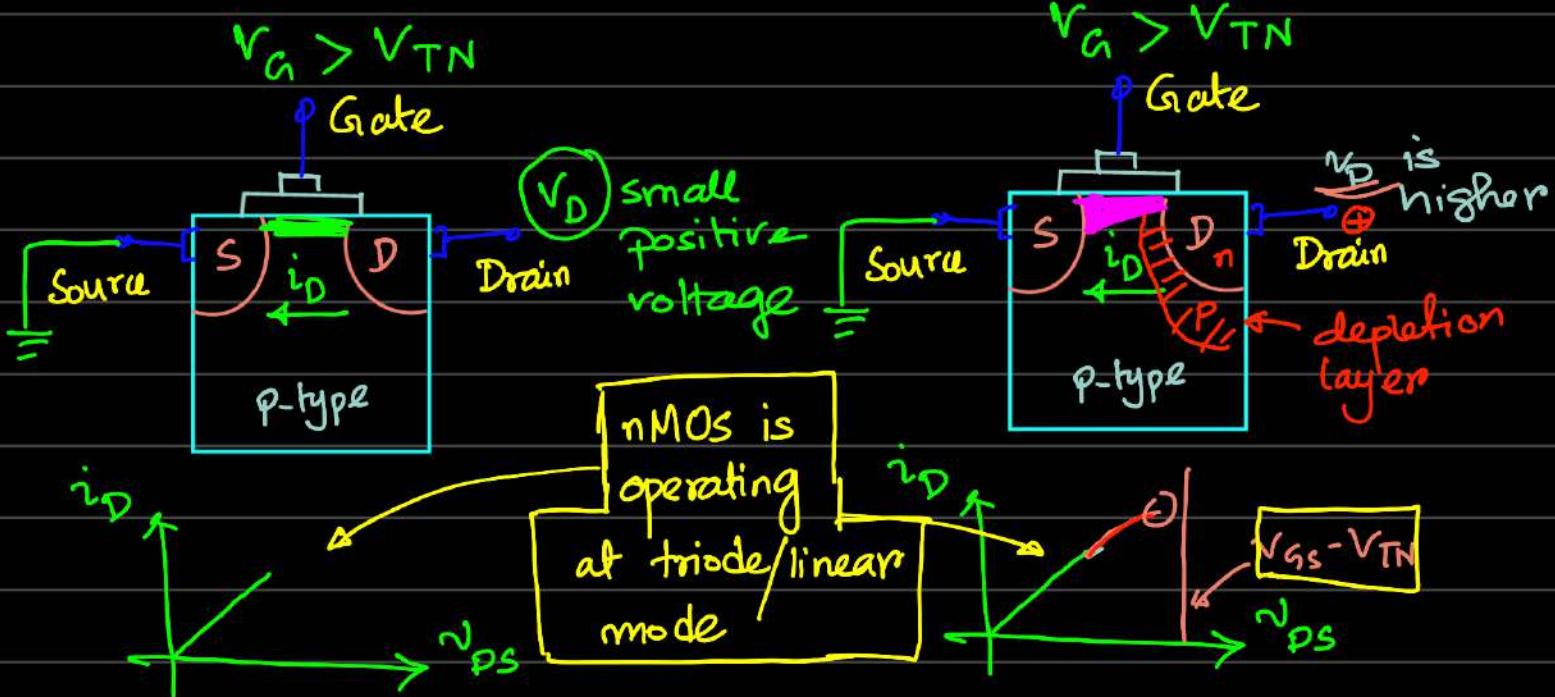


# If we apply positive voltage then depletion layer would form under the oxide layer. → **Depletion**

# finally if we apply voltage higher voltage then an inversion layer would form beneath the channel.  
→ **Inversion**

# This inversion layer is used as channel between drain to source.

# What happens if we change drain voltage when nMOS is in inversion period:



At this location nMOS is at transition point

# nMOS is operating at saturation mode

# Operating mode of MOSFET

① Cutoff

Field effect transistors  $\rightarrow$  Field = Electric

② Linear/Triode

field which is applied using gate voltage and that controls the current inside transistor.

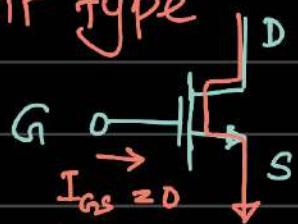
③ Saturation

# For nMOSFET :-

① Enhancement type

n-MOS

$$V_{TN} > 0$$



\* Cutoff:  $V_{GS} < V_{TN}$

\* Triode:  $V_{GS} > V_{TN}$  and

$$V_{DS} \leq V_{GS} - V_{TN}$$

\* Saturation:  $V_{GS} > V_{TN}$

$$\text{and } V_{DS} \geq V_{GS} - V_{TN}$$

$$\text{Transition: } V_{DS} = V_{GS} - V_{TN}$$

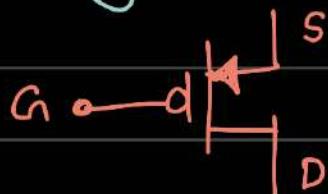
\* Saturation:  $V_{GS} > V_{TN}$

$$\text{and } V_{DS} \geq V_{GS} - V_{TN}$$

# For pMOSFET.

\* Enhancement type - PMOS

$$V_{TP} < 0$$



\* Depletion type PMOS.

$$V_{TP} > 0$$



\* Cutoff:  $V_{SG} = V_S - V_G < |V_{TP}|$

(±)

\* Triode:  $V_{SG} < |V_{TP}|$  and  $V_{SD} \leq V_{SG} + V_{TP}$

\* Saturation:  $V_{SG} < |V_{TP}|$  and  $V_{SD} \geq V_{SG} + V_{TP}$

Transition region:  $V_{SD} = V_{SG} + V_{TP}$

Current - Voltage Relationship :-

N MOS

\* Triode:

$$i_D = K_n [2(V_{GS} - V_{TN})V_{DS} - V_{DS}^2]$$

conduction parameters

\* Saturation:  $V_{DS} = V_{GS} - V_{TN}$

$$i_D = K_n (V_{GS} - V_{TN})^2$$

PMOS

\* Triode:

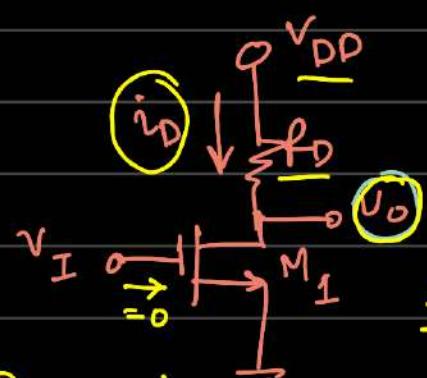
$$i_D = K_p [2(V_{SG} + V_{TP})V_{SD} - V_{SD}^2]$$

\* Saturation:  $V_{SD} = V_{SG} + V_{TP}$

$$i_D = K_p (V_{SG} + V_{TP})^2$$

# # Load line, Quiescent point, NMOS inverter iv - characteristics

# Example: NMOS INVERTER:



Q1 Determine  $V_O$  for  $V_I = 5V$   
and  $V_I = 1.5V$

Specification:-  $V_{DD} = 5V$ ,  $R_D = 20k\Omega$

$V_{TN} = 0.5V$ ,  $K_n = 0.3mA/V^2$

Soln: (a)  $V_I = 5V$ .  $M_1$  is in triode mode.

Reasoning:

Because this might be an inverter, when the input voltage is high, output terminal (drain terminal) might be at smaller voltage. So  $V_{DS} < V_{GS} - V_{TN}$

$$V_{GS} = 5 - 0 = 5V, V_{GS} - V_{TN} = 4.5V > 0.$$

$$i_D = K_n [2(V_{GS} - V_{TN})V_{DS} - V_{DS}^2] = \frac{V_{DD} - V_O}{R_D} \quad [V_{DS} = V_O]$$

$$\Rightarrow 0.3 \frac{mA}{V^2} [2(5 - 0.5)V_O - V_O^2] = \frac{5 - V_O}{20k}$$

$$\Rightarrow 20k\Omega \times 0.3mA [9V_O - V_O^2] = 5 - V_O$$

$$\Rightarrow 6 [9V_O - V_O^2] = 5 - V_O \Rightarrow \boxed{6V_O^2 - 55V_O + 5 = 0}$$

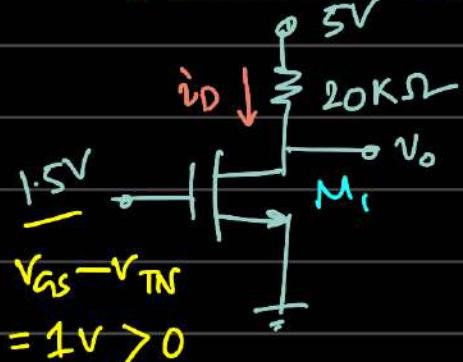
$$V_O = \begin{cases} 9.074V & \rightarrow i_D \text{ would be negative, this solution cannot happen.} \\ 0.092V \end{cases}$$

Verification:  $V_{DS} = 0.092V < (V_{GS} - V_{TN}) = 4.5V$

Therefore, our assumption about  $M_1$  is valid.

(b)  $V_I = 1.5V$

# Assumption:  $M_1$  is in saturation mode.



$$i_D = K_n [V_{GS} - V_{TN}]^2$$

$$= 0.3 [(1.5 - 0.5)]^2 = 0.3mA$$

$$\frac{5 - V_O}{20k} = i_D = 0.3mA \Rightarrow \boxed{V_O = -1V}$$

$V_{DS} = -1V < (V_{GS} - V_{TN}) = 4.5V$ . Our assumption is wrong.

# Therefore,  $M_1$  must be in triode mode.

$$i_D = 0.3m [2(1.5 - 0.5) \cdot V_o - V_o^2] = \frac{5 - V_o}{20k}$$

$$\Rightarrow 0.3V_o^2 + 0.65V_o - 0.25 = 0$$

$$V_o = \begin{cases} \frac{1.667V}{0.5V} \end{cases} \rightarrow V_{DS} = 1.667 > \begin{cases} V_{GS} - V_{TN} \\ = 1V \end{cases}$$

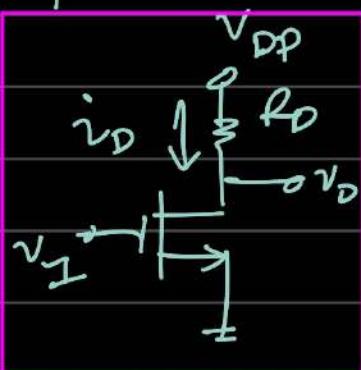
This cannot be the output voltage, because we concluded that  $M_1$  must be in triode.

Therefore,  $V_o = 0.5V$ .

Verification:  $V_{DS} = 0.5 < (V_{GS} - V_{TN}) = 1V$  ✓

Example: Determine the transition point, maximum drain current and maximum power dissipation of an NMOS inverter with resistor.

Specification:  $V_{DD} = 2.5V$ ,  $R_D = 20k\Omega$ ,  $V_{TN} = 0.5V$ ,  $K_n = 0.3mA/V^2$



# Quiz 3 will be held at class time. April 2. UB 80402. or online.

→ Time: 20/25 min

→ Syllabus: ECL logic family.

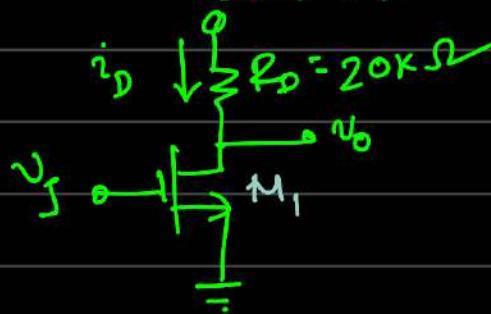
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# Lecture 13: MOS logic family. CMOS logic-circuit

Example: Determine the transition point, maximum drain current and maximum power dissipation of an NMOS inverter with resistor.

Specification:  $V_{DD} = 2.5V$ ,  $R_D = 20k\Omega$ ,  $V_{TN} = 0.5V$ ,  $K_n = 0.3mA/V^2$

Sol<sup>n</sup>:  $\sqrt{V_{DD}(2.5V)}$



Observation: When output ( $V_O$ )

has the smallest value then  $i_D = \frac{V_{DD} - V_O}{R_D}$  would have a maximum value. Therefore, maximum input voltage is needed to produce this output value.

We can take maximum value of input voltage at  $2.5V$ .

$$V_I = 2.5V \quad [M_1 \rightarrow \text{triode}]$$

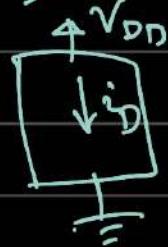
$$i_D = \frac{2.5 - V_O}{20k} = 0.3m \left[ 2(2.5 - 0.5) V_O - V_O^2 \right]$$

$$\Rightarrow 6V_O^2 - 25V_O + 2.5 = 0. \quad V_O = \begin{cases} 0.1025V \\ 4.064V \end{cases}$$

$V_O \neq 4.064V$  because that will produce negative  $i_D$ .

$$V_O = 0.1025V \quad [\text{verify: } 0.1025 < (V_{GS} - V_{TN}) = 2V]$$

$$i_D = \frac{2.5 - 0.1025}{20k} = [0.1198mA]$$



$$P = \Delta V I = (V_{DD} - 0) i_D = 2.5 \times 0.1198$$

$$\text{maximum power dissipation} = [0.3mW]$$

Transition point:  $V_{DS} = V_{GS} - V_{TN}$

at transition point,  $i_D = K_n (V_{GS} - V_{TN})^2$

$$i_D = \frac{V_{DD} - V_O}{R_D} = K_n (V_{GS} - V_{TN})^2 = K_n V_O^2$$

$$\Rightarrow \frac{2.5 - V_O}{20k} = 0.3m \cdot V_O^2 \Rightarrow 6V_O^2 + V_O - 2.5 = 0$$

$$V_o = \begin{cases} 3.4051 \text{ V} & \rightarrow \text{if it were the soln, it would be negative.} \\ 0.5675 \text{ V} \end{cases}$$

∴ At transition point  $V_o = 0.5675 \text{ V}$

$$V_J = V_o + V_{TN} = 1.0675 \text{ V}$$

## NMOS NOR GATE EXAMPLE

$$V_{DD} = 5 \text{ V}$$

Objective: Determine the current and voltages in this gate for different input conditions:

$$R_D = 20 \text{ k}\Omega, K_n = 0.1 \text{ mA/V}^2$$

$$V_{TN} = 0.8 \text{ V}$$

Sol<sup>n</sup>: ① Case 1:  $V_1 = V_2 = 0 \text{ V}$ .

For  $M_1$ , we have  $V_{GS1} = V_{G1} - V_{S1} = 0 - 0 = 0 < 0.8 \text{ V}$

"  $M_2$  " "  $V_{GS2} = V_{G2} - V_{S2} = 0 < 0.8 \text{ V}$

Therefore,  $M_1$  and  $M_2$  are in cutoff mode.

$$I_{D1} = I_{D2} = i_D = 0. V_o = V_{DD} = 5 \text{ V}$$

② Case 2:  $V_1 = 5 \text{ V}$  and  $V_2 = 0 \text{ V}$ .

Since  $V_{GS2} = 0 < 0.8$ ,  $M_2$  must be in cutoff.  $I_{D2} = 0$

So, we can assume  $M_1$  is operating in triode region.

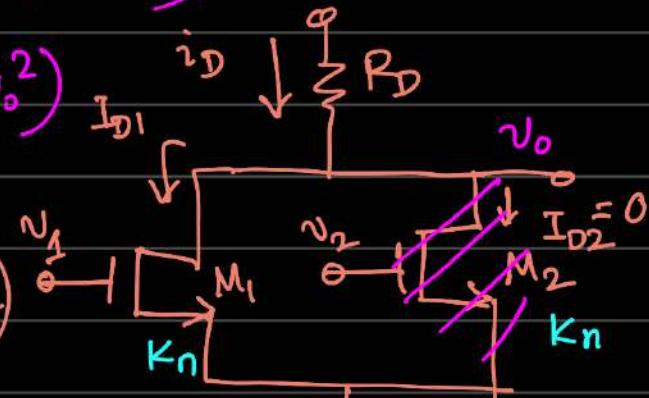
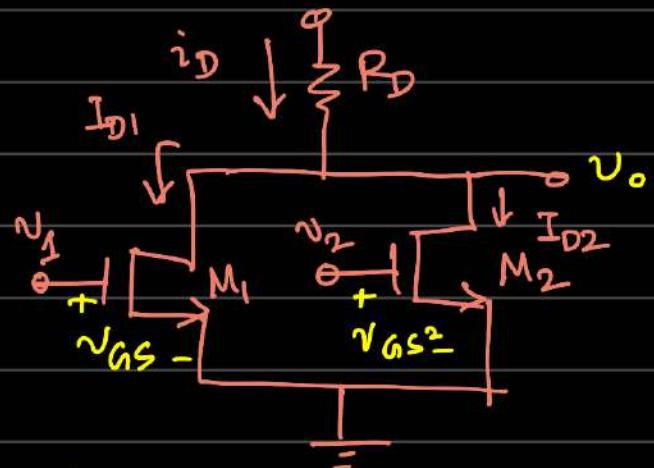
$$i_D = \frac{V_{DD} - V_o}{R_D} = K_n (2(V_{GS} - V_{TN}) V_{DS} - V_{DS}^2) \quad V_{DD} = 5 \text{ V}$$

$$\Rightarrow \frac{5 - V_o}{20 \text{ k}} = 0.1 \text{ m} (2(5 - 0.8) V_o - V_o^2)$$

$$\Rightarrow 2V_o^2 - 9.4V_o + 5 = 0$$

$$V_o = \begin{cases} 8.6 \text{ V} & \rightarrow (i_D < 0, \text{ impossible}) \\ 0.29 \text{ V} & \therefore V_o = 0.29 \text{ V} \end{cases}$$

$$i_D = I_{D1} = \frac{5 - 0.29}{20} = 0.2354 \text{ mA}$$



Case 3:  $V_1 = 0V, V_2 = 5V$ .  $M_1 \rightarrow \text{cutoff}, M_2 \rightarrow \text{Triode}$ ,

$V_o = 0.29V, i_D = 0.2354 \text{ mA} \quad [k_{n1} \neq k_{n2}]$

$I_{D1} = 0 \text{ mA}, I_{D2} = 0.2354 \text{ mA}$ .

Case 4:  $V_1 = V_2 = 5V$

Assuming,  $M_1$  and  $M_2$  are in triode region.

Reasoning: Because both inputs are high we might expect very low output voltage or drain voltage. ( $V_{DS} < V_{GS} - V_{TN}$ )

$$i_D = I_{D1} + I_{D2}$$

$$\Rightarrow \frac{5 - V_o}{20k} = 0.1m [2 \times (5 - 0.8)V_o - V_o^2] \times 2$$

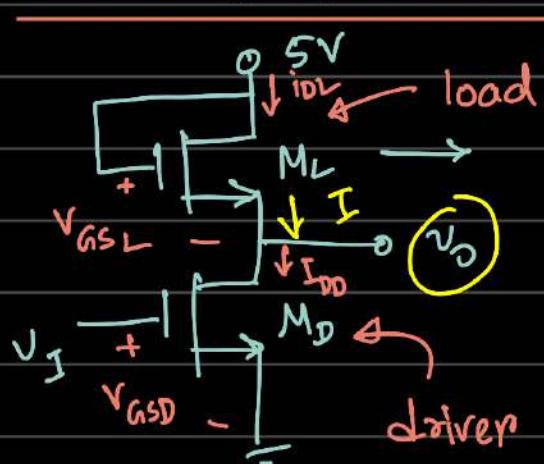
$$\Rightarrow 8V_o^2 - 34.6V_o + 5 = 0. \quad V_o = \begin{cases} 4.17V \\ 0.149V \end{cases} \rightarrow \text{Check yourself!}$$

$V_o \neq 4.17V$  because,  $V_{DS} = 4.17V$  which is much large value

$$V_o = 0.149V, i_D = \frac{5 - 0.149}{20k} = 0.243 \text{ mA}$$

$$I_{D1} = I_{D2} = \frac{i_D}{2} = 0.121 \text{ mA}$$

### NMOS INVERTER with ENHANCEMENT LOAD



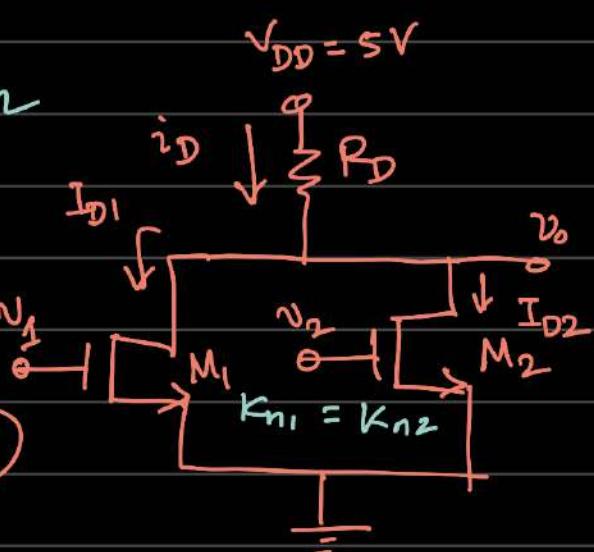
load nMOS is going to be enhancement type.

Determine the DC currents and voltages in the circuit containing enhancement load.

This is only true for MOSFET

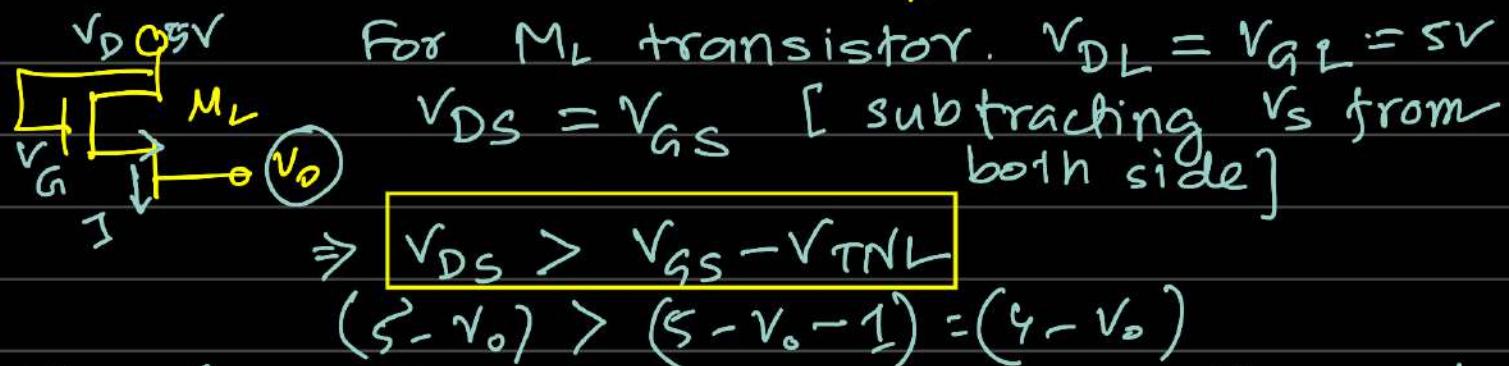
Specifications:  $V_{TNL} = V_{TND} = 1V, k_{nD} = 50 \mu A/V^2$

$k_{nL} = 10 \mu A/V^2$ . Determine  $V_o$ , when  $V_I = 5V$  and  $V_I = 1.5V$ .



## Lecture 14: CMOS logic families

Sol<sup>n</sup>: Case 1:  $V_I = 0V$ .  $V_{GSD} = 0 < V_{TNL} = 1V$   
 So  $M_D$  would be in cutoff mode.  $I = 0mA$ .



Therefore,  $M_L$  must be in saturation mode.

$I = i_{DL} =$  drain current for  $= 0$   
 load MOSFET

$$\therefore K_{nL} (V_{GSL} - V_{TNL})^2 = 0 \Rightarrow V_{GSL} = V_{TNL}$$

$$\Rightarrow V_{GL} - V_{SL} = V_{TNL} \Rightarrow 5 - V_o = 1 \Rightarrow V_o = 4V$$

Case 2:  $V_I = 5V$ . We are assuming  $M_D$  might be in triode region.

$5V = V_{DD}$

$$I_{DD} = K_{nD} (2(V_{GSD} - V_{TND}) V_{DSD} - V_{DS}^2)$$

$$I_{DL} = K_{nL} (V_{GSL} - V_{TNL})^2$$

Using KCL we can write.

$$I_{DD} = I_{DL}$$

$$\Rightarrow 0.05 [2(5 - 0 - 1) V_o - V_o^2] = 0.01 (5 - V_o - 1)^2$$

$$\Rightarrow 6V_o^2 - 48V_o + 16 = 0$$

$$V_o = \begin{cases} 7.65V & \rightarrow \text{because this higher than } V_{DD} \\ 0.34V & \rightarrow I_{DL} = K_{nL} (V_{GSL} - V_{TNL})^2 \\ & = 0.01 (5 - 0.34 - 1)^2 = 0.133mA \end{cases}$$

Verification:  $V_{DS} = 0.34 < V_{GSD} - V_{TNL}$   
 $5 - 1 = 4 \quad \checkmark$

Case ③.  $V_1 = 1.5V$ .  $M_2 \rightarrow \text{sat}$ ,

Assuming  $M_D \rightarrow \text{sat.}$

$$I_{DD} = I_{D2} \Rightarrow k_{nL} (V_{GSL} - V_{TNL})^2 = k_{nD} (V_{GSD} - V_{TND})^2$$

$$\Rightarrow 0.01 (5 - v_o - 1)^2 = 0.05 (1 \cdot 5 - 1)^2$$

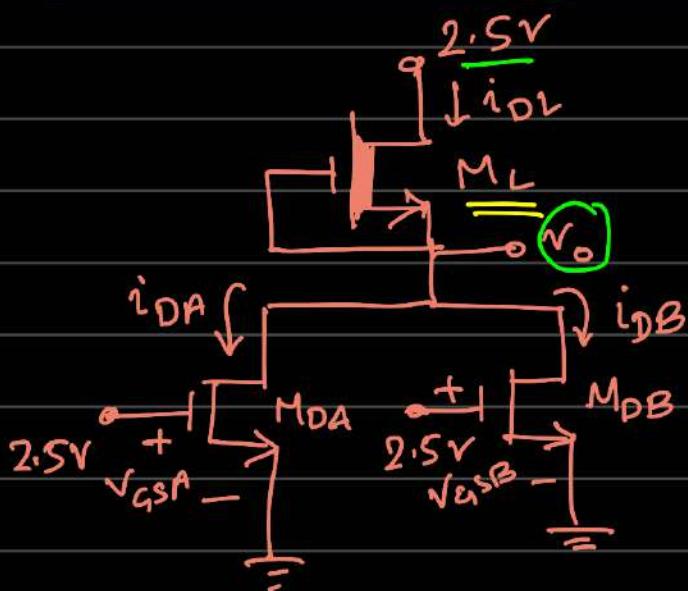
$$\Rightarrow v_o = 2.88 \text{ V.} \Rightarrow v_{DS} = 2.88 > \frac{1 \cdot 5 - 1}{0.5} \text{ V.}$$

$$I_D = 0.05 (1.5 - 1)^2 \text{ mA} = 1.25 \times 10^{-2} \text{ mA.}$$

Our assumption is valid for  $M_D$ .

quiz 4

## NMOS NOR gate with Depletion Load



Determine the low output voltage for this nMOS NOR gate.

$$k_n' = 100 \mu A/V^2, V_{TND} = 0.4 V$$

Here.  $k_n' \left( \frac{W}{L} \right) = K_n$  = conduction parameter

Sol<sup>n</sup>: Observation: For M<sub>L</sub> depletion type nMOS we can see that  $V_{GS} = 0 < V_{TNL} = -0.6V$ . Therefore M<sub>L</sub> is always ON, regardless of input voltages. For this particular case V<sub>O</sub> might be small. Because it is a NOR gate.

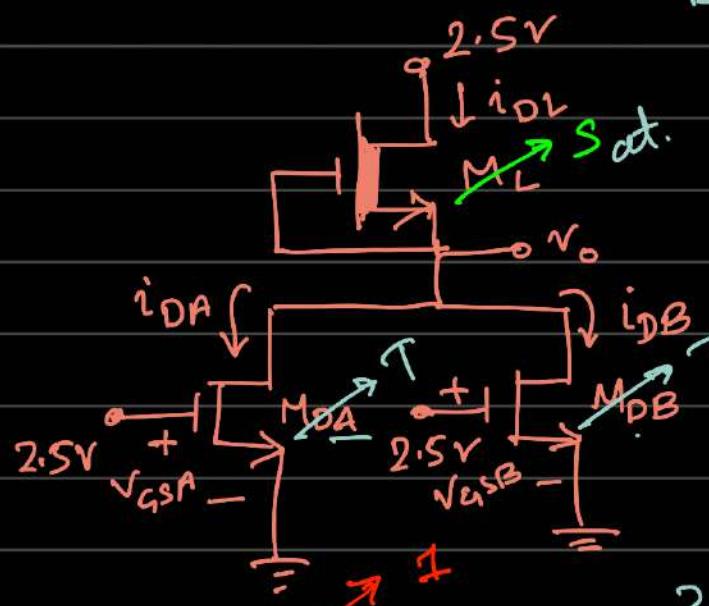
$$v_{DSL} = 2.5 - \underline{v_0} > v_{ASI} - v_{T_{NL}}$$

$$= 0 - (-0.6) = 0.6$$

| We can expect  
| that  $M_L$  is in  
| saturation.

If we can also expect  $M_{DA}$  and  $M_{DB}$  to be in triode mode cause  $V_{DA} = V_{DB} = V_o$

is small.



$$i_{DL} = i_{DA} + i_{DB}$$

$$\Rightarrow K_{nL} (V_{GSL} - V_{TNL})^2$$

$$= K_{nA} (2(V_{GSA} - V_{TNA}) V_{DSA} - V_{DSA}^2) + K_{nB} (2(V_{GSB} - V_{TNB}) V_{DSB} - V_{DSB}^2)$$

$$V_{TND} = V_{TNA} = V_{TNB}$$

$$\Rightarrow \underbrace{K_n \left( \frac{W}{L} \right)}_{K_{nL}} \left( 0 - (-0.6) \right)^2 = \cancel{K_n \left( \frac{W}{L} \right)}_{DA} \left( 2(2.5 - 0 - 0.4) V_o - V_o^2 \right) + \cancel{K_n \left( \frac{W}{L} \right)}_{DB} \left( 2(2.5 - 0 - 0.4) V_o - V_o^2 \right)$$

$$\Rightarrow 4V_o^2 - 16.8V_o + 0.36 = 0 \Rightarrow V_o = \begin{cases} 4.178V \\ 0.02153V \end{cases}$$

$V_o \neq 4.178V$  because it is greater than  $V_{DD} = 2.5V$

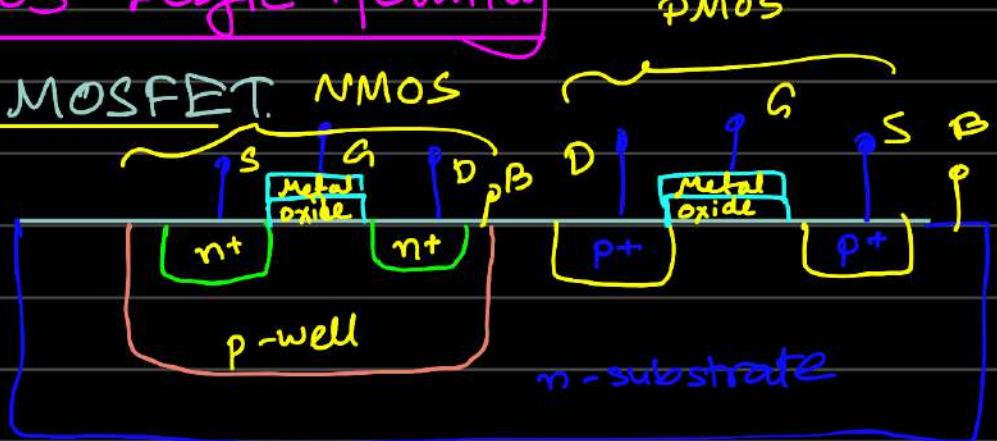
$$\therefore V_o = 0.02153V. \quad i_{DL} = K_n \left( \frac{W}{L} \right) \left( V_{GSL} - V_{TNL} \right)^2 = 0.1m \cdot 1 \cdot \left( 0 - (-0.6) \right)^2 = 0.036mA.$$

$$i_{DA} = K_n \left( \frac{W}{L} \right)_{DA} \left( 2(V_{GSA} - V_{TNA}) V_{DSA} - V_{DSA}^2 \right) = 0.018mA$$

$$i_{DB} = K_n \left( \frac{W}{L} \right)_{DB} \left( 2(V_{GSB} - V_{TNB}) V_{DSB} - V_{DSB}^2 \right) = 0.018mA$$

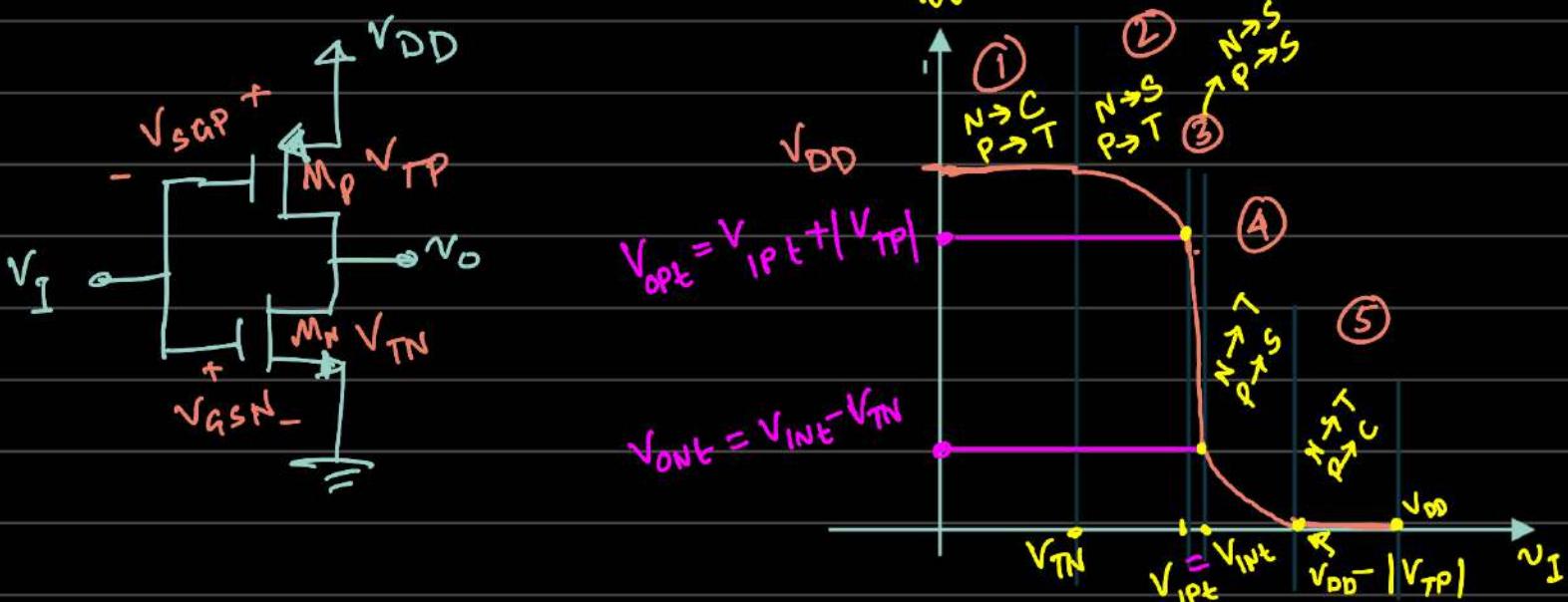
## CMOS logic family

Complementary MOSFET



# CMOS Transfer Characteristics:

CMOS Inverter circuit.



Region ①: when  $V_I < V_{TN}$ ,  $M_N$  is in cutoff and  $M_P$  is in triode mode.  $V_o = V_{DD}$

Region ②: when  $V_{TN} < V_I < V_{IPT}$  = transition input voltage.  $M_P$  is in triode mode.  $M_N$  is in saturation mode.

Region ③.  $V_{IPT} < V_I < V_{INT}$ ,  $V_{IPT} = V_I = V_{INT}$   
 $M_P$  and  $M_N$  are in saturation mode.

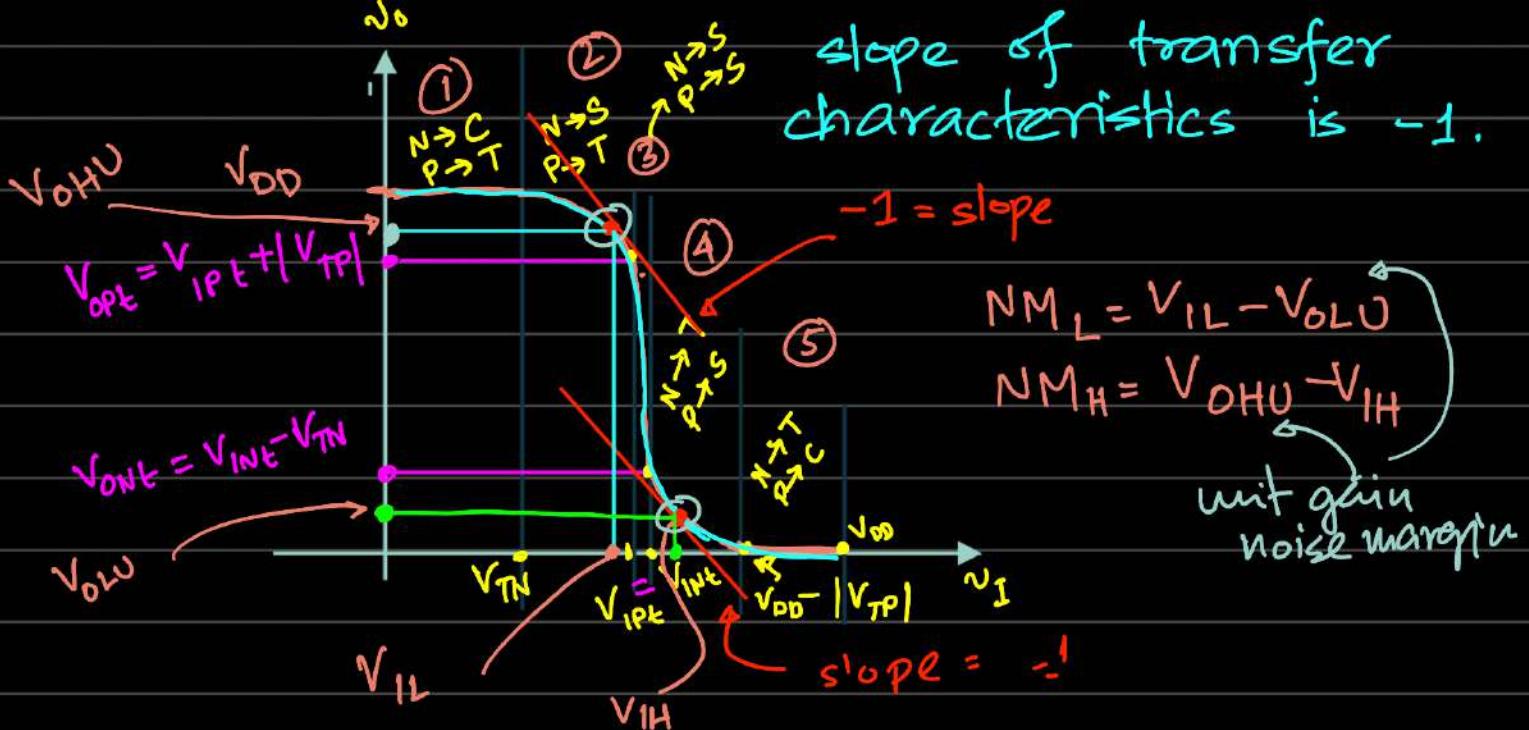
Region ④  $V_{INT} < V_I < V_{DD} - |V_{TP}|$   
 $M_P$  is in saturation mode and  $M_N$  is in triode mode.

Region ⑤.  $V_{DD} - |V_{TP}| < V_I$ ,  $M_P$  is in cutoff mode and  $M_N$  is in triode mode.  $V_o = 0V$ .

## CMOS INVERTER NOISE MARGIN

Unit gain Noise margin:

We would set the noise voltages for input and output levels where the

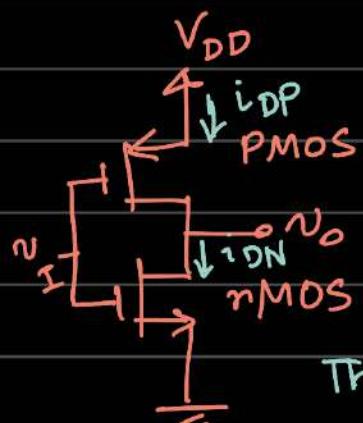


## Lecture 15: CMOS Logic family.

$$\text{differential gain} = \frac{dv_o}{dv_I}$$

$$\text{unit gain} \Rightarrow \left| \frac{dv_o}{dv_1} \right| = 1 \quad / \quad \frac{dv_o}{dv_1} = -1$$

Example: 16.9 Determine the noise margins of a CMOS inverter.



Specifications:  $V_{DD} = 3.3V$ ,

$$(k_n = k_p = 50 \mu A/\sqrt{2})$$

$$V_{TN} = -V_{TP} = 0.4V \Rightarrow V_{TP} = -0.4V$$

# V<sub>OHU</sub> and V<sub>IL</sub> calculation:

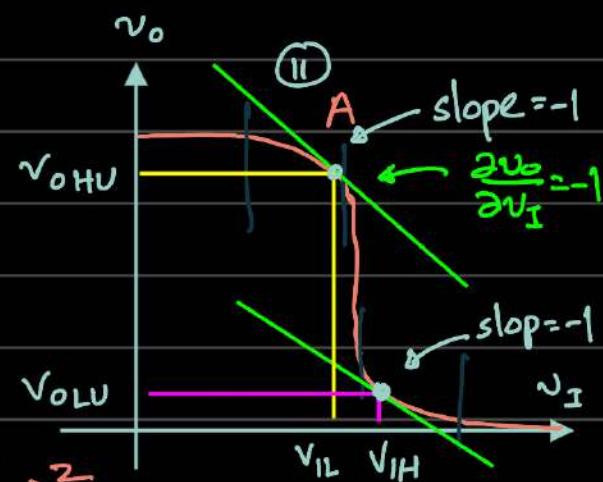
1 This point belongs to region (II) of transfer characteristics curve. Therefore,

NMOS and PMOS would operate in saturation and triode respectively. According to KCL

$$i_{DP} = i_{DN}$$

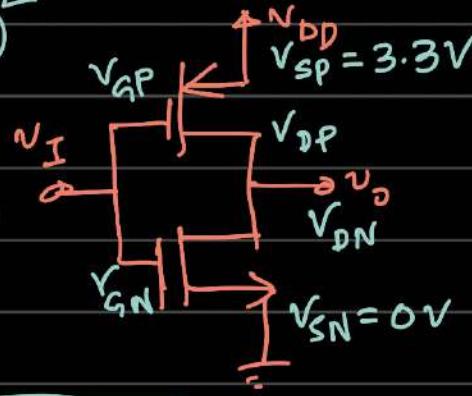
$$\Rightarrow \cancel{K_p} (2(\sqrt{s_{GP}} + \sqrt{s_{TP}}) \sqrt{s_{SDP}} - \sqrt{s_{SDP}}^2) =$$

$$K_n (\sqrt{\sigma_{SN}} - \sqrt{\sigma_{TN}})^2$$



$$\Rightarrow 2(V_{SP} - V_{GP} + V_{TP})(V_{SP} - V_{DP}) - (V_{SP} - V_{DP})^2 = (V_{GN} - V_{SN} - V_{TN})^2$$

$$\Rightarrow 2(3.3 - V_I - 0.4)(3.3 - V_o) - (3.3 - V_o)^2 = (V_I - 0 - 0.4)^2$$



Let,  $3.3 - V_o = Y \cdot [V_I - 0.4 = X] \Rightarrow V_I = X + 0.4$

$$\Rightarrow 2(3.3 - (X + 0.4) - 0.4)Y - Y^2 = X^2$$

$$\Rightarrow 2(2.5 - X)Y - Y^2 = X^2 = X^2 + Y^2 + 2XY - 5Y = 0 \quad \checkmark$$

$$\frac{dV_o}{dV_I} = -1 \Rightarrow \frac{dY}{dX} = \left( \frac{dV_I}{dX} \right) \left( \frac{dV_o}{dV_I} \right) \left( \frac{dY}{dV_o} \right)^{-1} = 1 \quad \left| \frac{dY}{dX} = 1 \right.$$

$$\frac{dV_I}{dX} \cdot \frac{d(X + 0.4)}{dX} = 1, \quad \frac{dY}{dV_o} = \frac{d(3.3 - V_o)}{dV_o} = -1$$

We want to find  $X, Y$  where  $\frac{dY}{dX} = 1$

$$\frac{d}{dX}(X^2 + Y^2 + 2XY - 5Y) = 0$$

$$\frac{d(fg)}{dx} = f \frac{dg}{dx} + g \frac{df}{dx}$$

$$\Rightarrow 2X + 2Y \frac{dY}{dX} + 2Y + 2X \frac{dY}{dX} - 5 \frac{dY}{dX} = 0$$

$$\Rightarrow 2X + 2Y + 2Y + 2X - 5 = 0 \Rightarrow 4X + 4Y - 5 = 0$$

$$Y = \frac{5}{4} - X \quad | \quad \left( \frac{5}{4} - X \right)^2 + X^2 + 2X\left( \frac{5}{4} - X \right) - 5\left( \frac{5}{4} - X \right) = 0$$

$$\Rightarrow X = \frac{15}{16}, \quad Y = \frac{5}{16}$$

$$V_I = X + 0.4 = V_{IL} = 1.3375$$

$$3.3 - V_o = Y \Rightarrow V_o = 3.3 - Y = V_{OHU} = 2.9875V$$

#  $V_{IH}$  and  $V_{OLU}$  calculation:

This point belongs to region IV. Therefore NMOS and PMOS will operate in triode and saturation mode respectively. Using KCL we get.

$$i_{DN} = i_{DP}$$

$$\cancel{K_p [2(V_{ASN} - V_{TN}) V_{DSN} - V_{DSN}^2]} \\ = \cancel{K_p (V_{SGP} + V_{TP})^2}$$

$$\Rightarrow 2(V_I - 0 - 0.4) V_o - V_o^2 = (3.3 - V_I - 0.4)^2$$

$$+ X = +V_I - 0.4, \quad + Y = +V_o$$

$$\Rightarrow 2X - Y^2 = (3.3 - (X + 0.4) - 0.4)^2 = (2.5 - X)^2$$

$$\Rightarrow X^2 + Y^2 - 2XY - 5X + 6.25 = 0$$

$$\Rightarrow \frac{d}{dX} (X^2 + Y^2 - 2XY - 5X + 6.25) = 0$$

$$\Rightarrow 2X + 2Y \frac{dY}{dX} - 2Y - 2X \frac{dY}{dX} - 5 = 0$$

$$\Rightarrow 2X + 2Y(-1) - 2Y - 2X(-1) - 5 = 0$$

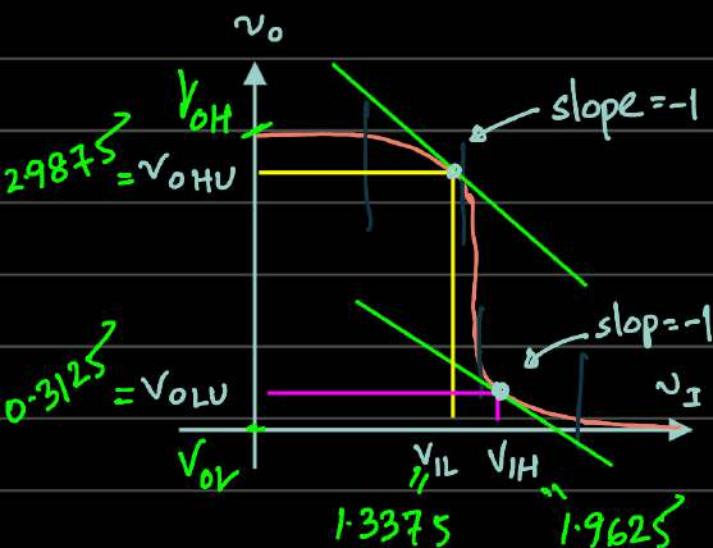
$$\Rightarrow 4X - 4Y - 5 = 0 \quad \Rightarrow \boxed{X = Y + 1.25}$$

$$(Y + 1.25)^2 + Y^2 - 2Y(Y + 1.25) - 5X + 6.25 = 0$$

$$\Rightarrow Y = 0.3125 = V_o \quad \text{and} \quad V_I = X + 0.4 = 1.9625 V$$

$$X = Y + 1.25$$

$$V_{OLU} = 0.3125 \quad \text{and} \quad V_{IH} = 1.9625 V$$



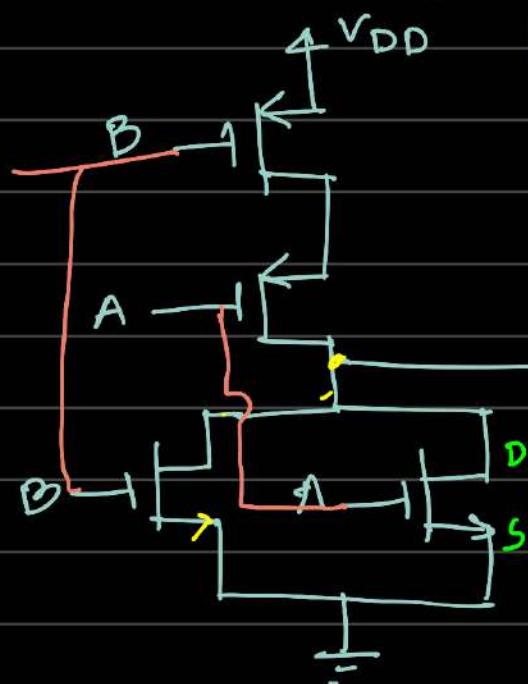
$$NM_L = V_{IL} - V_{OLU} \\ = 1.3375 - 0.3125 \\ = 1.025 V$$

$$NM_H = V_{o_HU} - V_{IH} \\ = 2.9875 - 1.9625 \\ = 1.025 V$$

$$\text{Noise margin, } NM = \min(NM_L, NM_H) \\ = 1.025 V$$

# CMOS logic Gate Construction

\* CMOS NOR gate:  $Y = \overline{A+B}$

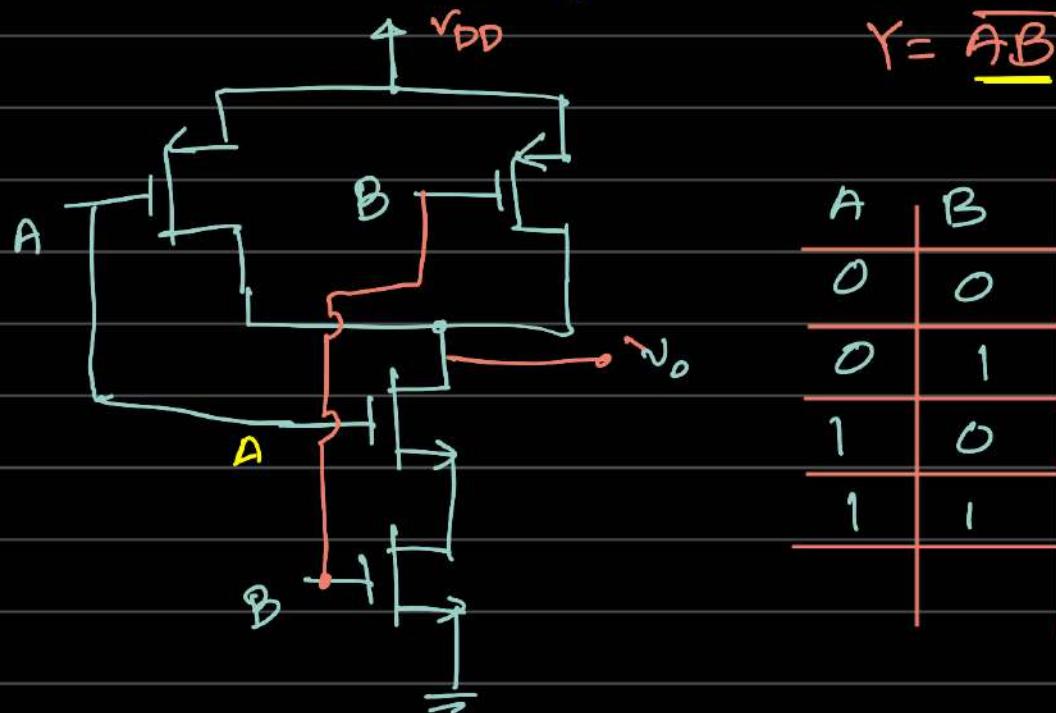


# If gate voltage is logical high, NMOS is ON.  
ON means drain and source are short circuited. PMOS is OFF.

# If gate voltage is logical low, NMOS  $\rightarrow$  OFF, PMOS  $\rightarrow$  ON.

A	B	$v_o$
0	0	$v_{DD}$
0	1	0
1	0	0
1	1	0

# CMOS NAND gate:



A	B	$v_o$
0	0	$v_{DD}$
0	1	$v_{DD}$
1	0	$v_{DD}$
1	1	0

# Conduction complement :-

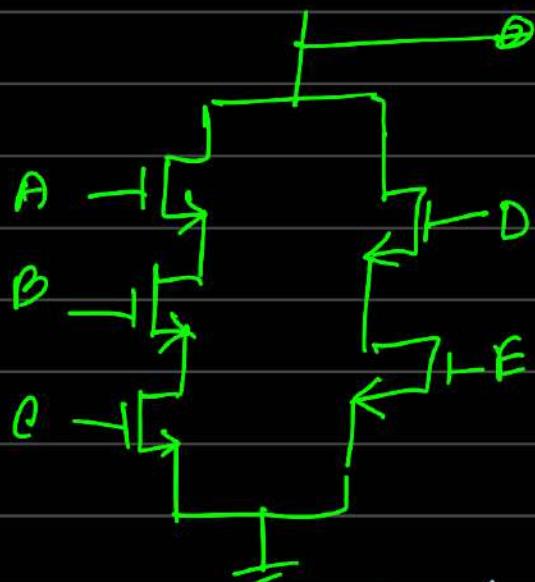
NMOS and PMOS section in CMOS logic gates are conduction complement. That is series connections are parallel in another part and vice versa.

# Pull-up network: makes output voltage high  
 # Pull-down network: makes output voltage low.  
 PMOS network  
 NMOS network.

#  $Y = \overline{ABC + DE}$

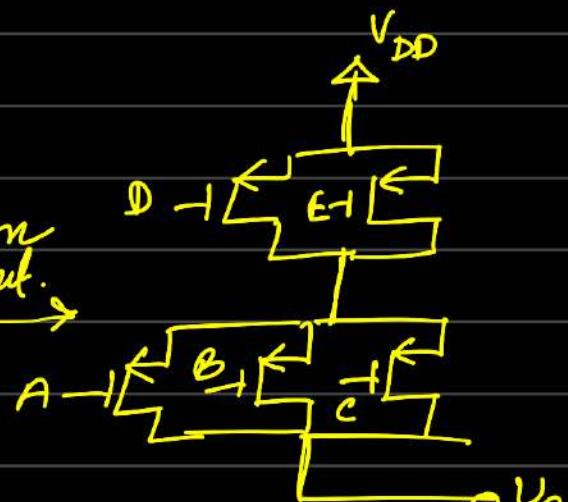
\* first we design the NMOS part.

# If inside the whole bar, inputs are in AND/OR  
 then NMOSs are in series/parallel.



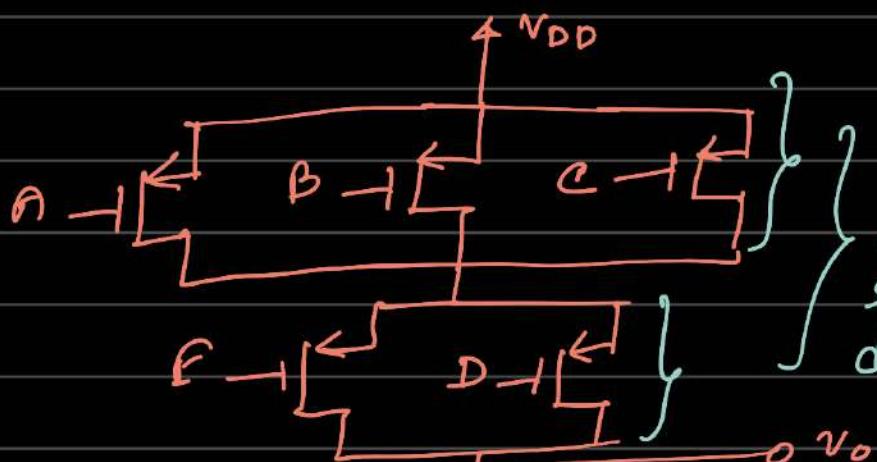
pull-down network.

conduction  
complement.

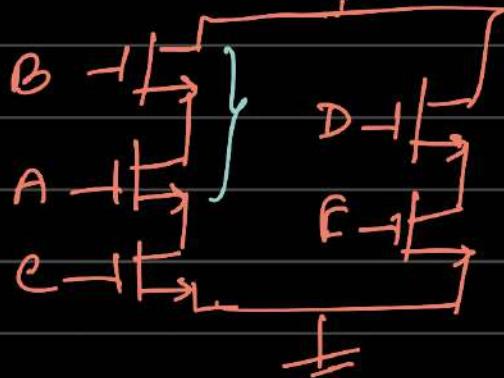


pull-up network.

Combined result.



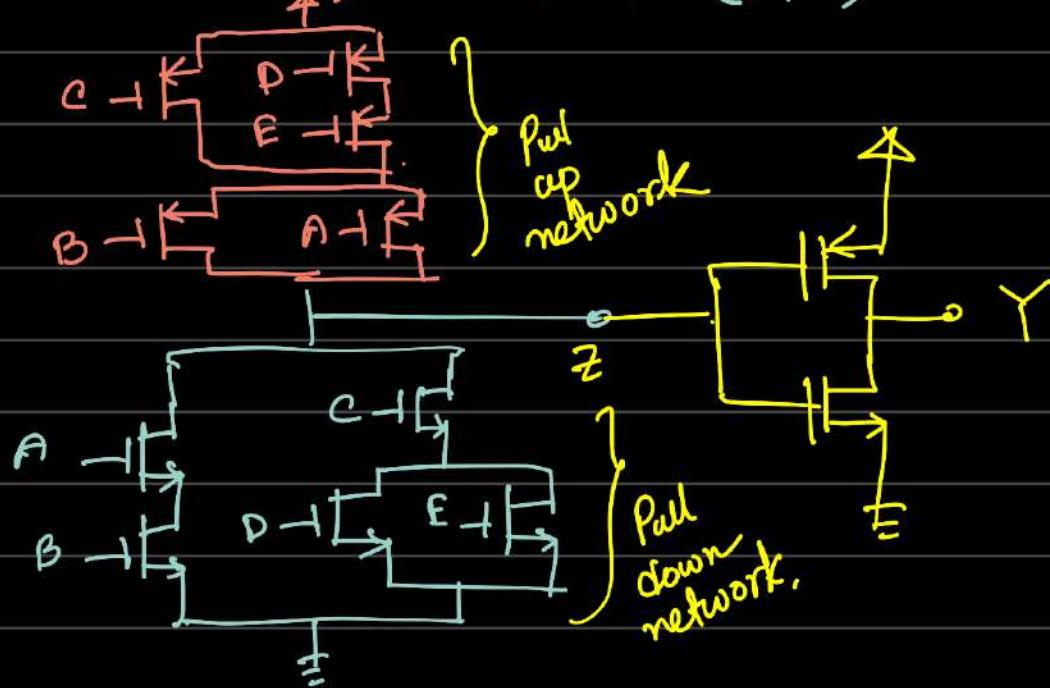
Shuffling two  
series component  
doesn't change  
result.



## Design example 16.11

$$Y = AB + C(D+E)$$

First we solve,  $Z = \overline{AB + C(D+E)}$

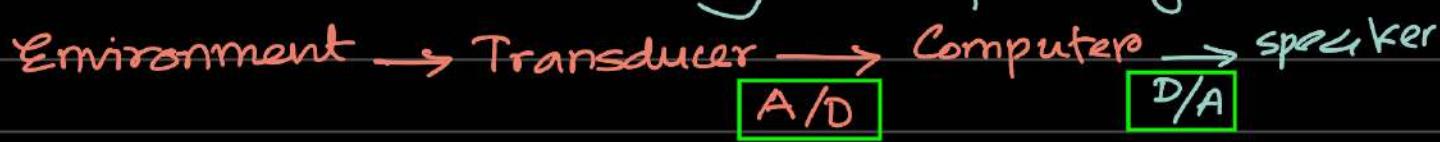


# April 16, Quiz 4. NMOS inverter with depletion load circuit.

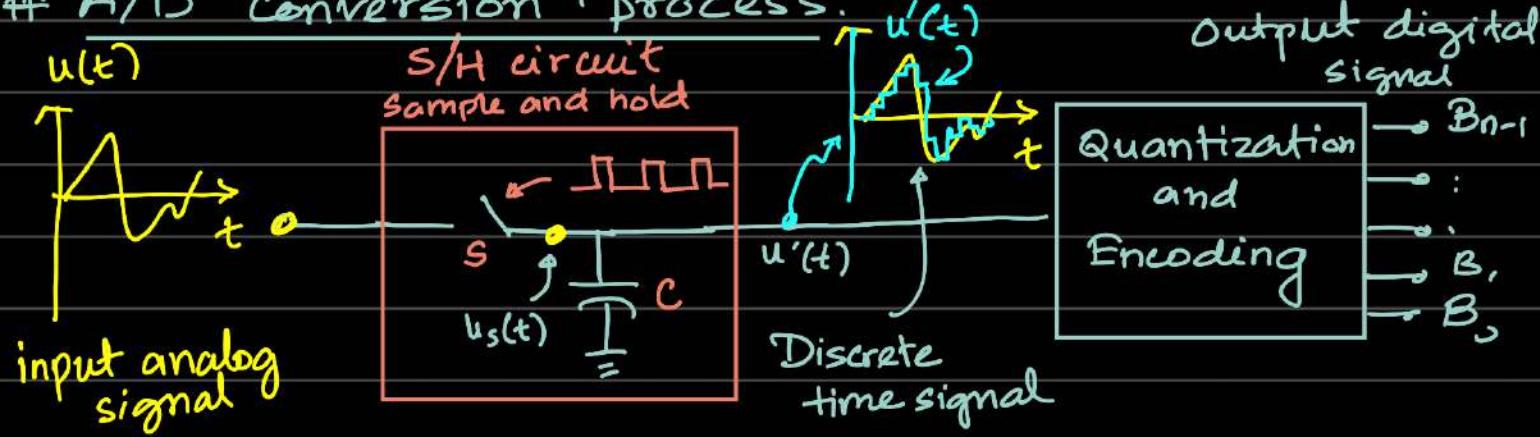
## Lecture 16: ADC and DAC

# Physical world's informations are analog. Analog means data could take any real value at each instant of time.

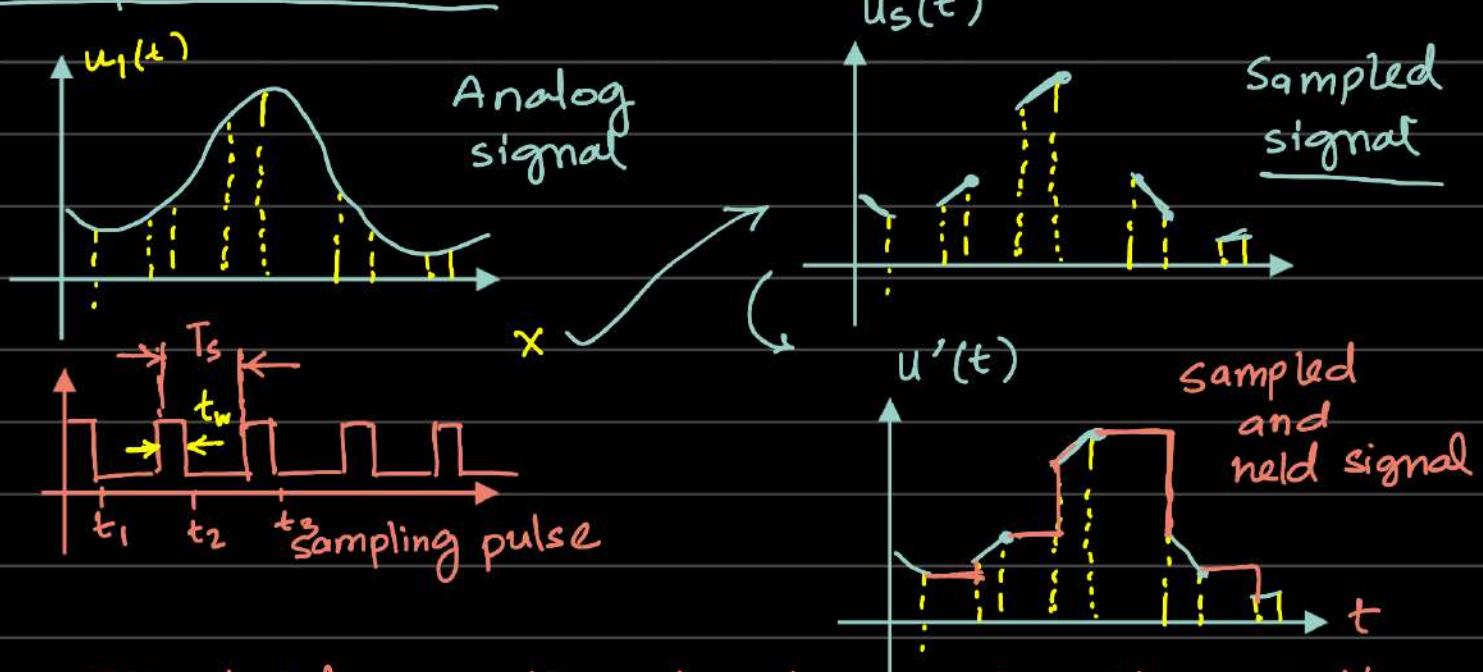
# In order to store/process we use digital data in our computers and microprocessor. Digital data means binary bit of strings.



## A/D Conversion process



## Sample and Hold:

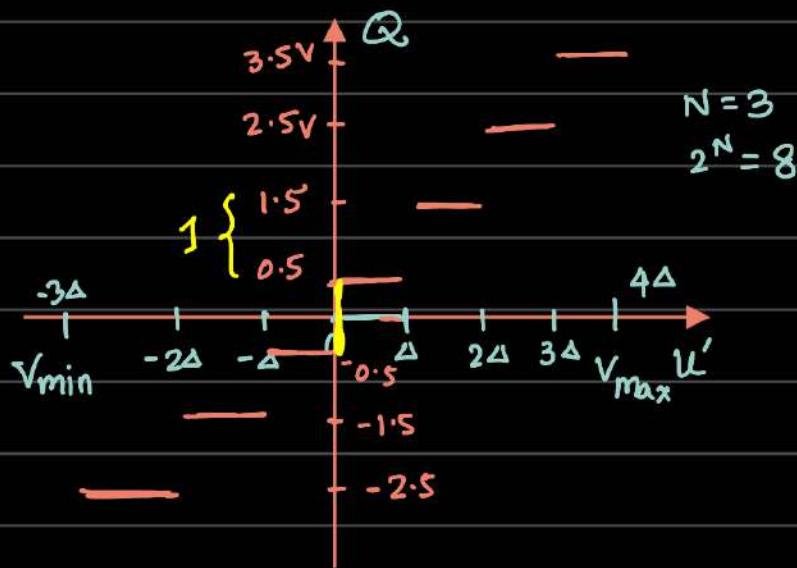


This hold operation is done using the capacitors.

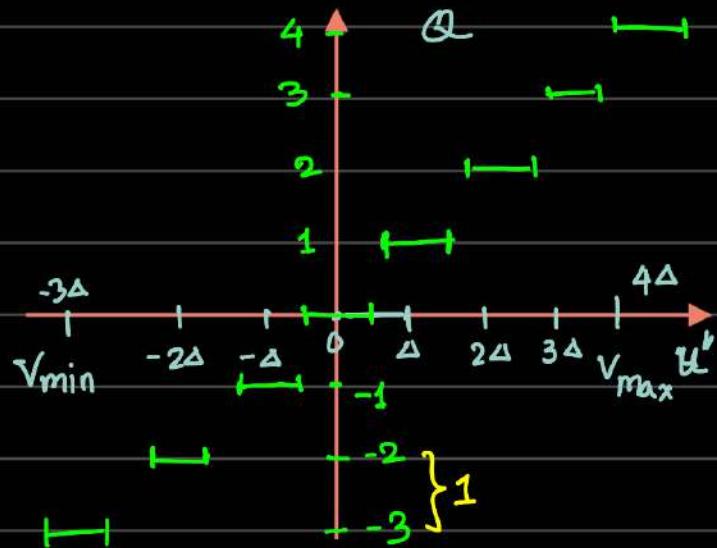
## Quantization:

Quantization is process by which we assign sampled and hold signal data to some fixed preassigned values.

### Midrise quantization



### Mid thread quantization



$N$  = number of bits we want as digital output

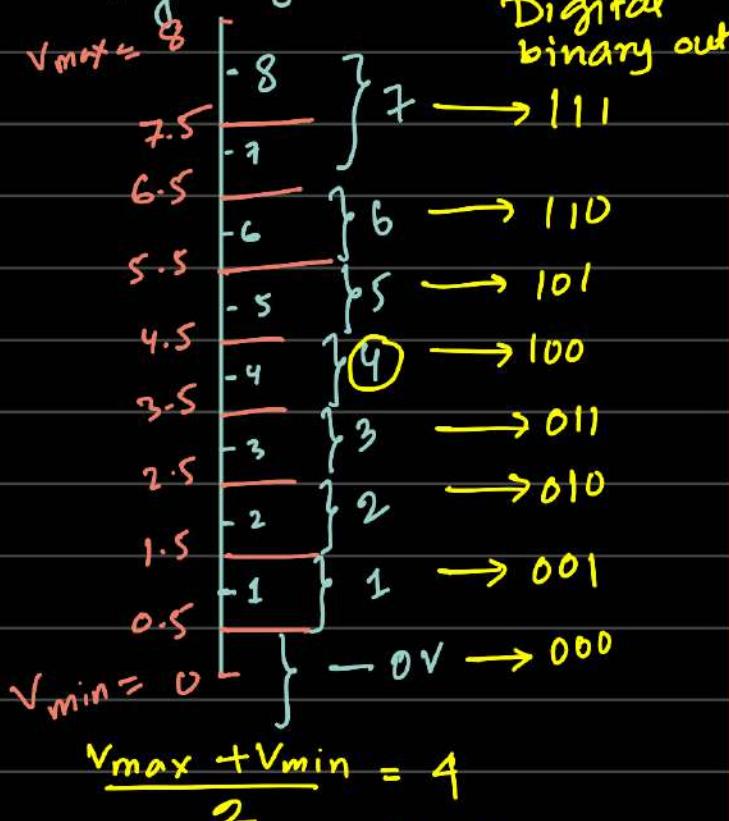
$$\Delta = \text{resolution} = \frac{V_{\max} - V_{\min}}{2^N}$$

$2^N$  = number of levels.

$V_{\max} / V_{\min}$  = maximum/minimum possible value of analog signal.

# Encoding: We can choose binary values for each quantized levels.

Analog signal.



Digital binary output

Midrise quantization

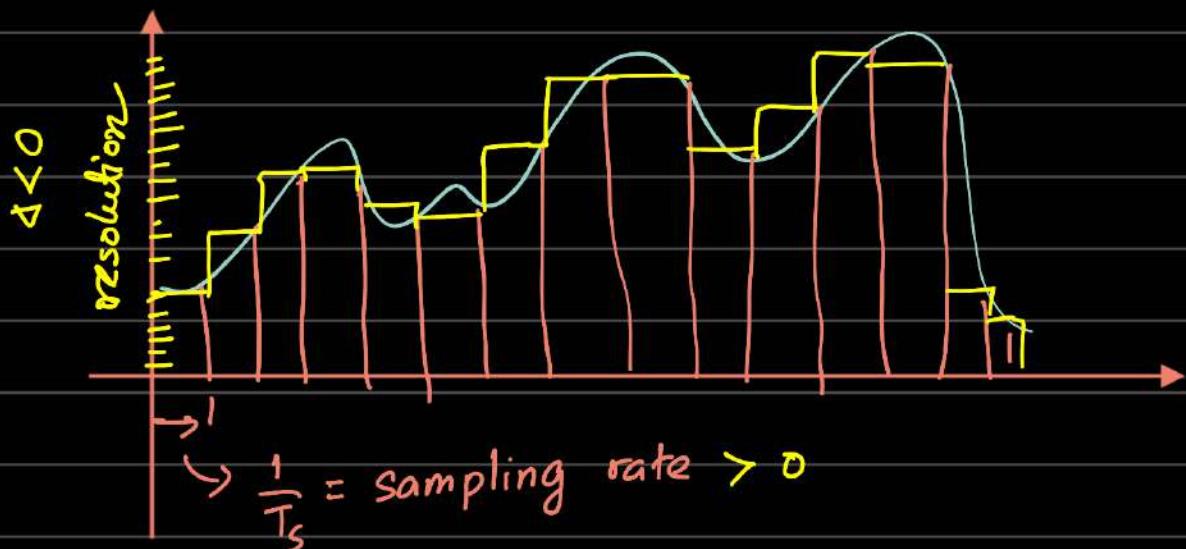
$$V_{max} = 10V, V_{min} = 0V$$

000	$0 - 1.25V$	$0.675$
001	$1.25 - 2.5$	$1.875$
010	$2.5 - 3.75$	$3.125$
011	$3.75 - 5.0$	$4.375$
100	$5.0 - 6.25$	$5.625$
101	$6.25 - 7.5$	$6.875$
110	$7.5 - 8.75$	$8.125$
111	$8.75 - 10.0$	$9.375$

$$\frac{V_{min} + V_{max}}{2} = 5V$$

voltage levels

1 v is a quantization level so it is actually midtread quantization.



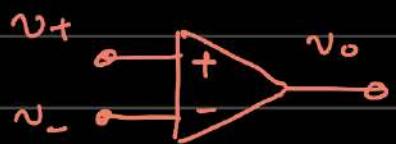
# Flash A/D Converter:

Ad. # This converter is very fast. It requires one clock cycle to convert the analog to digital data.

Dis. # It requires a lot component.

$$N = 3, 2^N = 8$$

### Midrise quantization:



$v_+ > v_-$ ,  $v_o = \text{High}$

$v_+ < v_-$ ,  $v_o = \text{Low}$

$$v^+_{ref} = 9.375 \text{ V}$$

$$v^-_{ref} = -0.675 \text{ V}$$

$$I = \frac{v^+_{ref} - v^-_{ref}}{8R} = \frac{10}{8R}$$

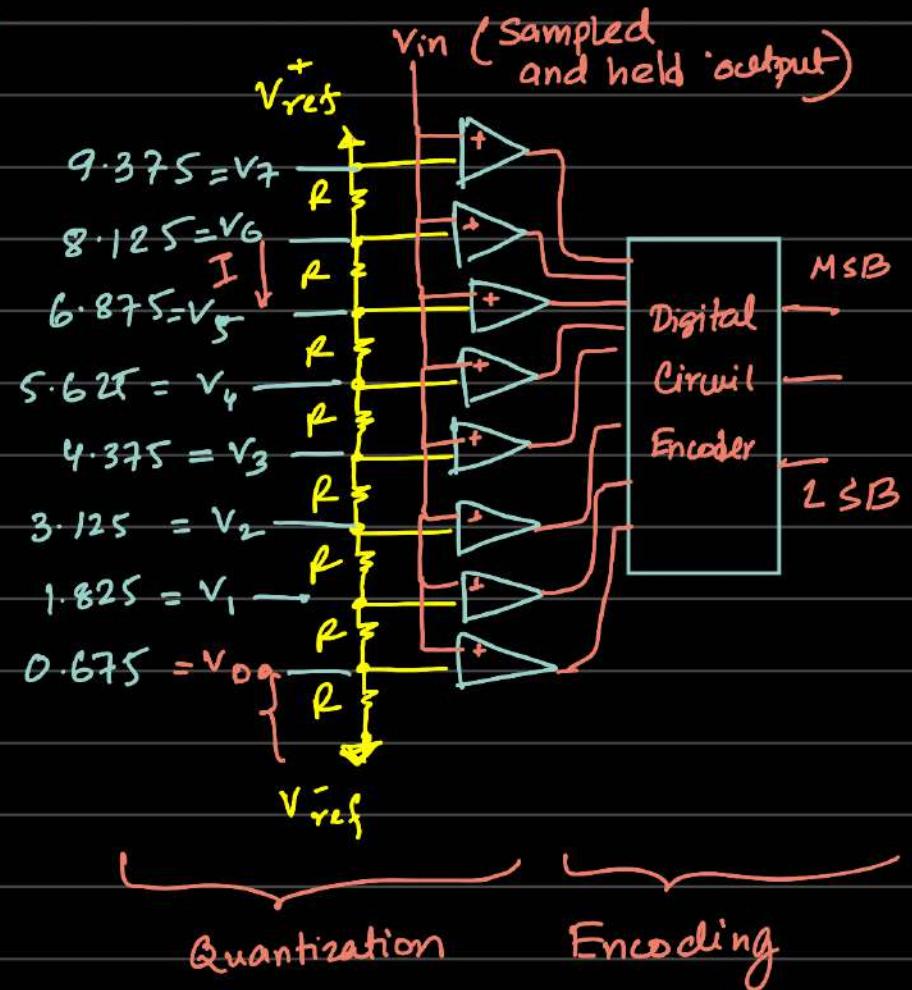
$$IR = v_o - v^-_{ref}$$

$$\Rightarrow v_o = v^-_{ref} + IR$$

$$= -0.675 + \frac{10}{8}$$

$$= 0.675$$

$$v_1 = v_o + IR = 1.825$$

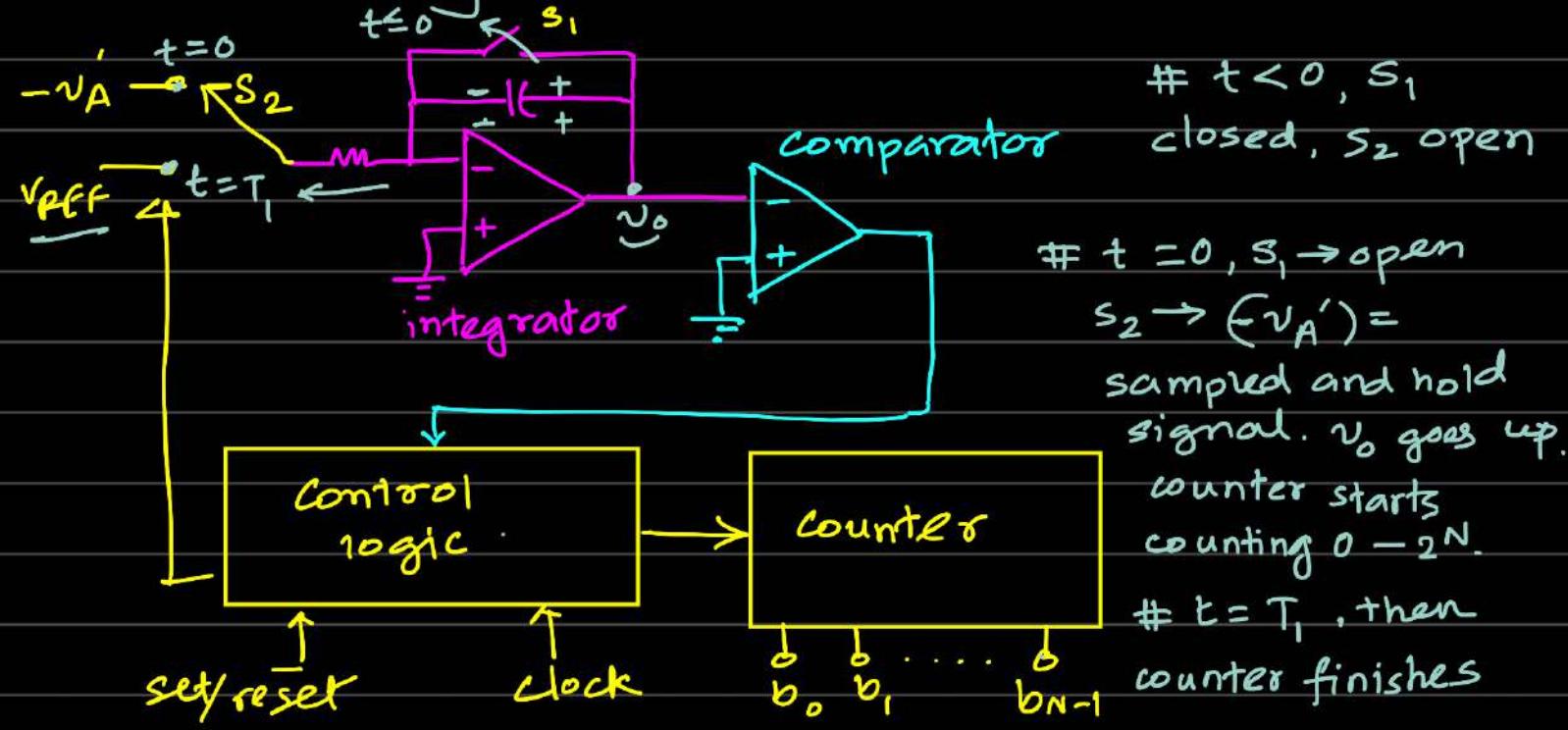


### Lecture 17: A/D and D/A

#### Dual slope A/D converters:

Adv.: Needs less circuit component

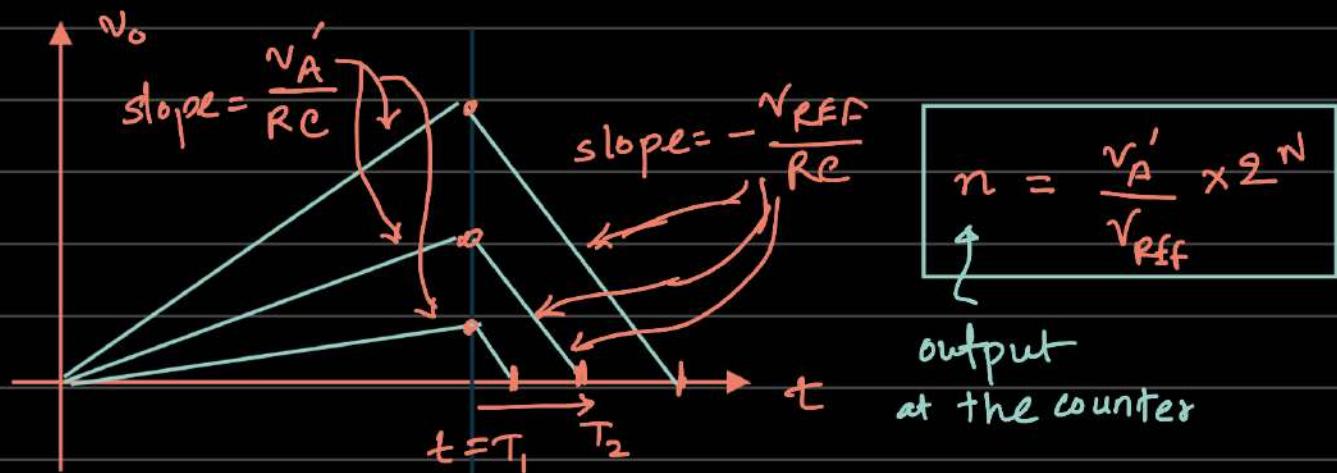
Dis: Very slow converter.



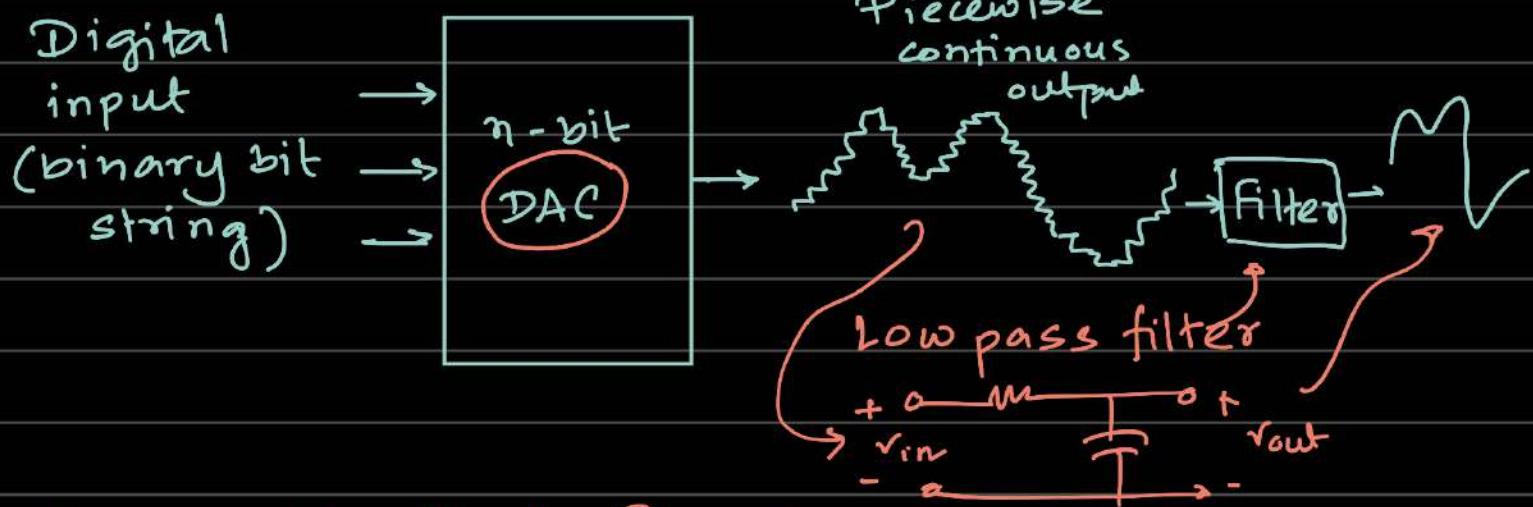
Counting to  $2^N$ .  $s_2 \rightarrow v_{ref}$ .  $v_o$  starts to decline. Counter again started counting.

#  $t = T_2$ ,  $v_o$  goes to negative value, then comparator gives HIGH output to control logic circuit and it freezes the counter value.

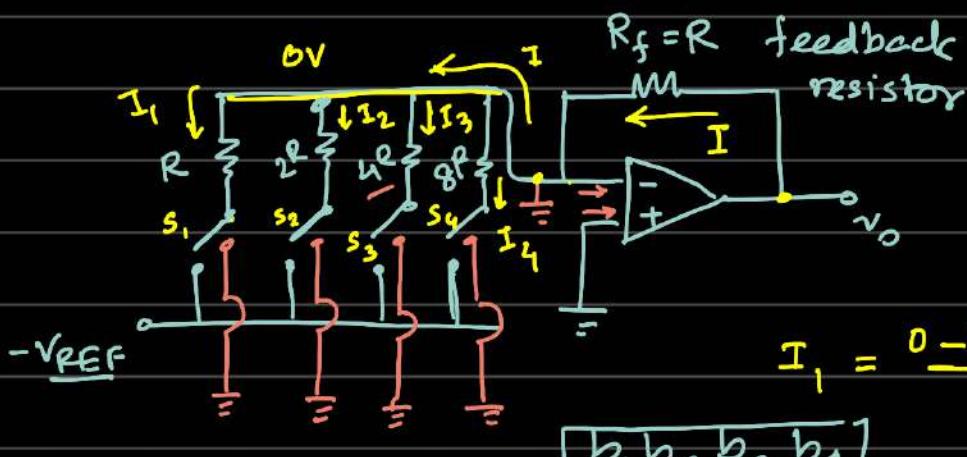
# From that moment the output of counter is the digital output/signal for analog input.



### Digital to Analog conversion:



### Binary Weighted Resistor



Virtual ground is assumed here.

$$I = \frac{v_o - 0}{R} = \frac{v_o}{R}$$

$$I = I_1 + I_2 + I_3 + I_4 \quad (\text{KCL})$$

$$I_1 = \frac{0 - (-v_{ref})}{R} \text{ or } \frac{0}{R}$$

$$[b_1 b_2 b_3 b_4]$$

If  $b_1 = 1$ , then switch  $S_1$  is connected to  $(-V_{REF})$   
 or if  $b_1 = 0$  " " "  $S_1$  " " " " "  $0$  ".

Same goes for  $b_2, b_3, b_4$ .

Then.  $I_1 = \frac{V_{REF}}{R}$  if  $b_1 = 1$  or  $I_1 = 0$  if  $b_1 = 0$

This implies that,

$$I_1 = b_1 \frac{V_{REF}}{R}$$

Similarly for.  $I_2 = \frac{0 - (-V_{REF})}{2R}$  if  $b_2 = 1$  or,  $I_2 = 0$  if  $b_2 = 0$ .

Therefore,

$$I_2 = b_2 \frac{V_{REF}}{2R}$$

In similar fashion we will get,

$$I_3 = \frac{b_3 V_{REF}}{4R}, \quad I_4 = \frac{b_4 V_{REF}}{8R}$$

finally,  $I = I_1 + I_2 + I_3 + I_4$

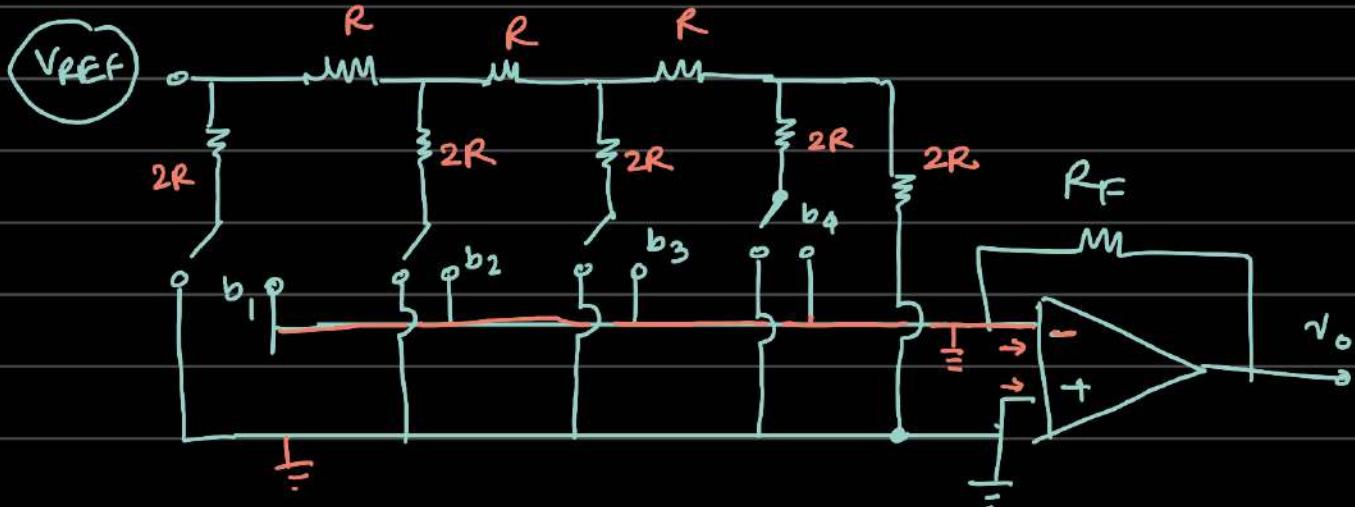
$$\Rightarrow \frac{V_o}{R} = b_1 \frac{V_{REF}}{R} + b_2 \frac{V_{REF}}{2R} + b_3 \frac{V_{REF}}{4R} + b_4 \frac{V_{REF}}{8R}$$

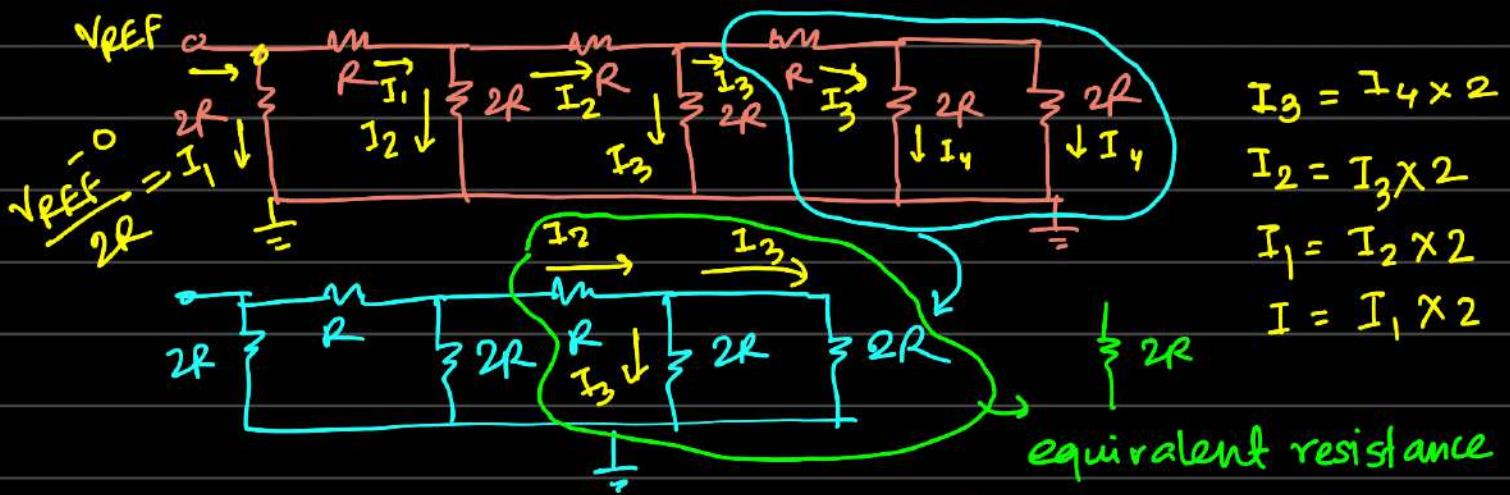
$$\Rightarrow V_o = V_{REF} \left( b_1 + \frac{b_2}{2} + \frac{b_3}{4} + \frac{b_4}{8} \right)$$

$$(1010) \rightarrow \nu_0 = 16 \left( 1 + \frac{0}{2} + \frac{1}{4} + \frac{0}{8} \right) = 16$$

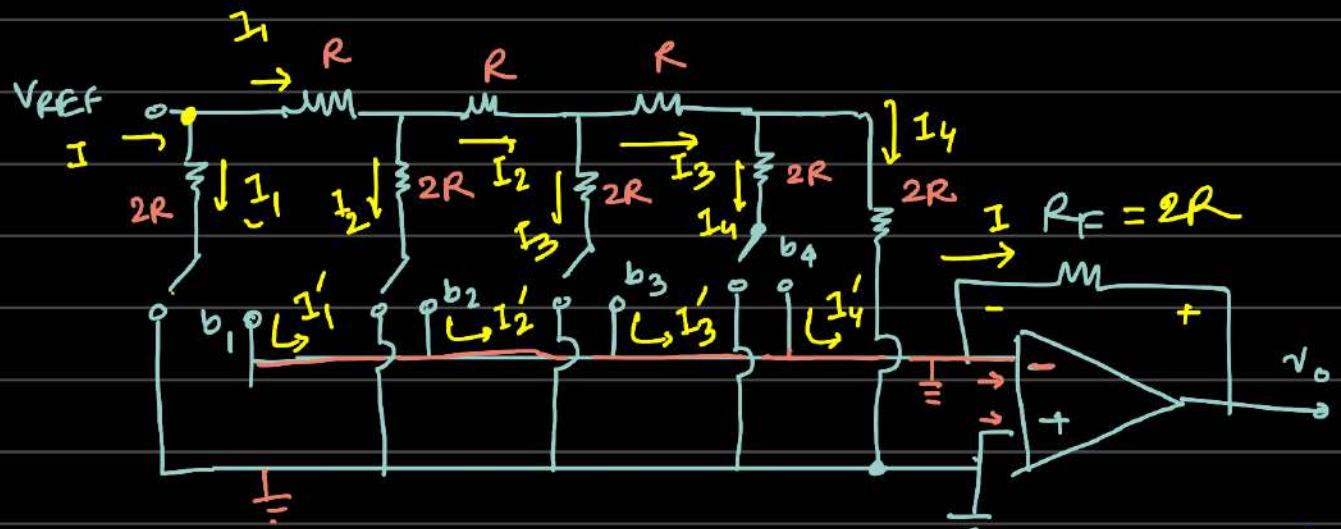
$= 20 \text{ V}$  Dis: output is very sensitive  
if the resistor values fluctuate  
a little.

## R-2R Ladder





$$\Rightarrow I_1 = \frac{I}{2}, I_2 = \frac{I_1}{2} = \frac{I}{4}, I_3 = \frac{I_2}{2} = \frac{I}{8}, I_4 = \frac{I_3}{2} = \frac{I}{16}$$



$$I = \frac{(0 - V_o)}{R_F} = -\frac{V_o}{R_F}, \quad I'_1 = b_1 I_1 \quad \text{if } b_1 = 0, I'_1 = 0 \\ \text{if } b_1 = 1, I'_1 = I_1$$

$$I'_2 = b_2 I_2, \quad I'_3 = b_3 I_3, \quad I'_4 = b_4 I_4$$

$$I = I'_1 + I'_2 + I'_3 + I'_4 \quad [\text{KCL}]$$

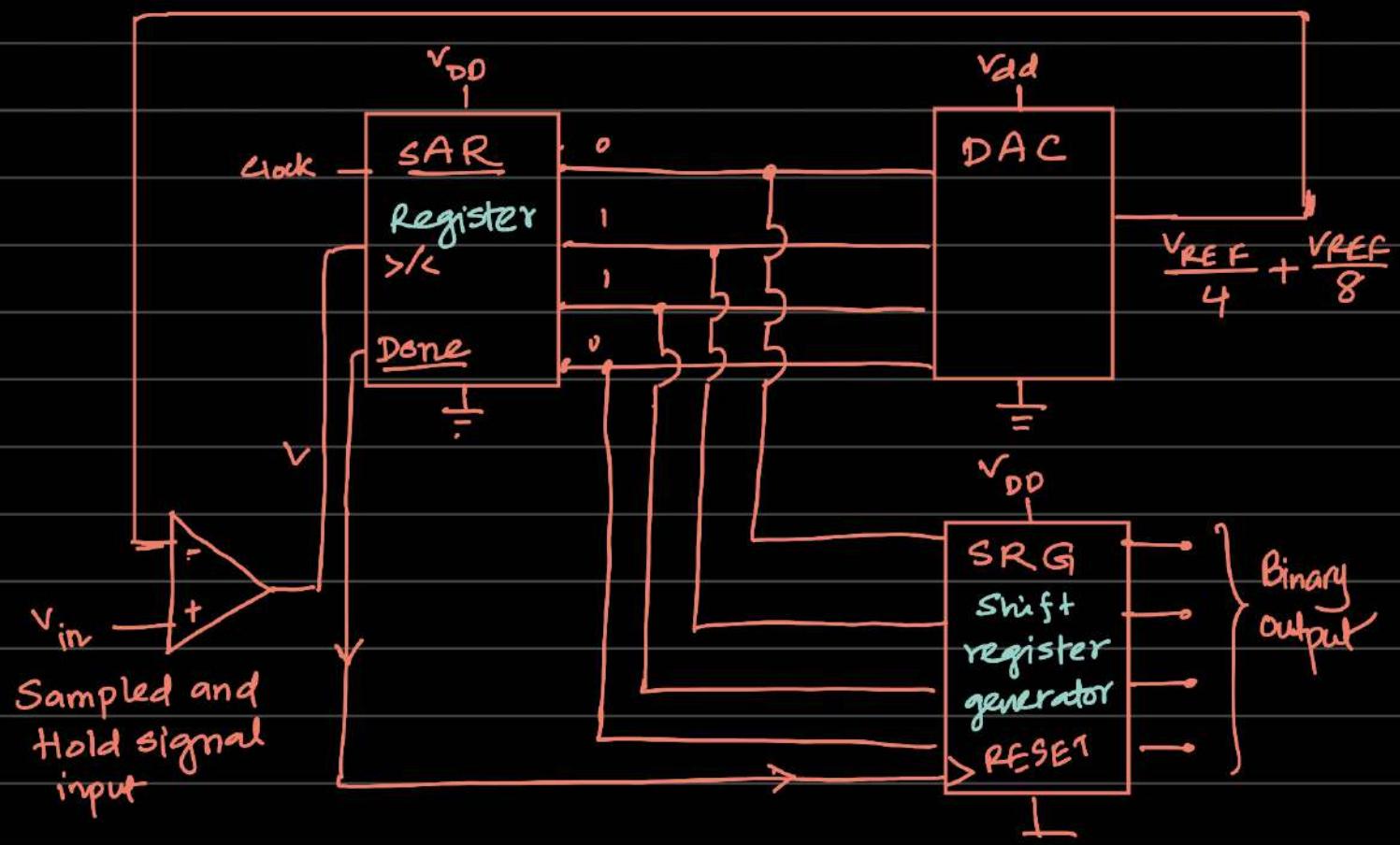
$$= b_1 I_1 + b_2 I_2 + b_3 I_3 + b_4 I_4$$

$$-\frac{V_o}{R_F} = b_1 \frac{V_{REF}}{2R} + b_2 \frac{V_{REF}}{4R} + b_3 \frac{V_{REF}}{8R} + b_4 \frac{V_{REF}}{16R}$$

$$\Rightarrow V_o = \left( -V_{REF} \right) \left( b_1 + \frac{b_2}{2} + \frac{b_3}{4} + \frac{b_4}{8} \right) \quad \boxed{2R = R_F}$$

## # Successive Approximation ADC

# Binary search : Adv : Takes moderate time and uses less components.

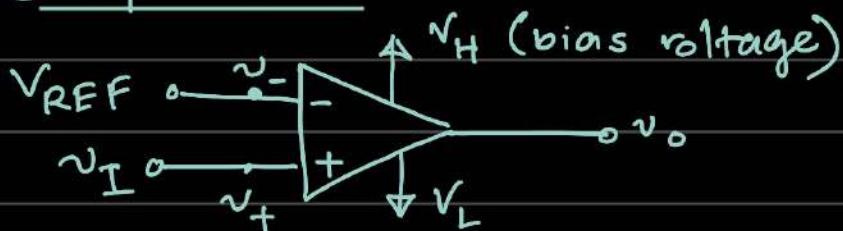


BUX video "lecture 14" → practice

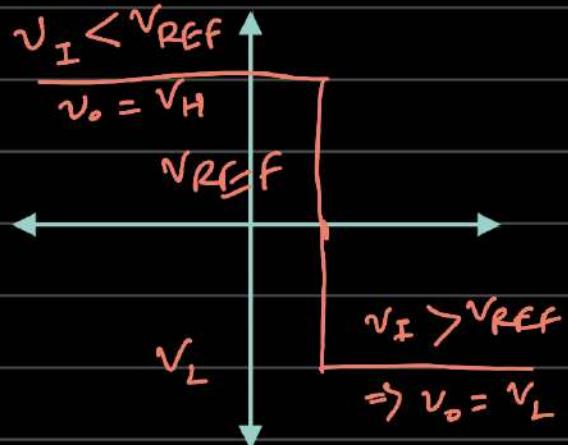
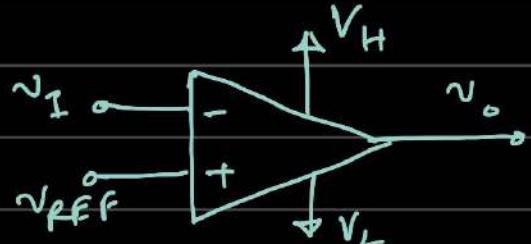
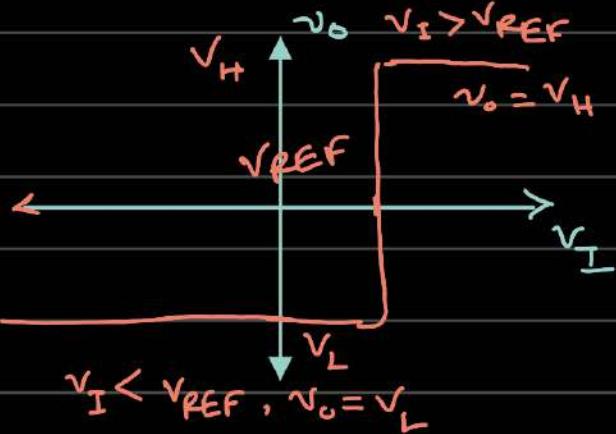
## Lecture 18: Schmitt Trigger

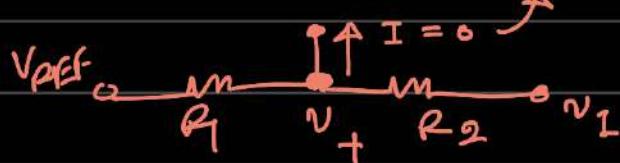
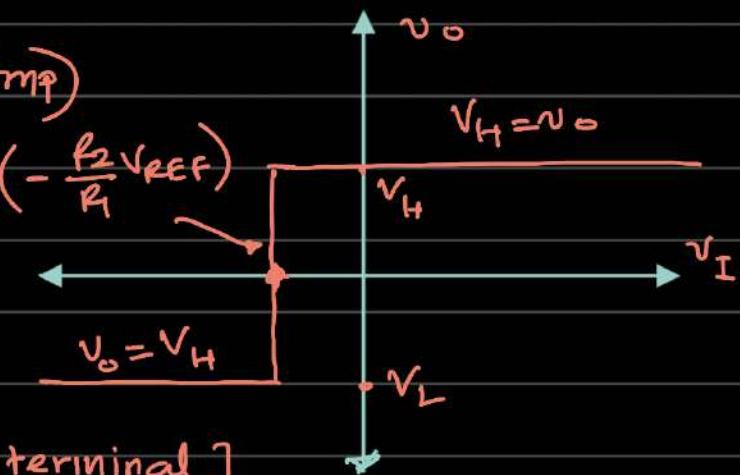
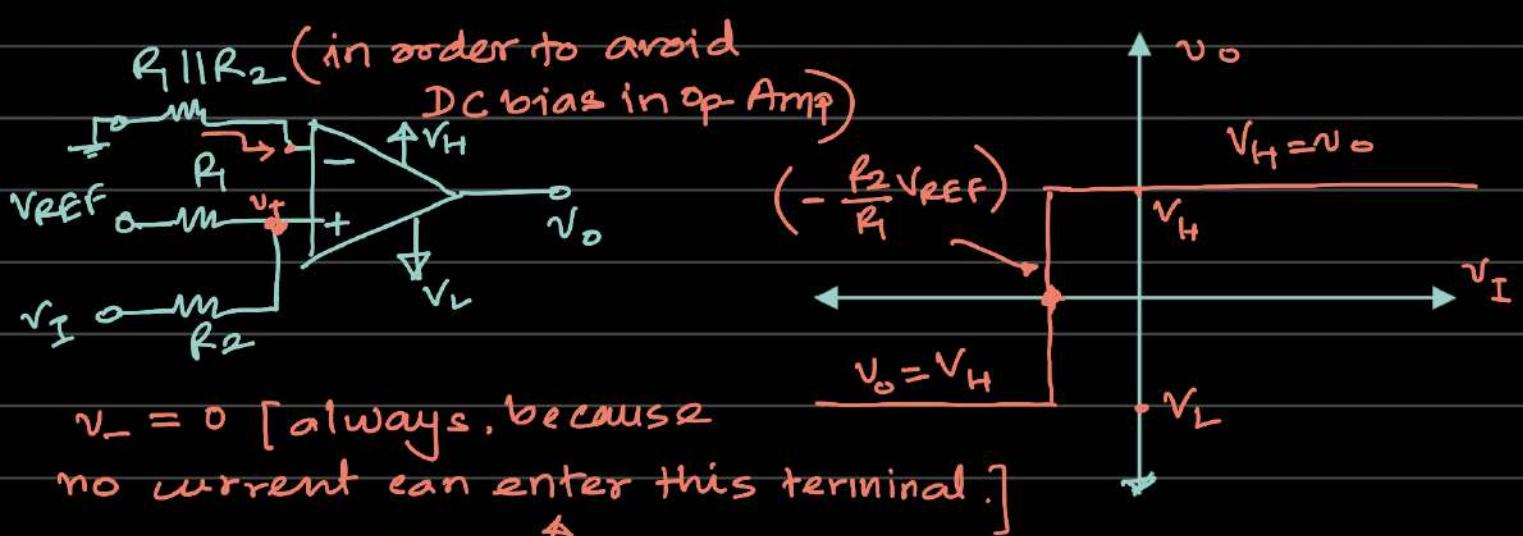
Otto H. Schmitt (1934) proposed this design.

Comparators:



$$\begin{aligned} v_+ > v_- &\Rightarrow v_o = v_H \\ v_+ < v_- &\Rightarrow v_o = v_L \end{aligned}$$





$$\frac{V_+ - V_{REF}}{R_1} + \frac{V_+ - V_I}{R_2} = 0 \quad [\text{Nodal equation at + terminal}]$$

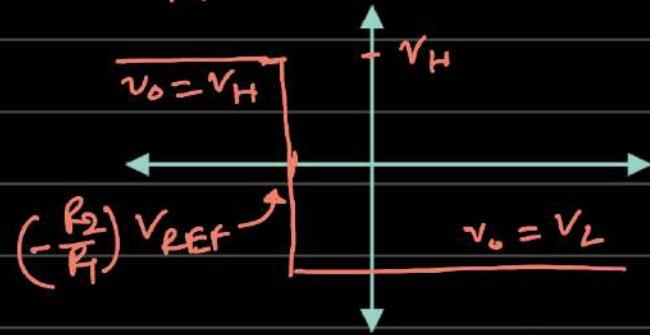
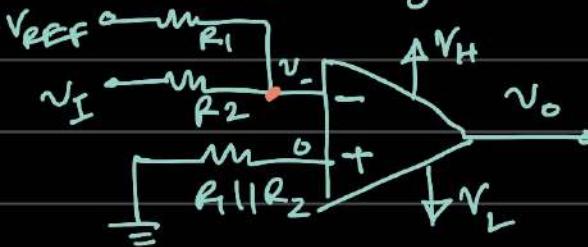
$$\Rightarrow V_+ = V_I \left( \frac{R_1}{R_1 + R_2} \right) + V_{REF} \left( \frac{R_2}{R_1 + R_2} \right)$$

$$\text{if } V_+ > V_- = 0 \Rightarrow V_I \left( \frac{R_1}{R_1 + R_2} \right) > V_{REF} \left( -\frac{R_2}{R_1 + R_2} \right) \Rightarrow V_I > \left( -\frac{R_2}{R_1} \right) V_{REF}$$

$$\Rightarrow V_0 = V_H$$

$$\text{or } V_+ < V_- = 0 \Rightarrow V_I < \left( -\frac{R_2}{R_1} \right) V_{REF} \text{ then } V_0 = V_L.$$

Another design:



$$\text{if } V_+ = 0 > V_- = V_I \left( \frac{R_1}{R_1 + R_2} \right) + V_{REF} \left( \frac{R_2}{R_1 + R_2} \right)$$

$$\Rightarrow V_I < \left( -\frac{R_2}{R_1} \right) V_{REF} \Rightarrow V_0 = V_H$$

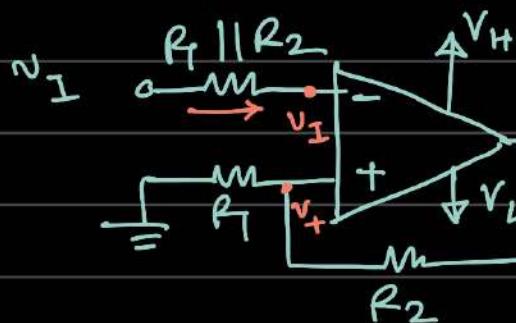
$$\text{again } V_+ < V_- \Rightarrow V_I > \left( -\frac{R_2}{R_1} \right) V_{REF} \Rightarrow V_0 = V_L$$

# These above 2 designs can be used to change transition voltage by tuning  $R_1$  and  $R_2$  resistors.

# These are the building blocks of Schmitt trigger circuit.

## Schmitt trigger circuit:

# Circuit operation largely depends on initial conditions.



# Suppose,  $v_I$  is a negative voltage with a large magnitude.

Since no current is entering through the + or - terminal  $v_- = v_I$ .

The node equation at "+" terminal is:  $\frac{v_+ - 0}{R_1} + \frac{v_+ - v_o}{R_2} = 0$

$$\Rightarrow v_+ = v_o \left( \frac{R_1}{R_2 + R_1} \right)$$

Since  $|v_I| \gg 0$  we can expect  $v_o = v_H$

$$\text{Until } v_I = v_- < v_+ = v_H \left( \frac{R_1}{R_1 + R_2} \right)$$

the  $v_o$  or output remains at  $v_H$

But if  $v_I$  crosses  $v_H \left( \frac{R_1}{R_1 + R_2} \right)$ , then  $v_o$  switches to  $v_L$

This  $v_H \left( \frac{R_1}{R_1 + R_2} \right)$  is called high threshold voltage,  $V_{TH}$ .

Case 2: If  $v_I$  is a very large positive voltage initially.

Now,  $v_- \gg 0$ , so we can expect  $v_- > v_+$  or  $v_o = v_L$

$$\text{therefore } v_+ = v_L \left( \frac{R_1}{R_1 + R_2} \right).$$

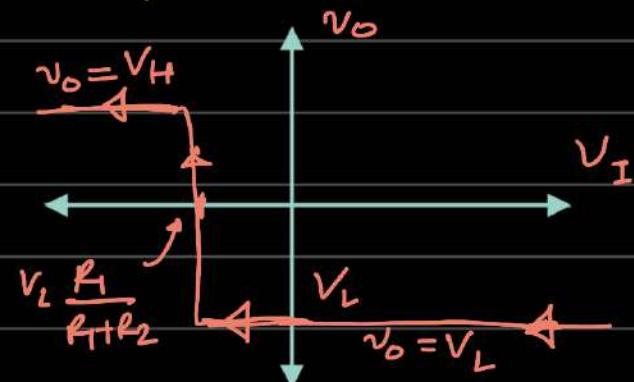
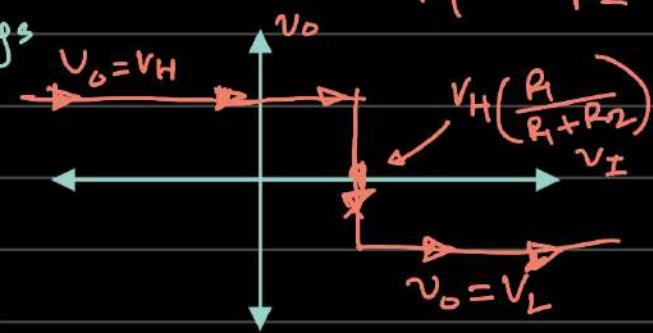
so  $v_o$  remains at  $v_L$  until

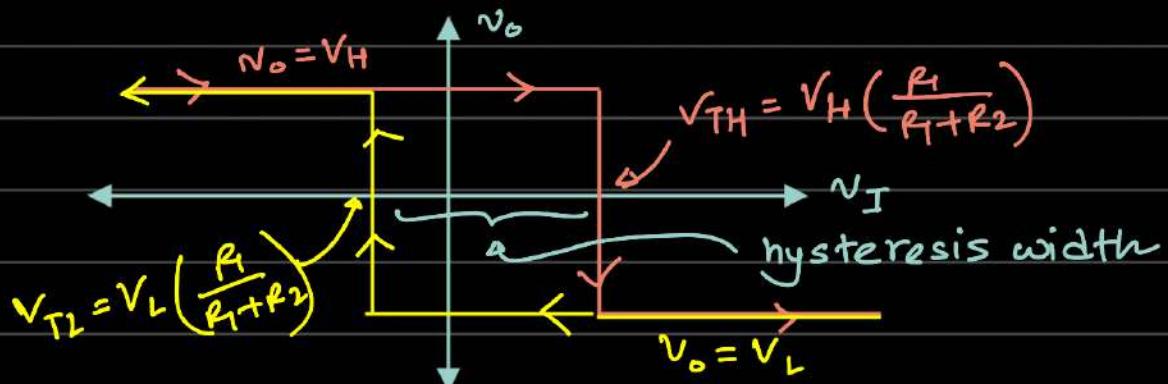
$$v_- > v_+ = v_L \left( \frac{R_1}{R_1 + R_2} \right).$$

But  $v_o$  changes to  $v_H$  when  $v_I > v_L \left( \frac{R_1}{R_1 + R_2} \right)$ .

This  $v_L \left( \frac{R_1}{R_1 + R_2} \right)$  is called low threshold voltage  $V_{TL}$ .

We can combine this two pictures to get the transfer characteristics of Schmitt Trigger.





Total input-output/ transfer characteristics curve.

This circuit is also known as **bistable multivibrators**.

Because output can remain in two (bi) stable states.

Example 15.6 Determine the hysteresis width of a particular Schmitt trigger.

$$R_1 = 10\text{ k}\Omega, R_2 = 90\text{ k}\Omega, V_H = 10V, V_L = -10V.$$

Sol<sup>n</sup>: Hysteresis width =  $V_{TH} - V_{TL}$

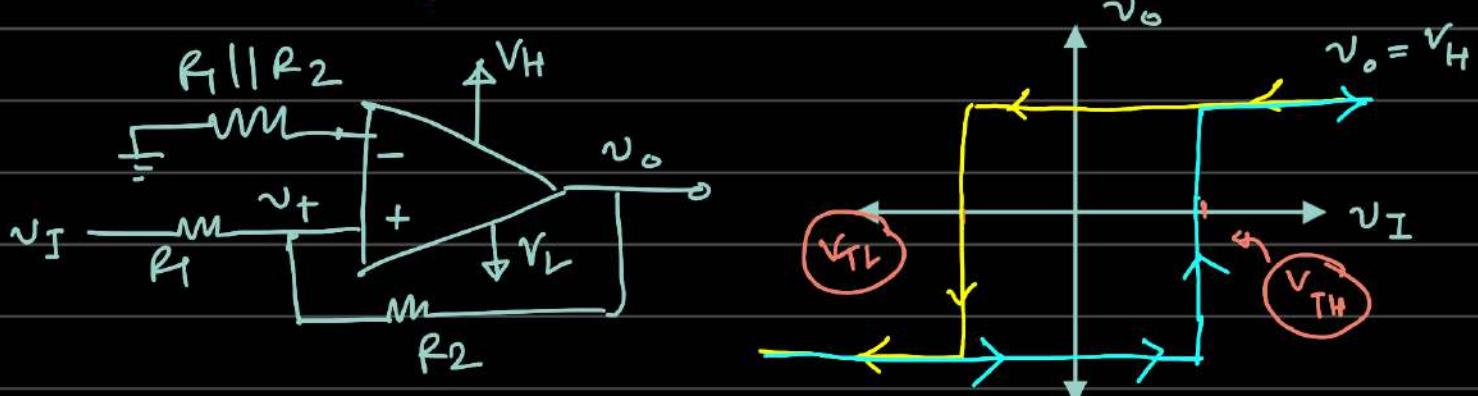
$$= V_H \left( \frac{R_1}{R_1+R_2} \right) - V_L \left( \frac{R_1}{R_1+R_2} \right)$$

$$= (V_H - V_L) \frac{R_1}{R_1+R_2}$$

$$= (10 - (-10)) \times \frac{10}{10+90} = 2V$$

Previous circuit is called inverting Schmitt trigger because when input is very positive/negative output is negative/ positive.

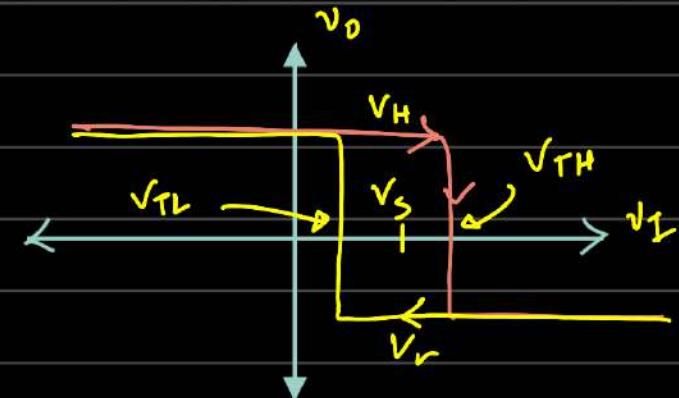
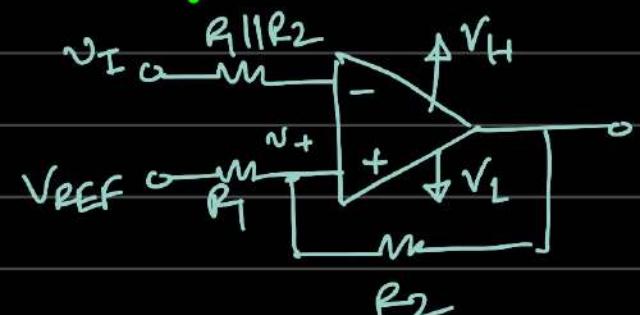
**Non inverting Schmitt trigger circuit.**



$$v_+ = v_I \frac{R_2}{R_1+R_2} + v_o \frac{R_1}{R_1+R_2} \Rightarrow v_+ < 0 \text{ and } v_o = V_H$$

$$v_- = 0 \text{ [Always]} \Rightarrow V_{TH} = V_L \left( -\frac{R_1}{R_2} \right)$$

# Schmitt trigger circuit with applied reference voltage:



Nodal equation at  $V_+$

$$\frac{V_+ - V_{REF}}{R_1} + \frac{V_+ - V_o}{R_2} = 0$$

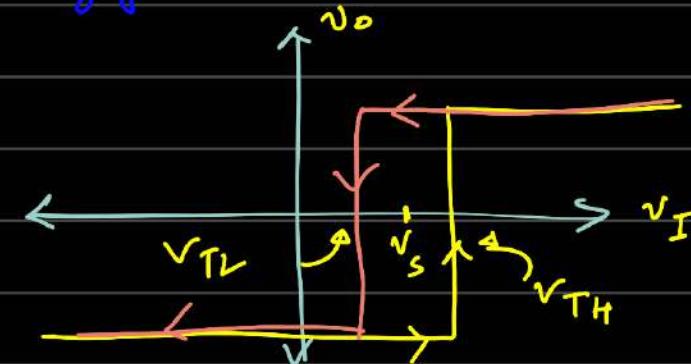
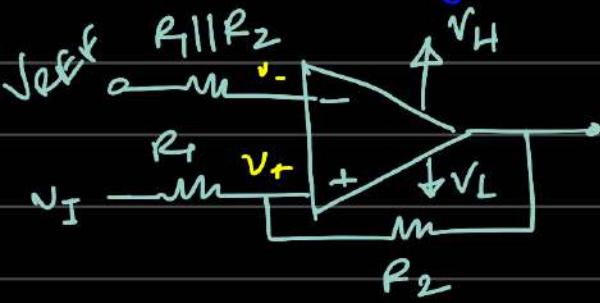
$$\Rightarrow V_+ = V_{REF} \left( \frac{R_2}{R_1 + R_2} \right) + V_o \times \frac{R_1}{R_1 + R_2}$$

$$V_{TH} = V_{REF} \left( \frac{R_2}{R_1 + R_2} \right) + V_H \left( \frac{R_1}{R_1 + R_2} \right)$$

$$V_{TL} = V_{REF} \left( \frac{R_2}{R_1 + R_2} \right) + V_L \left( \frac{R_1}{R_1 + R_2} \right)$$

Shifted voltage.  $V_S = V_{REF} \frac{R_2}{R_1 + R_2}$

Non-inverting Schmitt trigger.



$$V_+ = V_I \times \frac{R_1}{R_1 + R_2} + V_o \times \frac{R_1}{R_1 + R_2}$$

$$V_- = V_{REF}$$

Do1:  $V_{TH} = V_{REF} \left( \frac{R_1 + R_2}{R_2} \right) + \left( -\frac{R_1}{R_2} \right) V_L$

$$V_{TL} = V_{REF} \left( \frac{R_1 + R_2}{R_2} \right) + \left( -\frac{R_1}{R_2} \right) V_H$$

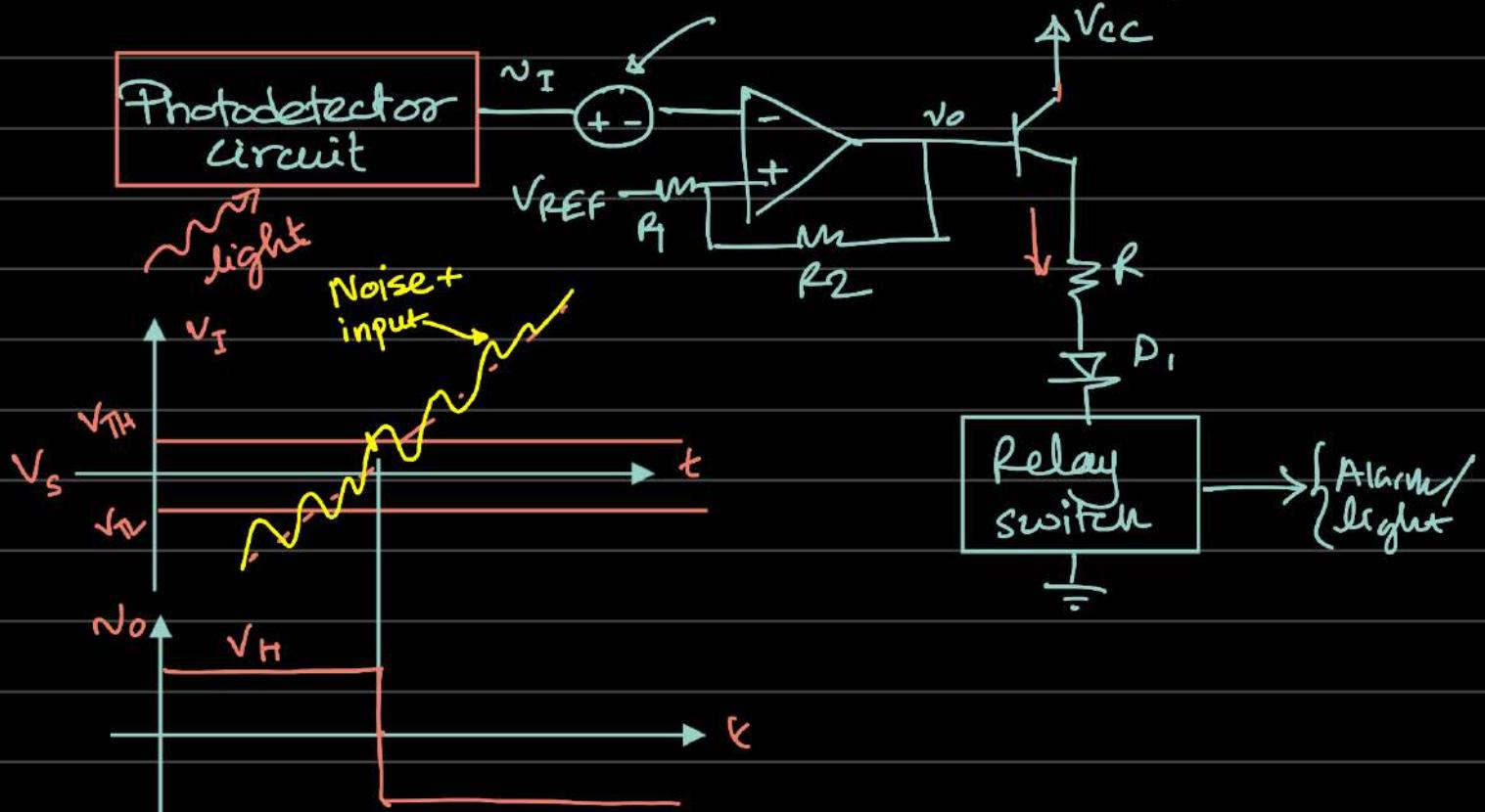
$\xleftarrow{VS}$

# Application:

□ Smoke detector

□ Street light control.

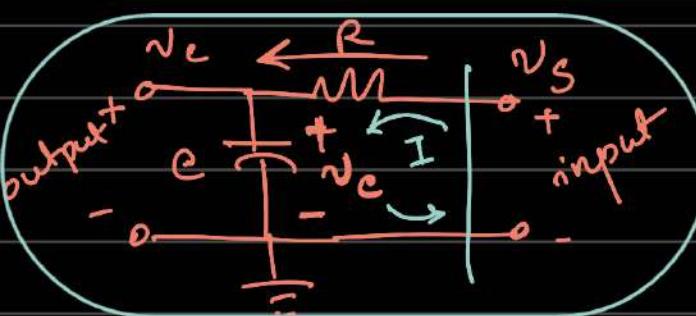
## Noise source: Chattering effect



## Design problem 15.7 (Practice | Final Exam)

### Lecture 19: Signal Generators.

#### Basic RC circuit Review:



We want to find the voltage of capacitor as a function of time. Assuming  $V_s$  = source voltage is constant.

Assuming an initial condition.  $V_c(t=t_1) = V_{initial}$

$V_c < V_s$ , ( $Q$  = charge in capacitor)  $\Delta \uparrow$

$V_c > V_s$ .  $Q \downarrow$ .

We know from the definition of current  $I = \frac{dQ}{dt}$

definition of capacitance gives us  $Q = CV_c$

$$\therefore I = \frac{dQ}{dt} = \frac{d}{dt}(CV) = C \frac{dV_c}{dt} = \frac{V_s - V_c}{R}$$

$$\Rightarrow \int \frac{dV_c}{V_s - V_c} = \frac{1}{RC} \int_{t_1}^{t_2} dt \Rightarrow -\ln|V_s - V_c| \Big|_{V_c(t_1)}^{V_c(t_2)} = \frac{1}{RC} (t_2 - t_1)$$

$RC = \tau$  = time constant of the circuit.

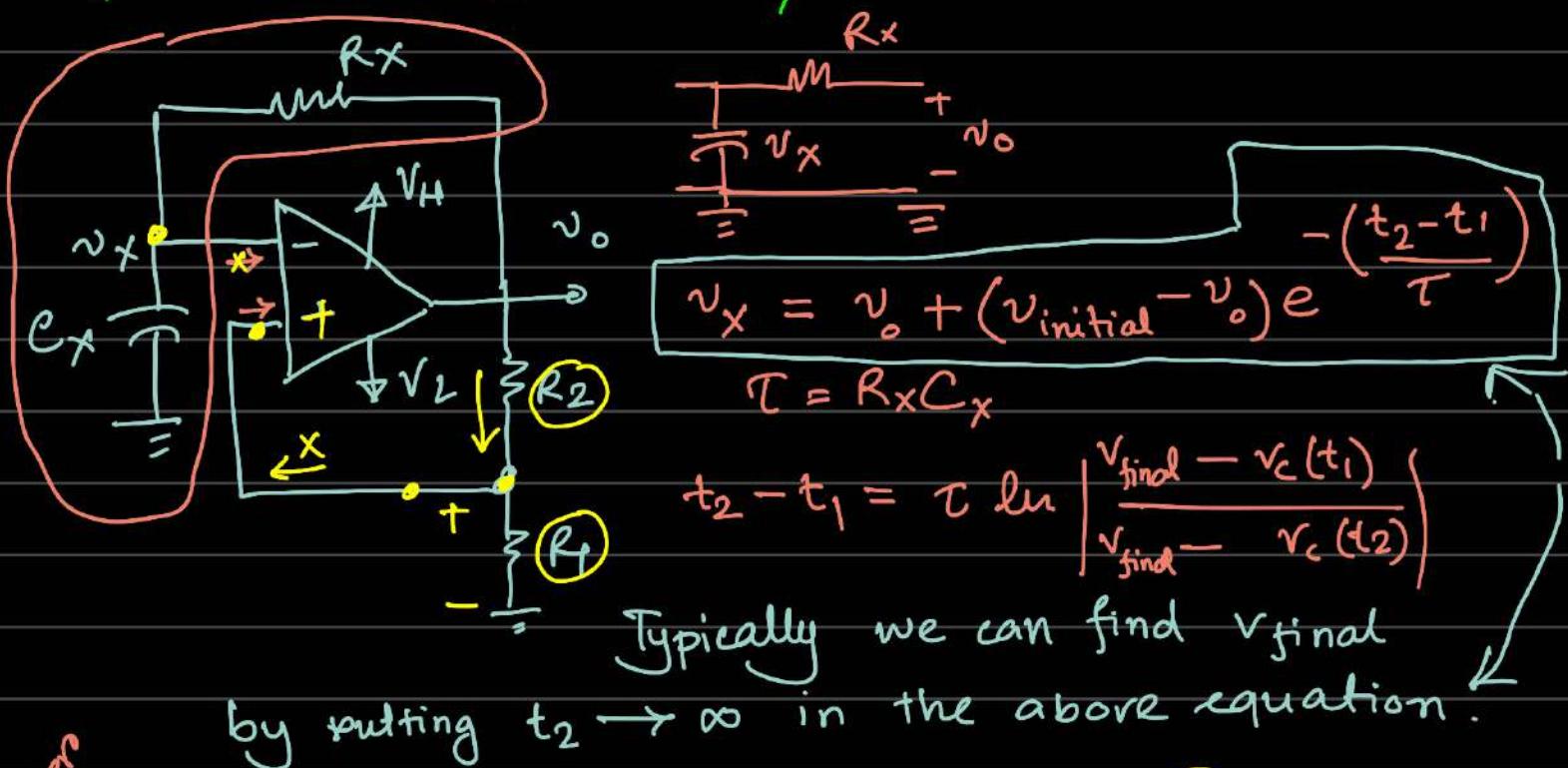
$$\Rightarrow \ln \left| \frac{V_s - V_c(t_1)}{V_s - V_c(t_2)} \right| = \frac{1}{\tau} (t_2 - t_1) \leftarrow$$

$$\Rightarrow V_c(t_2) = V_s + (V_c(t_1) - V_s) \exp\left(-\frac{t_2 - t_1}{\tau}\right)$$

$$\underline{t_2 \rightarrow \infty}, \underline{V_c(\text{final}) = V_s}, \underline{V_c(t_1) = V_{\text{initial}}}$$

$$V_c(t_2) = V_{\text{final}} + (V_{\text{initial}} - V_{\text{final}}) \exp\left(-\frac{t_2 - t_1}{\tau}\right)$$

**Square Wave Generator / Astable Multivibrator**



*Ref* Higher threshold voltage.  $V_{TH} = V_H \frac{R_1}{R_1 + R_2}$

Lower threshold voltage.  $V_{TL} = V_L \frac{R_1}{R_1 + R_2}$

# Coughlin - ch-6

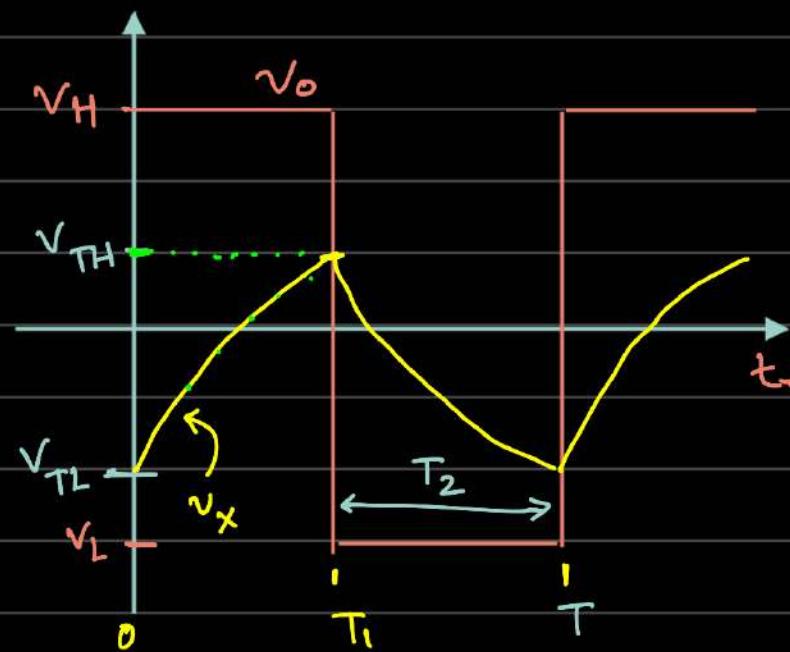
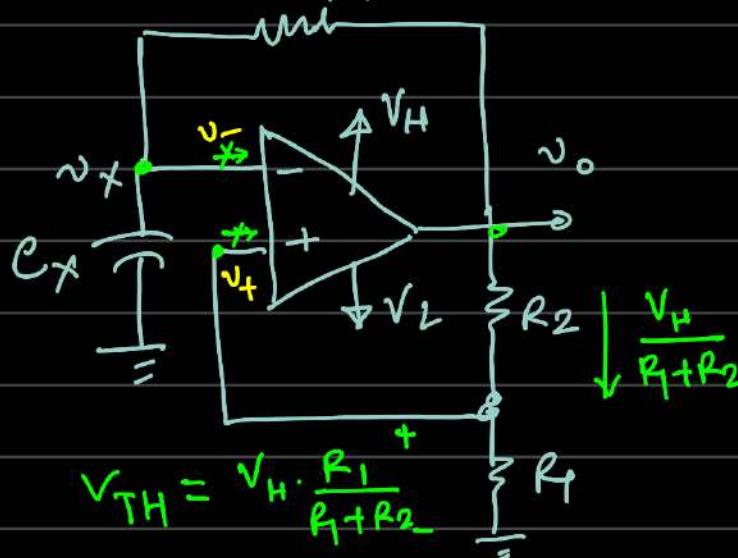
$$V_{UT} = V_{TH}, V_{LT} = V_{TL}.$$

$$V_H = (+V_{sat}), V_L = (-V_{sat})$$

$|+V_{sat}| \neq |-V_{sat}|$  [Problematic issue in Coughlin's book]

# Steady State Behavior

Case 1 :  $0 < t < T_1$



Initially,  $v_{initial} = v_x(t=0) = v_{TL}$ ,  $v_o = v_H$

Up until  $v_x < v_{TH}$ , the output will remain at  $v_H$ .

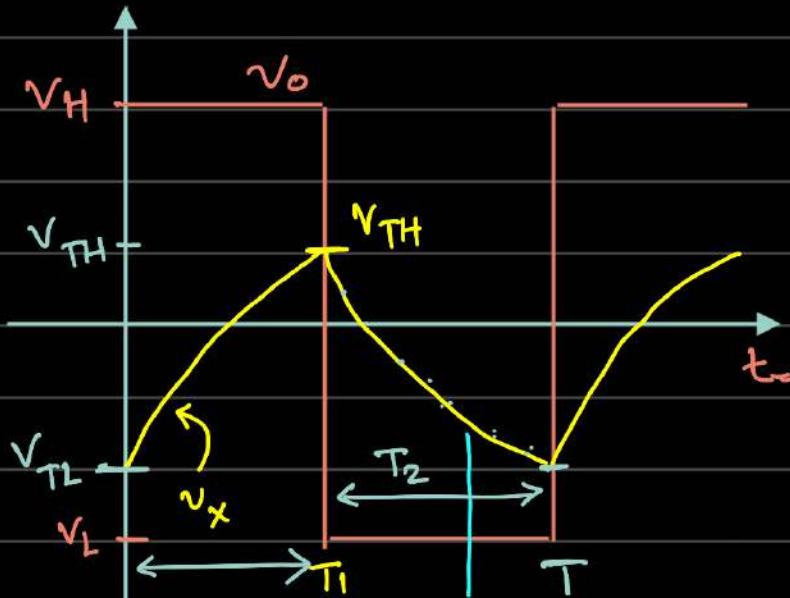
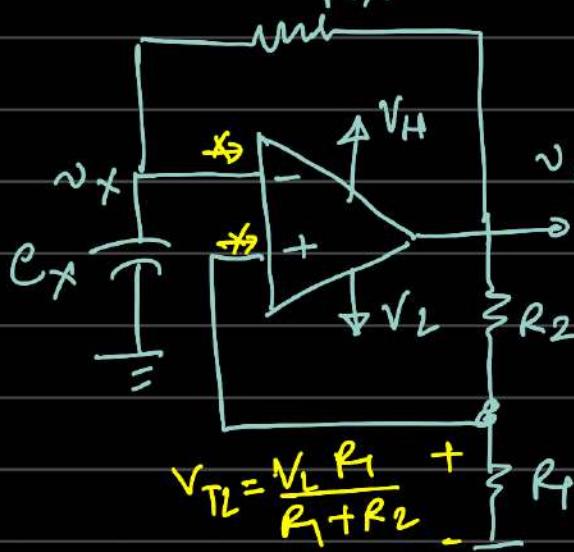
$$v_x(t) = v_H + (v_{TL} - v_H) \exp\left(-\frac{t-0}{R_x C_x}\right) \quad (0 < t < T_1)$$

At  $v_x(T_1) = v_{TH}$  and after that the output changes to  $v_L$  because now  $v_-$  is greater than  $v_+$ .

$$v_x(T_1) = v_{TH} = v_H + (v_{TL} - v_H) \exp\left(-\frac{T_1}{R_x C_x}\right)$$

$$\Rightarrow T_1 = R_x C_x \ln\left(\frac{v_H - v_{TL}}{v_H - v_{TH}}\right)$$

Case 2 :  $T_1 < t < T_2$



$$v_x(T_1) = V_{\text{initial}} = V_{TH}$$

$$v_x(t) = V_L + (V_{TH} - V_L) \exp\left(-\frac{t - T_1}{R_x C_x}\right)$$

$$T_2 = T - T_1 \quad \text{and} \quad v_x(T) = V_{TL}$$

After  $t > T$ ,  $v_x$  will be less than  $V_L$  and that changes the output voltage  $v_o = V_L$  to  $v_o = V_H$ .

$$v_x(T) = V_{TL} = V_L + (V_{TH} - V_L) \exp\left(-\frac{T - T_1}{R_x C_x}\right) \xrightarrow{T_2}$$

$$\Rightarrow T_2 = R_x C_x \ln\left(\frac{V_L - V_{TH}}{V_L - V_{TL}}\right)$$

Neumann 15.8 For the Schmitt trigger oscillator, the saturation output voltages are +10V and -5V.

$$R_1 = R_2 = 20\text{ k}\Omega, \quad R_x = 50\text{ k}\Omega, \quad \text{and} \quad C_x = 0.01\text{ }\mu\text{F}$$

Determine the frequency of oscillation and duty cycle.

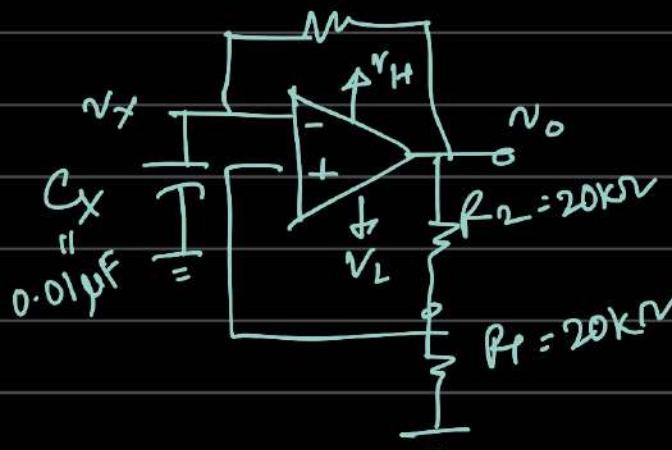
Sol<sup>n</sup>:

$$R_x = 50\text{ k}\Omega$$

$$V_{TH} = \frac{V_H R_1}{R_1 + R_2} = \frac{10 \times 20}{20 + 20} = 5\text{ V}$$

$$V_{TL} = \frac{V_L R_1}{R_1 + R_2} = \frac{-5 \times 20}{20 + 20} = -2.5\text{ V}$$

$$\tau = R_x C_x = 50 \times 10^3 \times 0.01 \times 10^{-6} = 0.5 \times 10^{-3} \text{ s} = 0.5 \text{ ms}$$



$T_1$  = voltage high time duration

$$= \tau \ln\left(\frac{V_H - V_{TL}}{V_H - V_{TH}}\right)$$

$$= 0.5 \ln\left(\frac{10 - (-2.5)}{10 - 5}\right) = 0.5 \ln(2.5)$$

$T_2$  = voltage low time duration =  $\tau \ln\left(\frac{V_L - V_{TH}}{V_L - V_{TL}}\right)$

$$= 0.5 \ln\left(\frac{-5 - 5}{-5 - 2.5}\right) = 0.5 \ln(4)$$

$$\text{Total period, } T = T_1 + T_2 = 0.5 \ln(2.5 \times 4) = 0.5 \ln(10)$$

$$\text{Frequency} = \frac{1}{T} = \frac{1}{0.5 \ln(10) \text{m}} = 0.868 \text{ KHz} = 868 \text{ Hz}$$

Duty cycle = % of time voltage is high

$$= \frac{T_1}{T} \times 100\% = \frac{\ln(2.5)}{\ln(10)} \times 100\% = 39.1\%$$

## # Triangular Wave Generator

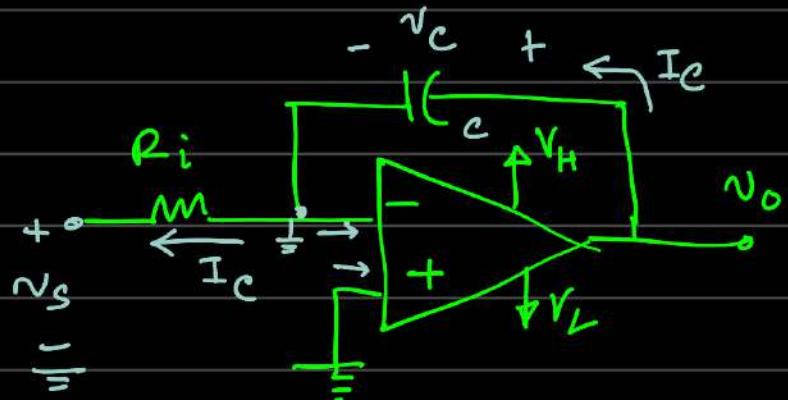
### Integrator:

$$I_C = C \frac{dV_C}{dt} = \frac{0 - V_S}{R_i}$$

$$V_C(t) = \frac{V_S}{R_i C} t$$

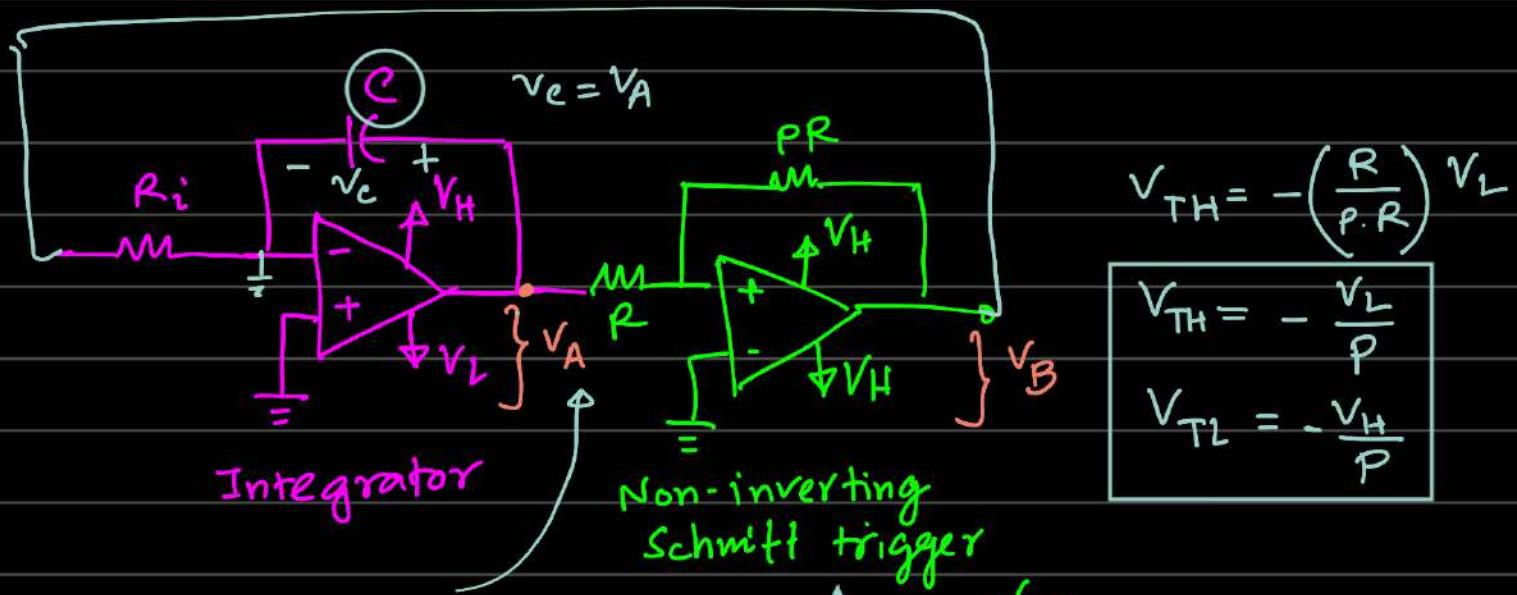
$$\Rightarrow \int \frac{dV_C}{V_S} = - \int \frac{dt}{R_i C}$$

$$V_{initial} \quad t_1$$



$$\Rightarrow V_C(t) - V_{initial} = - \frac{(t - t_1)}{R_i C} \Rightarrow V_C(t) = V_{initial} - \frac{V_S}{R_i C} (t - t_1)$$

## Circuit of Triangular Wave Generator:

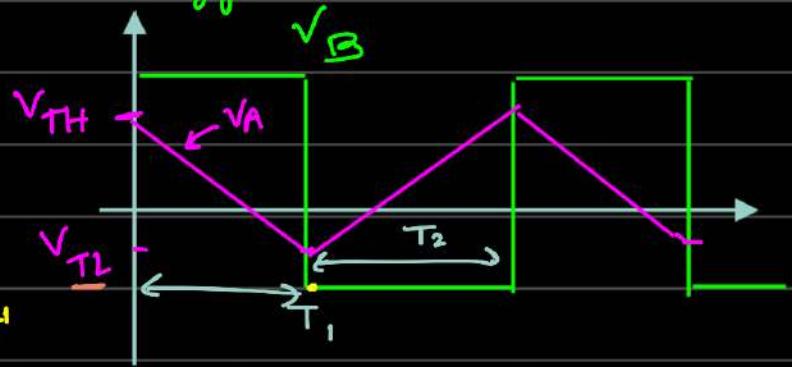


Triangular wave

Case 1:  $0 < t < T$

$$V_C(t) = V_{initial} - \frac{V_S}{R_i C} (t - 0)$$

$$V_C(T_1) = V_{TL} \text{ and } V_C(0) = V_{TH}$$



$$V_C(T_1) = V_{TL}, \quad V_{initial} = V_{TH}$$

$$T_1 = R_i C \left( \frac{V_{TH} - V_{TL}}{V_H} \right)$$

By doing similar calculation one can derive.

$$T_2 = R_i C \left( \frac{V_{TL} - V_{TH}}{V_L} \right)$$

Therefore, total time period becomes,

$$T = T_1 + T_2$$

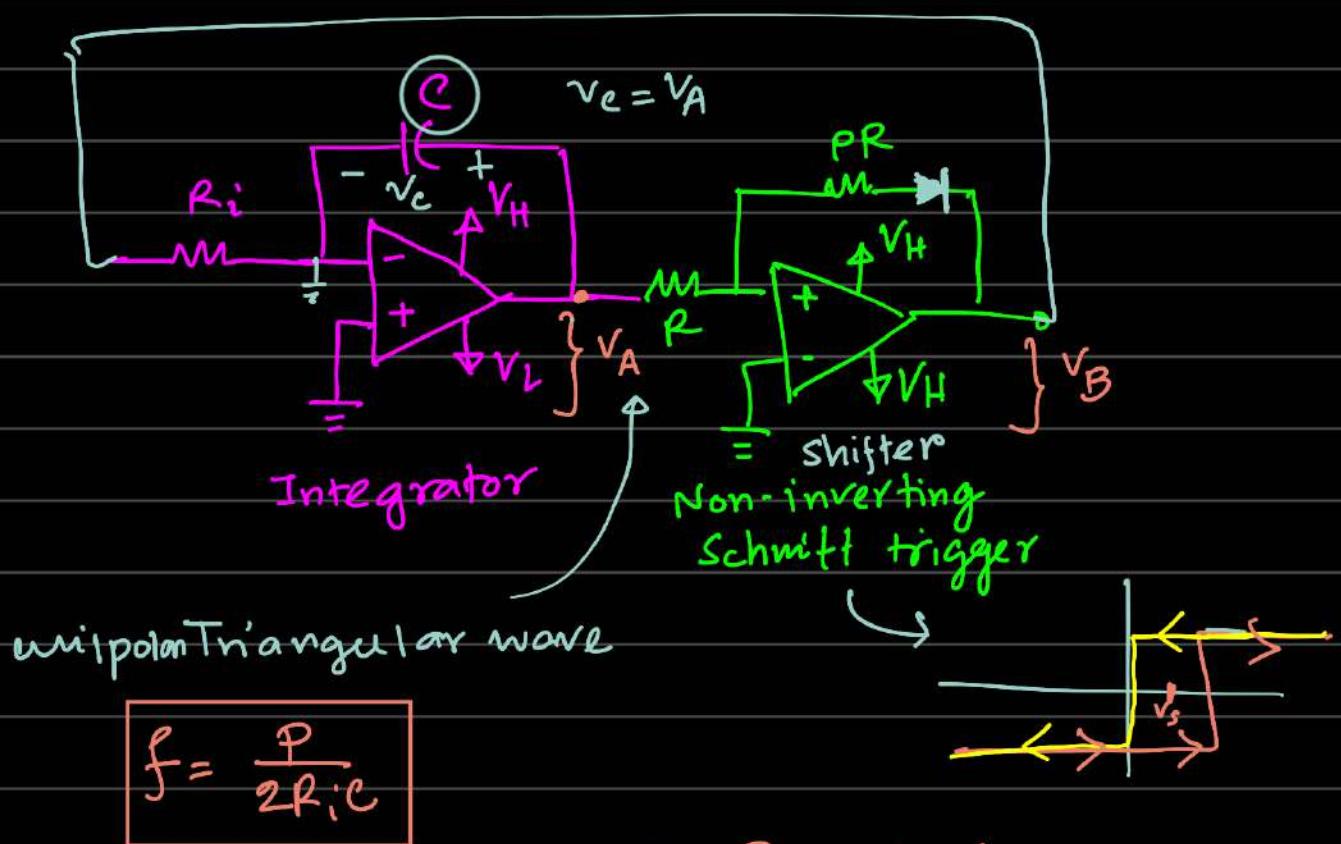
$$T = \left( \frac{V_{TH} - V_{TL}}{V_H} + \frac{V_{TL} - V_{TH}}{V_L} \right) \times R_i C$$

$$f = \frac{1}{T} \text{ suppose. } [V_H = -V_L \text{ and } V_{TH} = -\frac{V_L}{P}]$$

$$f = \frac{P}{4R_i C}$$

$$V_{TL} = -\frac{V_H}{P}$$

# Unipolar triangular wave generator:



Details are in Bux lecture.