Basic I/O Interfacing
8255 or 82C55

The programmable peripheral Interface

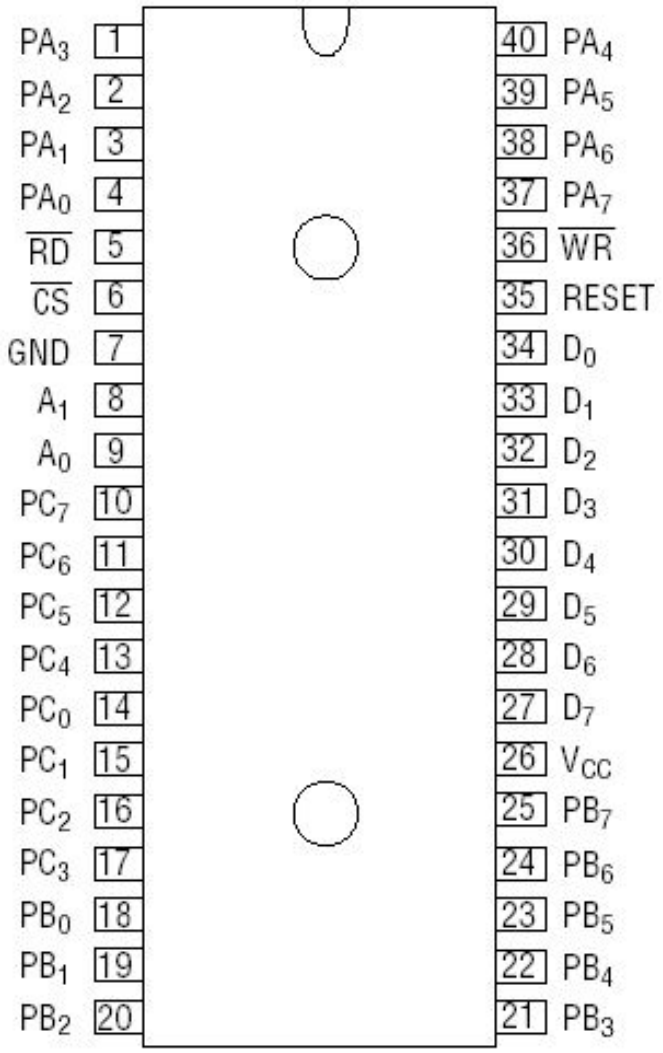
The 82C55 **programmable peripheral interface (PPI)** is a very popular low-cost interfacing component that is used found in many applications.

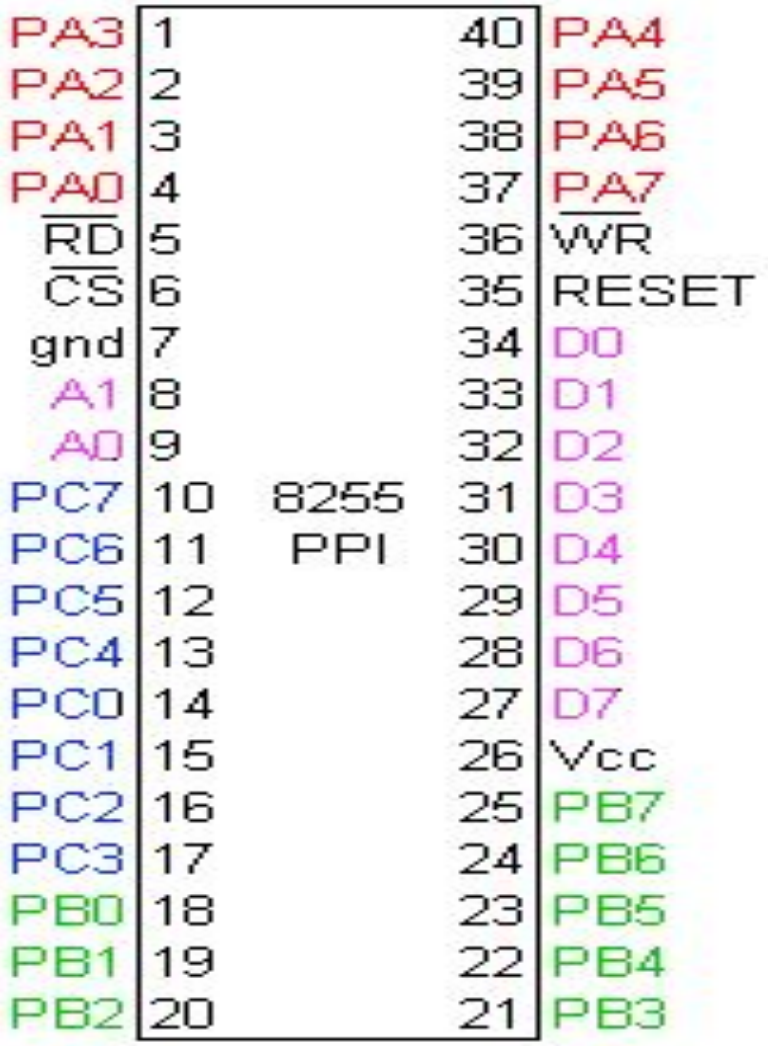
Applications range from 7-segment display, stepper motor connection, counters to key pad management.

This device is still in use today and is used to interface and detect key presses on modern keyboards, parallel printers and other interfacing chipsets.

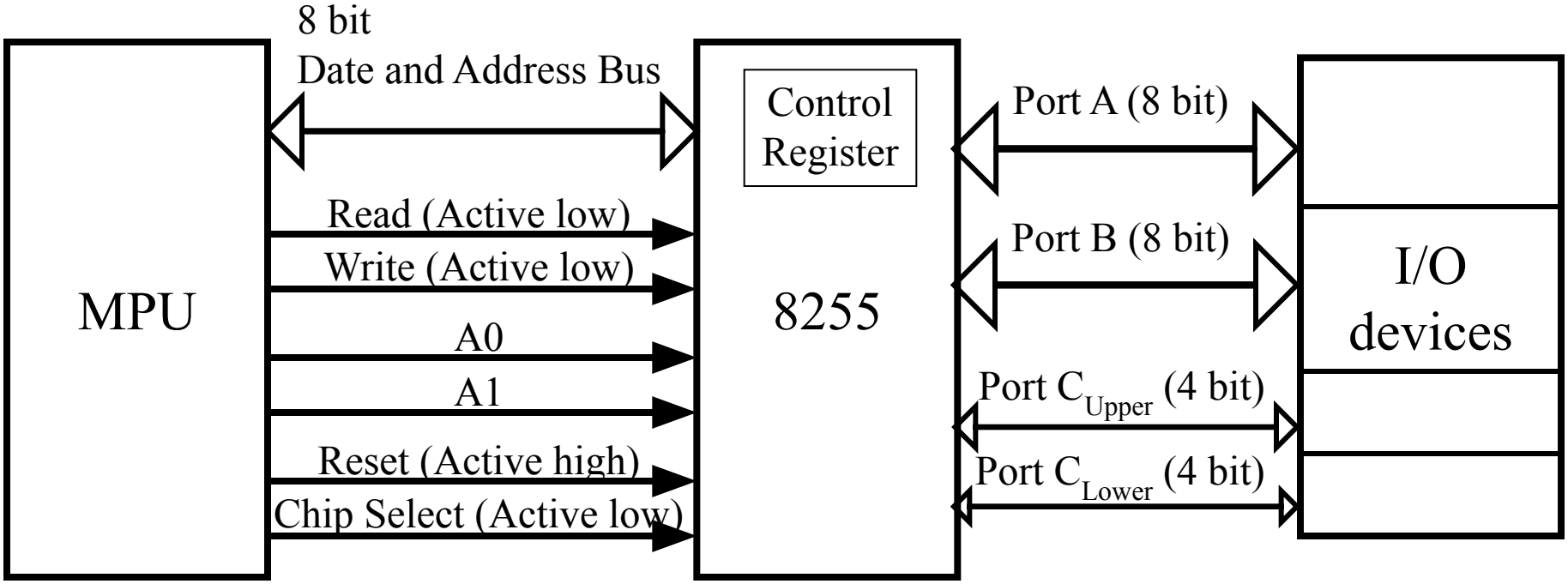
For those of you who are doing computer interfacing course you will be extensively using this device to interface various devices with the PC.

Pin Diagram 8255



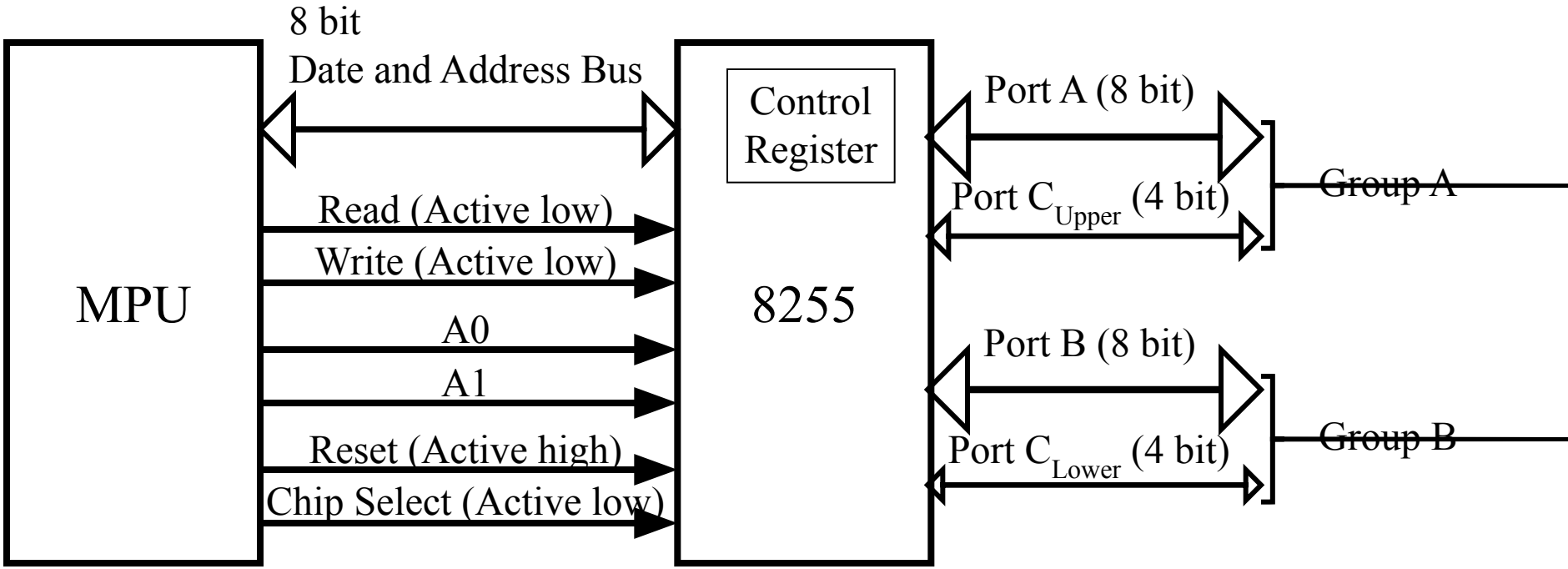


Connection Diagram



A1	A0	Function
0	0	Port A
0	1	Port B
1	0	Port C
1	1	Command Registers

Connection Diagram



82C55

This devices has 24 pins for I/O.

The I/O pins can be programmed in groups of 12 pins.

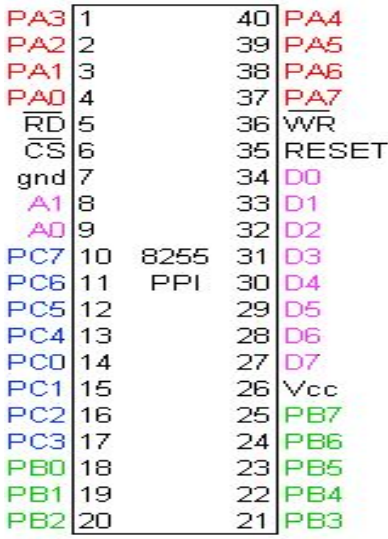
There are three distinct modes of operation Mode 0, Mode 1 and Mode 2.

Group A connections consists of Port A(PA0-PA7) and the upper half of port C (PC4-PC7)

Group B connections consists of Port B (PB0-PB7) and the lower half of port C (PC0-PC3)

Function of pins:

- Data bus(D_0-D_7):These are 8-bit bi-directional buses, connected to 8085 data bus for transferring data.



- $\overline{CS}$: This is Active Low signal. When it is low, then data is transfer from 8085.

- $\overline{Read}$: This is Active Low signal, when it is Low read operation will start.

- $\overline{Write}$: This is Active Low signal, when it is Low Write operation will start.

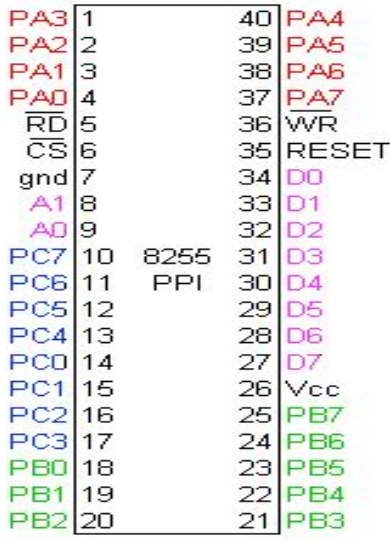
82C55

CS pin is used to select the device for reading or writing.

Control lines A0 and A1 are used to select the Port that requires interaction.

A1	A0	Function
0	0	Port A
0	1	Port B
1	0	Port C
1	1	Command Registers

- RESET: This is used to reset the device. That means clear control registers.



- PA_0-PA_7:It is the 8-bit bi-directional I/O pins used to send the data to peripheral or to receive the data from peripheral.

- PB_0-PB_7:Similar to PA

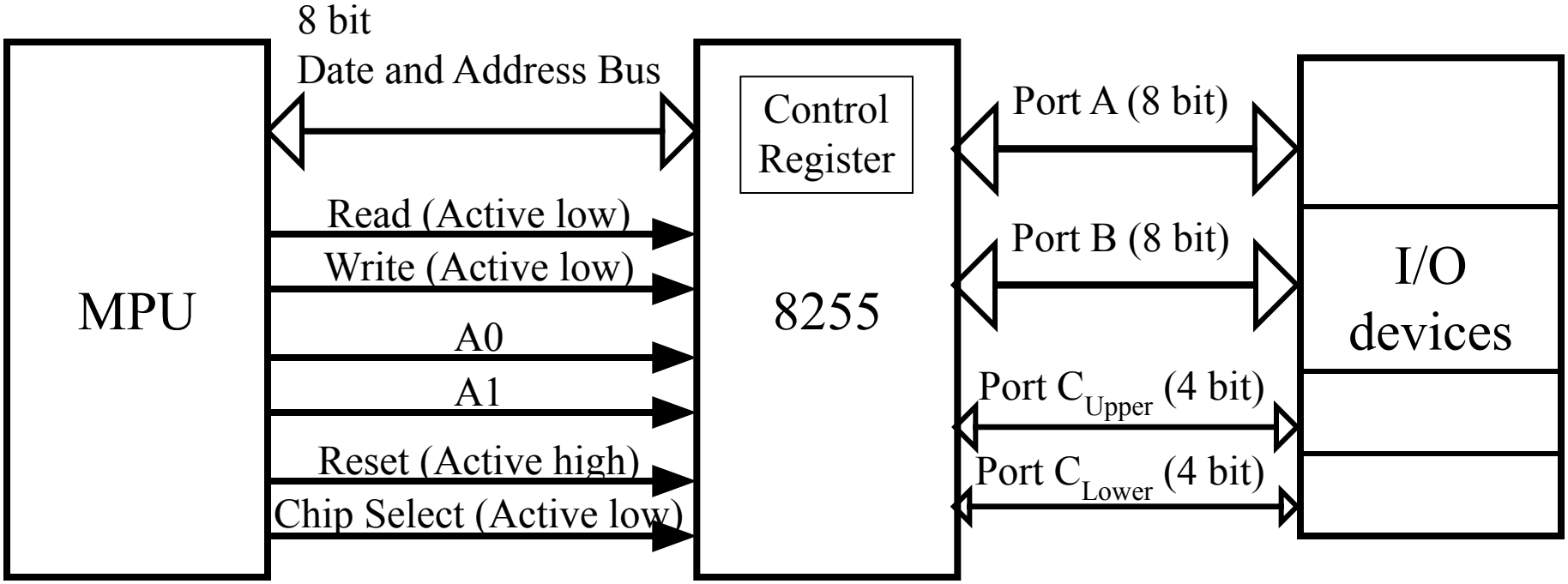
- PC_0-PC_7:This is also 8-bit bidirectional I/O pins. These lines are divided into two groups.

  PC_0 to PC_3(Lower Groups)

  PC_4 to PC_7 (Higher groups)

  These two groups working in separately using 4 data's.

Connection Diagram



A1	A0	Function
0	0	Port A
0	1	Port B
1	0	Port C
1	1	Command Registers

Click on Correct Answer

A1	A0	$\overline{RD}$	$\overline{WR}$	$\overline{CS}$	Reset
0	0	1	0	0	0

Data Bus Port A
Data Bus Port C
Data Bus Control

A1	A0	$\overline{RD}$	$\overline{WR}$	$\overline{CS}$	Reset
1	0	0	1	1	0

Data Bus Port C
Data Bus Port C
Nothing Happen

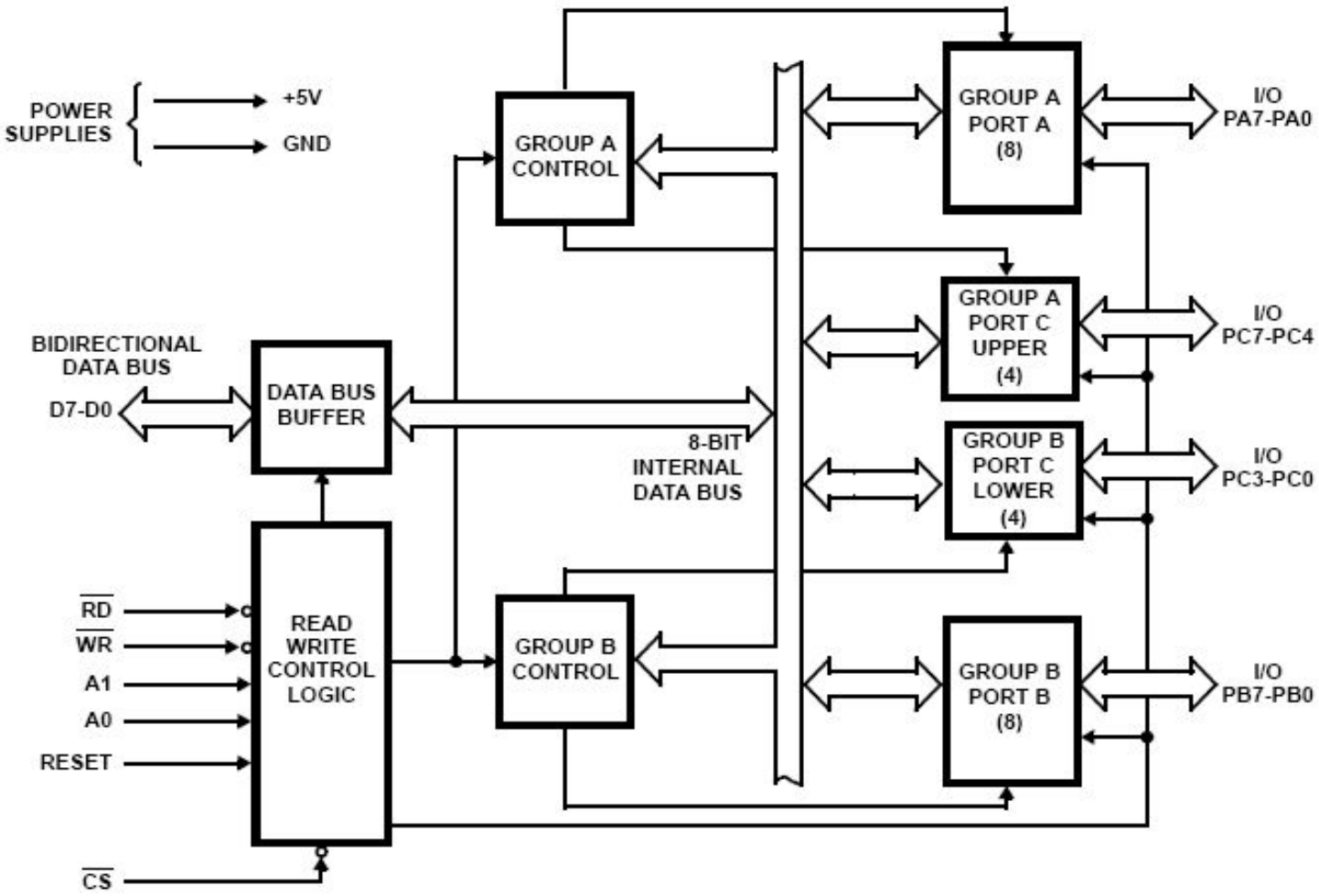
A1	A0	$\overline{RD}$	$\overline{WR}$	$\overline{CS}$	Reset
1	1	1	0	0	0

Data Bus Port A
Data Bus Port C
Data Bus Control

A1	A0	$\overline{RD}$	$\overline{WR}$	$\overline{CS}$	Reset
0	1	0	1	0	0

Date Bus Port B
Date Bus Port B
Date Bus Control

Block Diagram



Data Bus buffer:

- It is a 8-bit bidirectional Data bus.
- Used to interface between 8255 data bus with system bus.
- The internal data bus and Outer pins D_0-D_7 pins are connected in internally.
- The direction of data buffer is decided by Read/Control Logic.

Group A and Group B control:

- Group A and B get the Control

  Signal from CPU and send the command to the individual control blocks.
- Group A send the control signal to port A and Port C (Upper) PC_7-PC_4.
- Group B send the control signal to port B and Port C (Lower) PC_3-PC_0.
- PORT A:
- This is a 8-bit buffered I/O latch.
- It can be programmed by mode 0 , mode 1, mode 2 .

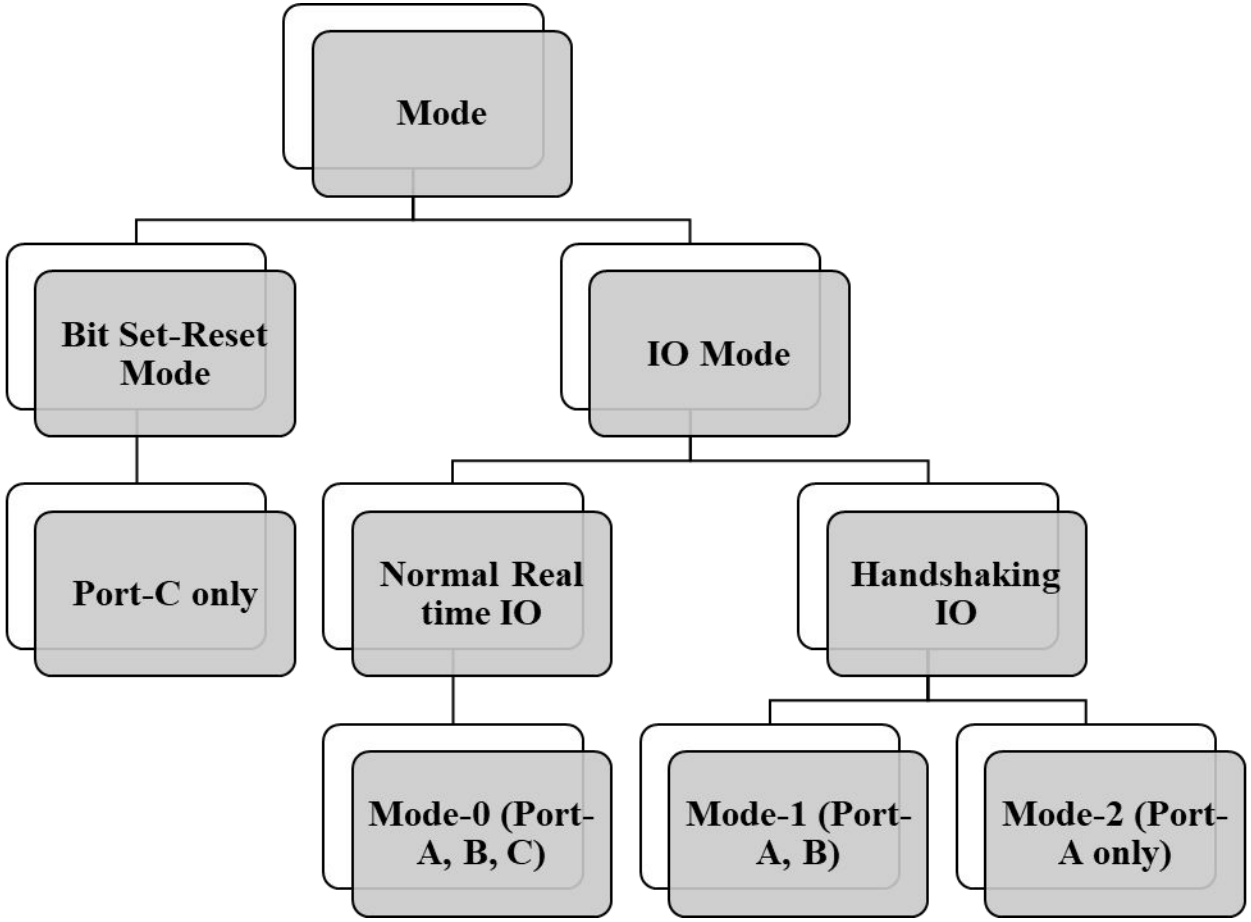
PORT B:

- This is a 8-bit buffer I/O latch.
- It can be programmed by mode 0 and mode 1.

• PORT C:

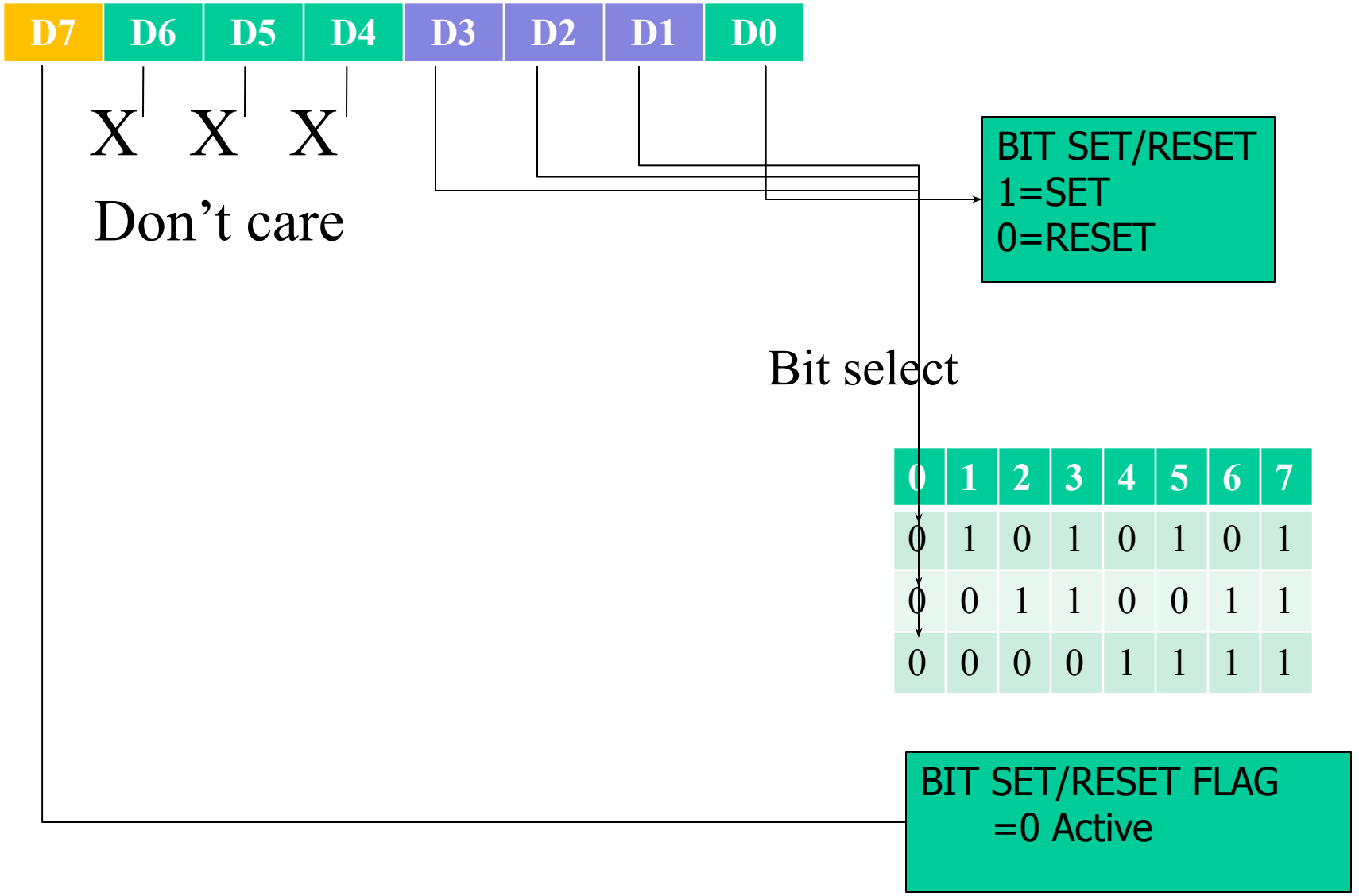
- This is a 8-bit Unlatched buffer Input and an Output latch.
- It is splitted into two parts.
- Support only mode 0
- It can be programmed by bit set/reset operation.

Mode


Mode
Bit Set-Reset Mode
IO Mode
Port-C only
Normal Real time IO
Handshaking IO
Mode-0 (Port-A, B, C)
Mode-1 (Port-A, B)
Mode-2 (Port-A only)

FOR BIT SET/RESET MODE:

- This is bit set/reset control word format.

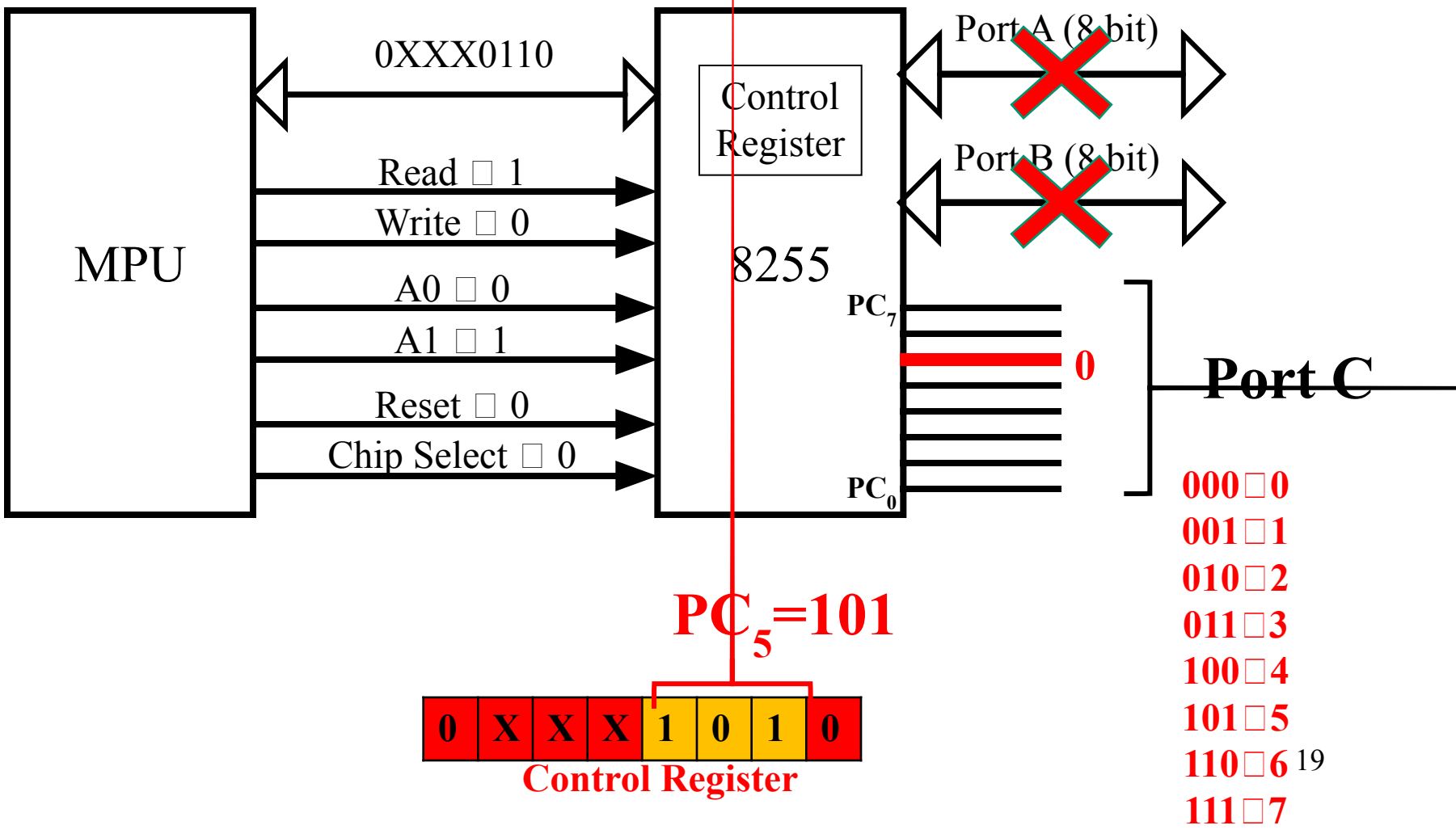


Operation modes:

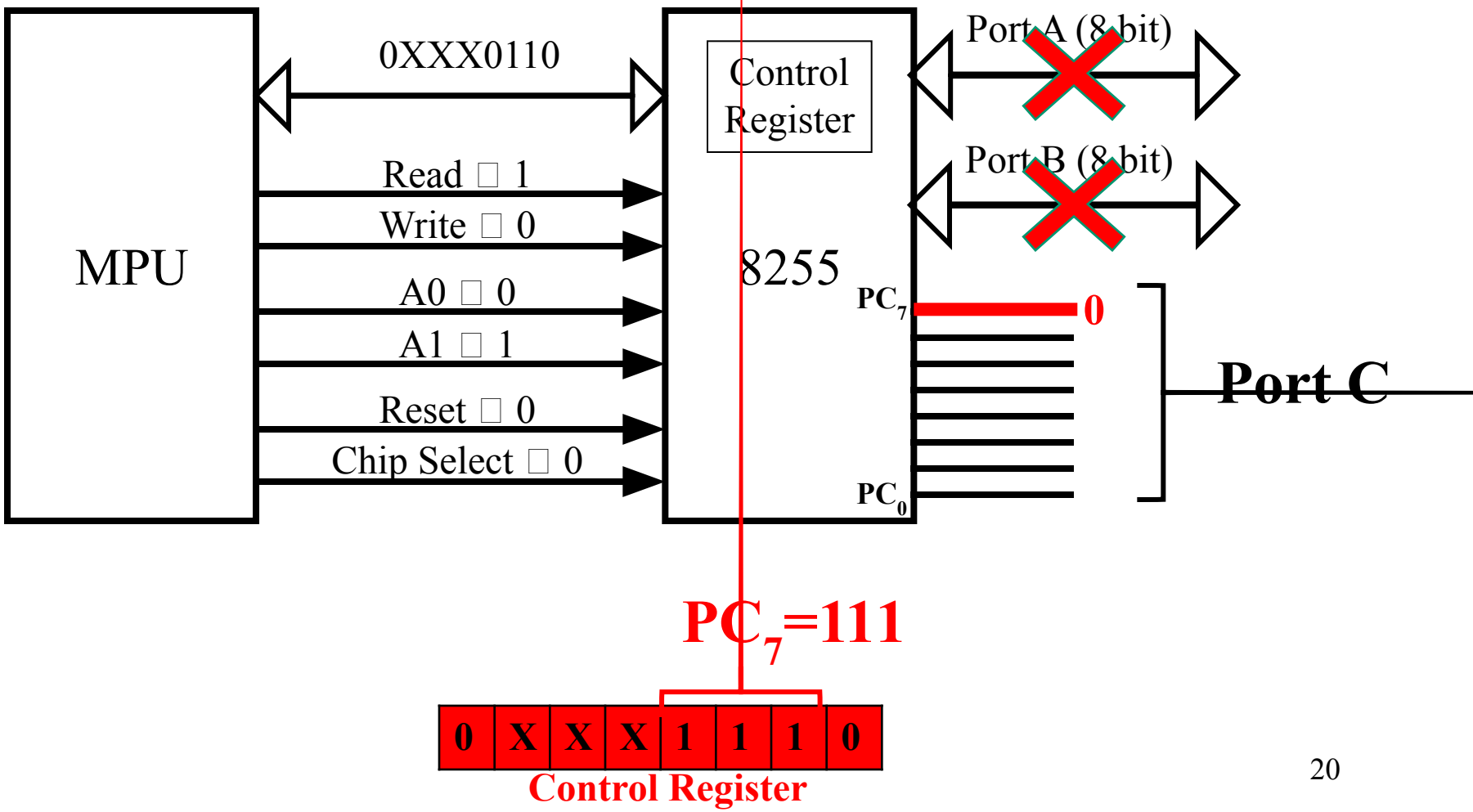
BIT SET/RESET MODE:

- A pin of PORT C (PC_0-PC_7)can be Set or Reset by sending OUT instruction to the CONTROL registers.
- Example:
- PC_3 is Set then control register will be 0XXX0111.
- PC_4 is Reset then control register will be 0XXX1000.
- X is a don’t care.

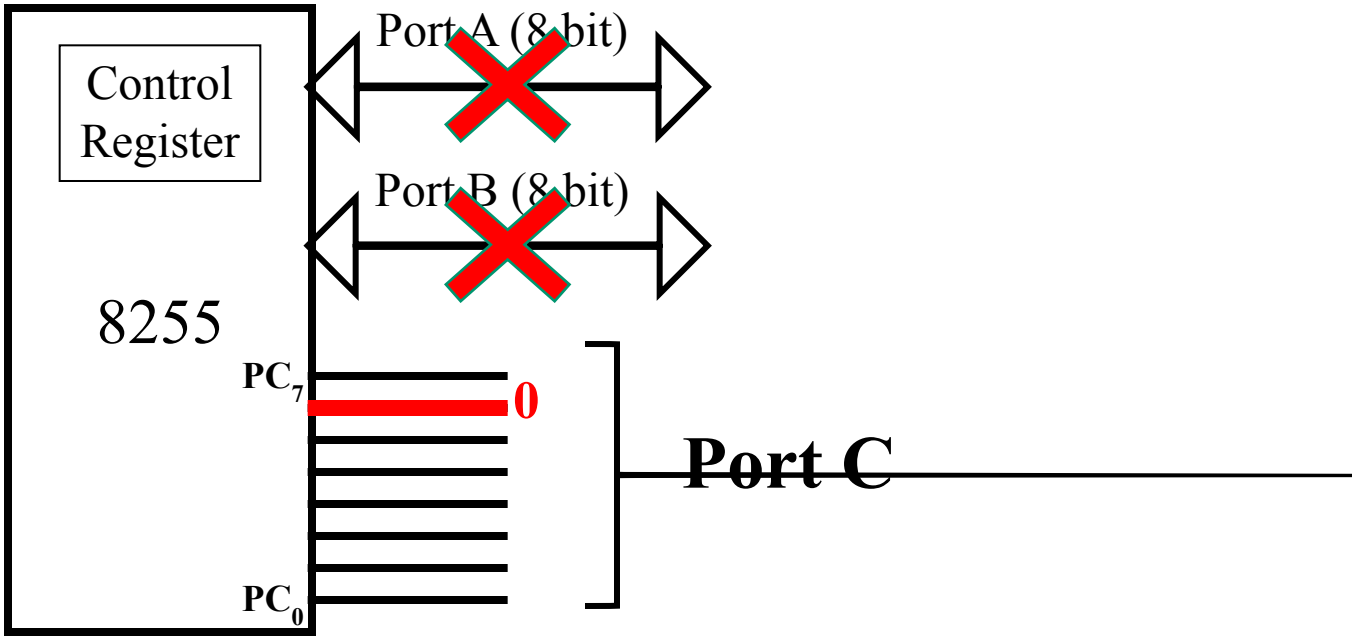
Bit Set-Reset Mode



Bit Set-Reset Mode



Bit Set-Reset Mode



Click on Correct Answer

01110100□

PC7 Set
PC2 Reset
Both are wrong answer

We want to PC5 set□

01010XXX
0XXX1010
0XXX1011

00000000□

PC0 Set
PC7 Reset
Both are wrong answer

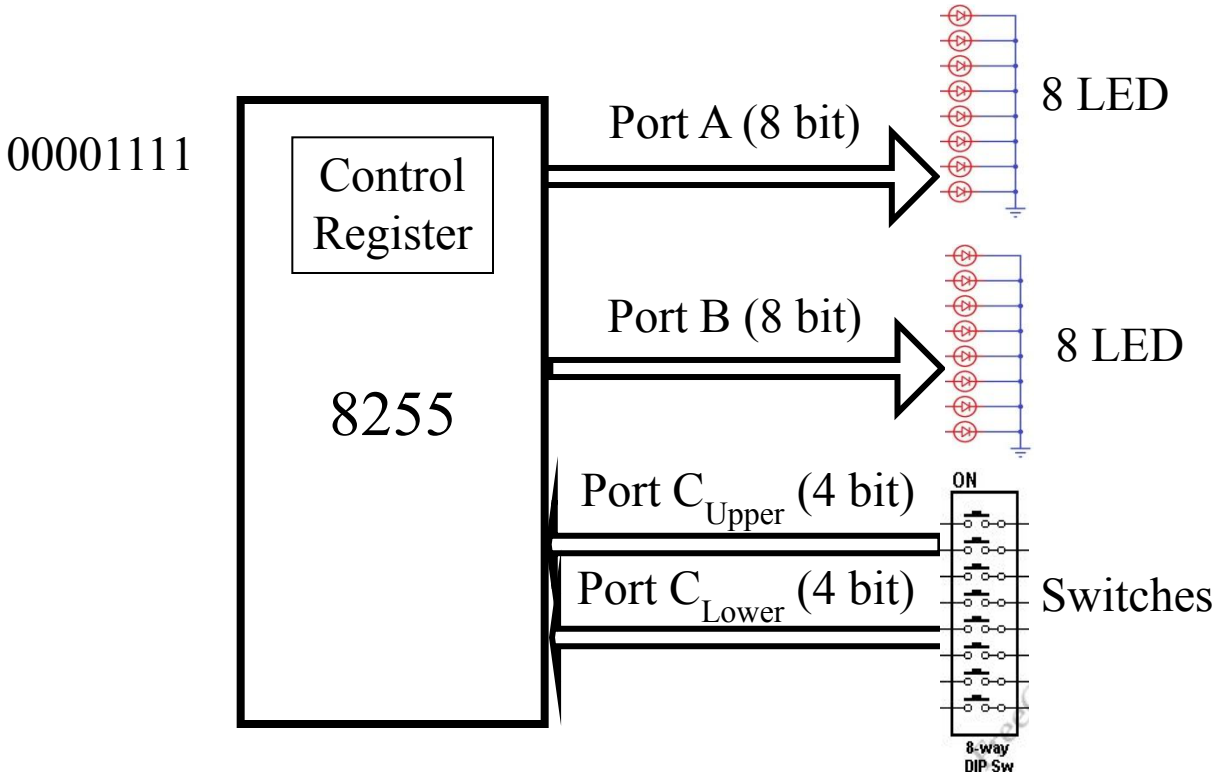
01010101□

PC2 Set
PC2 Reset
In I/O Mode

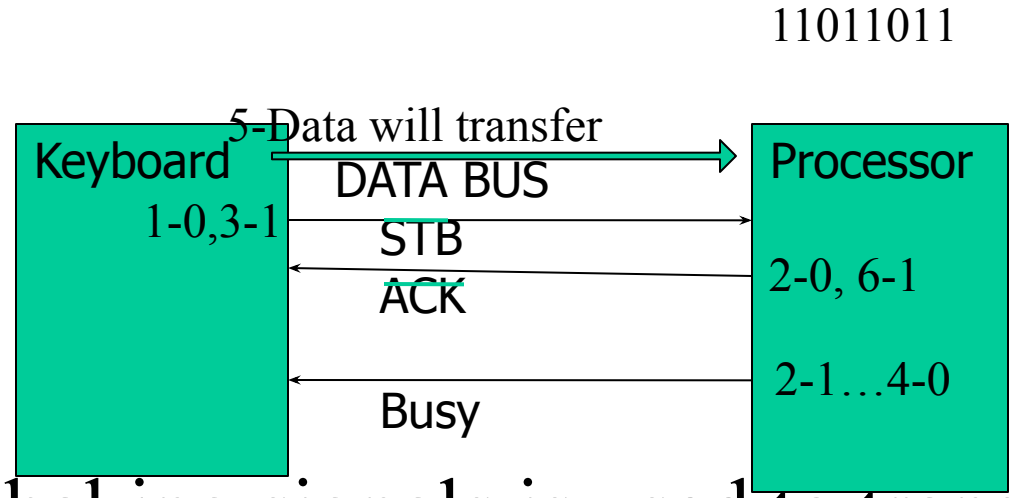
I/O MODES

- MODE 0(Simple input / Output):
- In this mode , port A, port B and port C is used as individually (Simply).
- Features:
- Outputs are latched, Inputs are buffered not latched.
- Ports do not have Handshake or interrupt capability.

Mode-0


00001111
Control Register
8255
Port A (8 bit)
Port B (8 bit)
Port C$_{Upper}$ (4 bit)
Port C$_{Lower}$ (4 bit)
8 LED
8 LED
Switches
ON
8-way DIP Sw

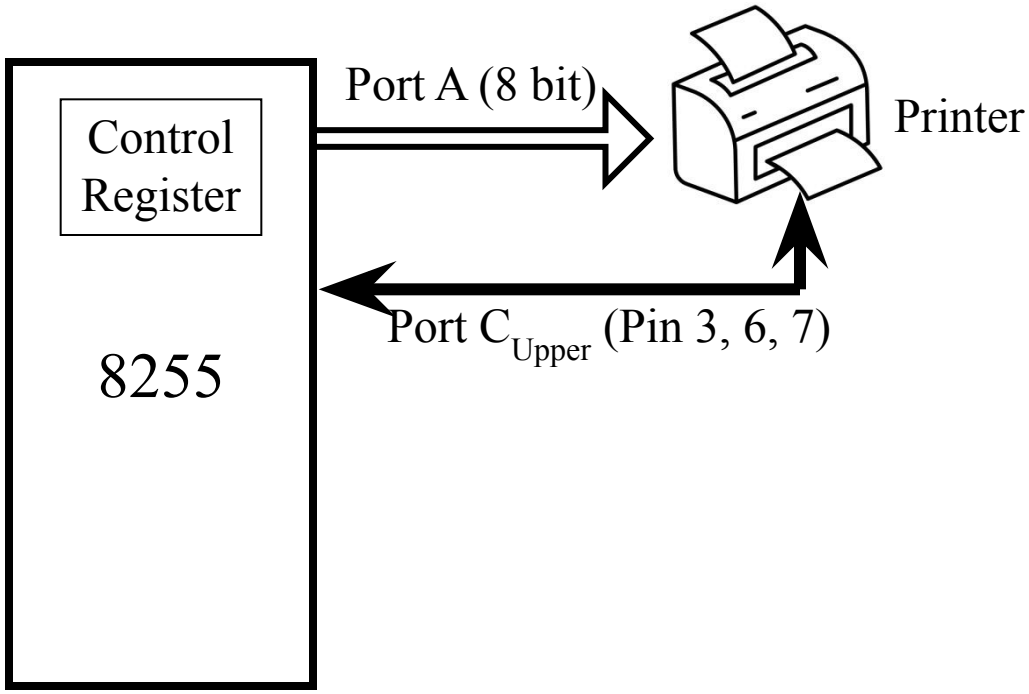
- MODE 1 :(Input/output with Hand shake)
- In this mode, input or output is transferred by hand shaking Signals.



- Handshaking signals is used to transfer data between whose data transfer rate is not same.

- Example:
- The computer send the data to the printer large speed compared to the printer.
- When computer send the data according to the printer speed at the time only, printer can accept.
- If printer is not ready to accept the data then after sending the data bus , computer uses another handshaking signal to tell printer that valid data is available on the data bus.
- Each port uses three lines from port C as handshake signals

Mode-1

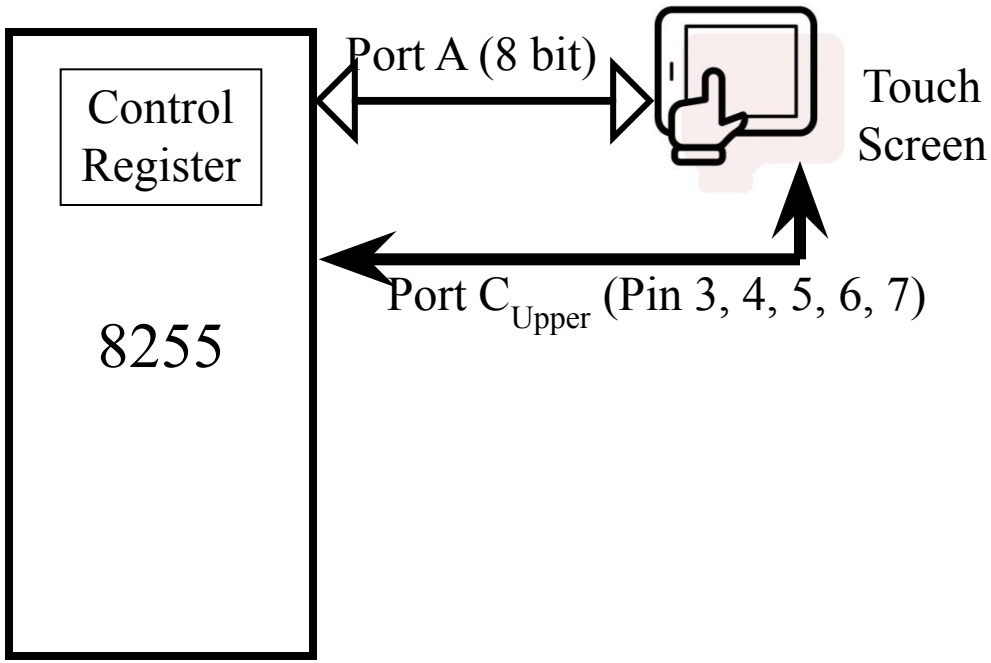

Control
Register
8255
Port A (8 bit)
Printer
Port C$_{Upper}$ (Pin 3, 6, 7)

MODE 2:bi-directional I/O data transfer:

- This mode allows bidirectional data transfer over a single 8-bit data bus using handshake signals.
- This feature is possible only Group A
- Port A is working as 8-biy bidirectional IO.
- PC_3-PC_7 is used for handshaking purpose.
- The data is sent by CPU through this port, when it is required.

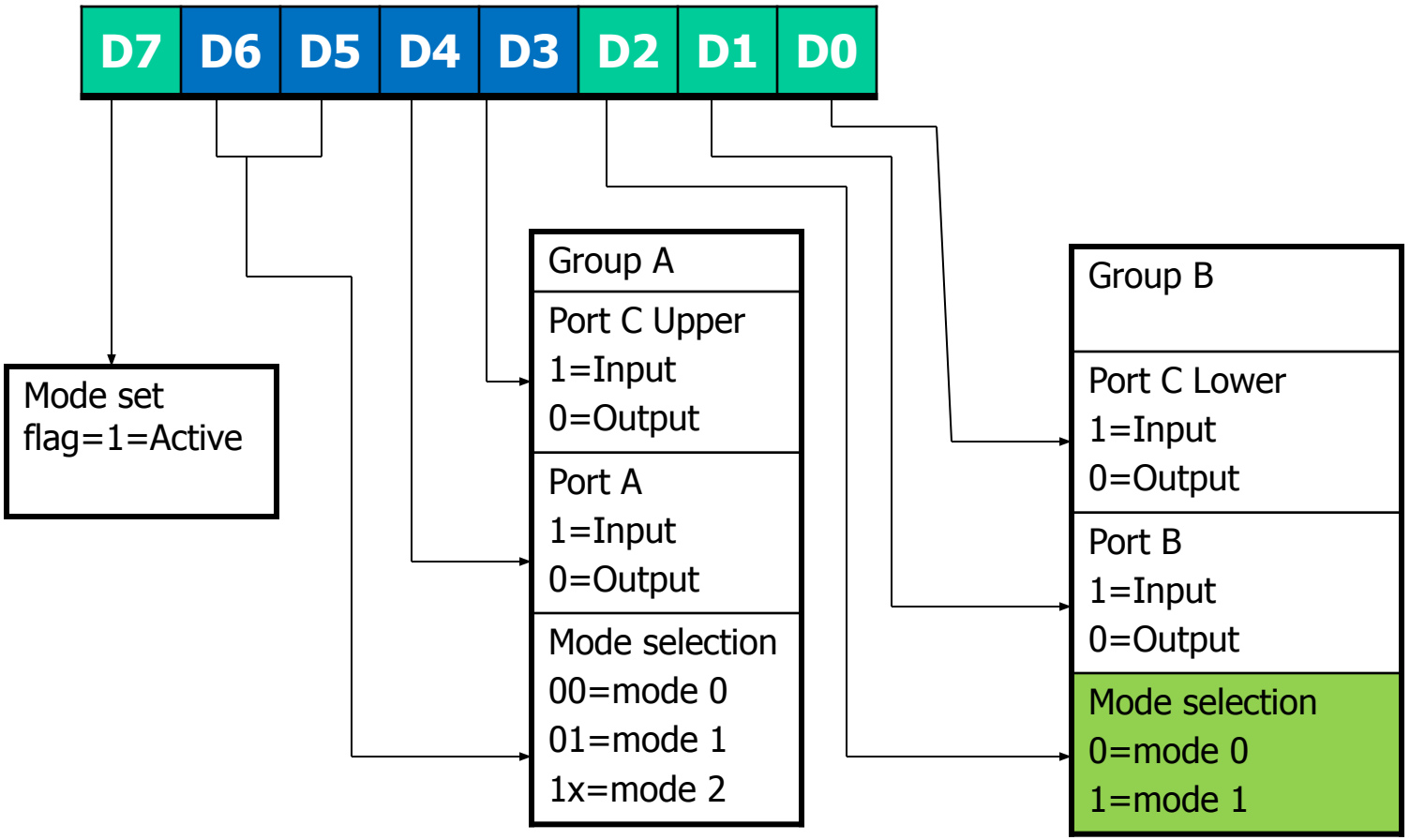
Mode-2

1	1	X	X	X	0	0	1



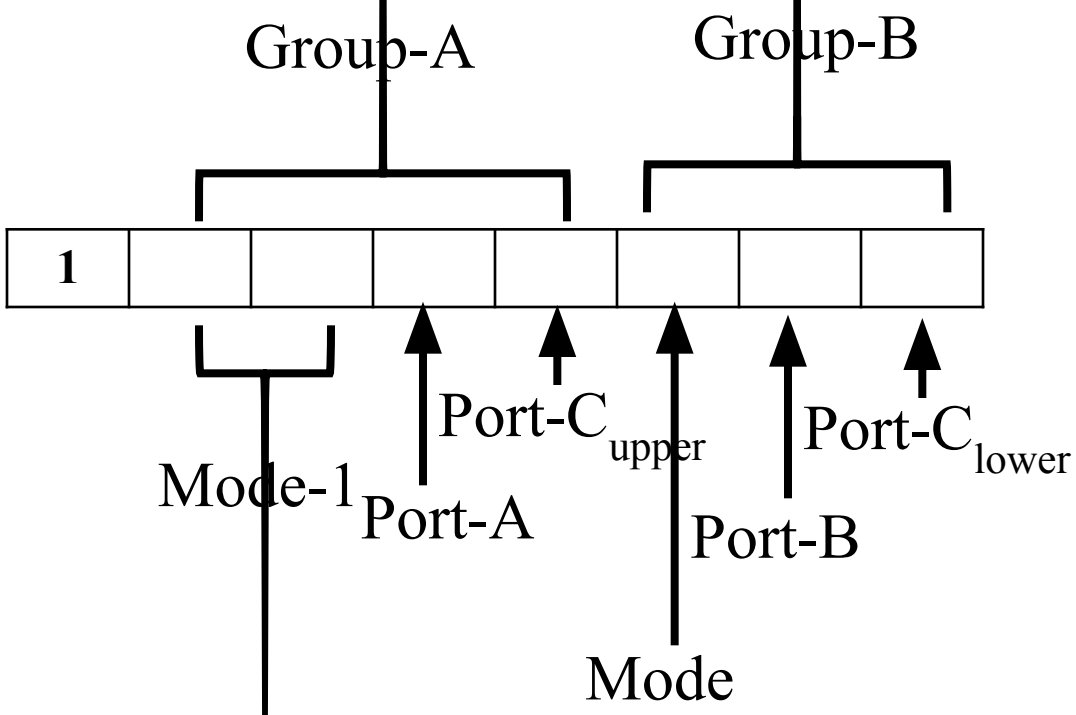
- FOR I/O MODE:

The format of control word

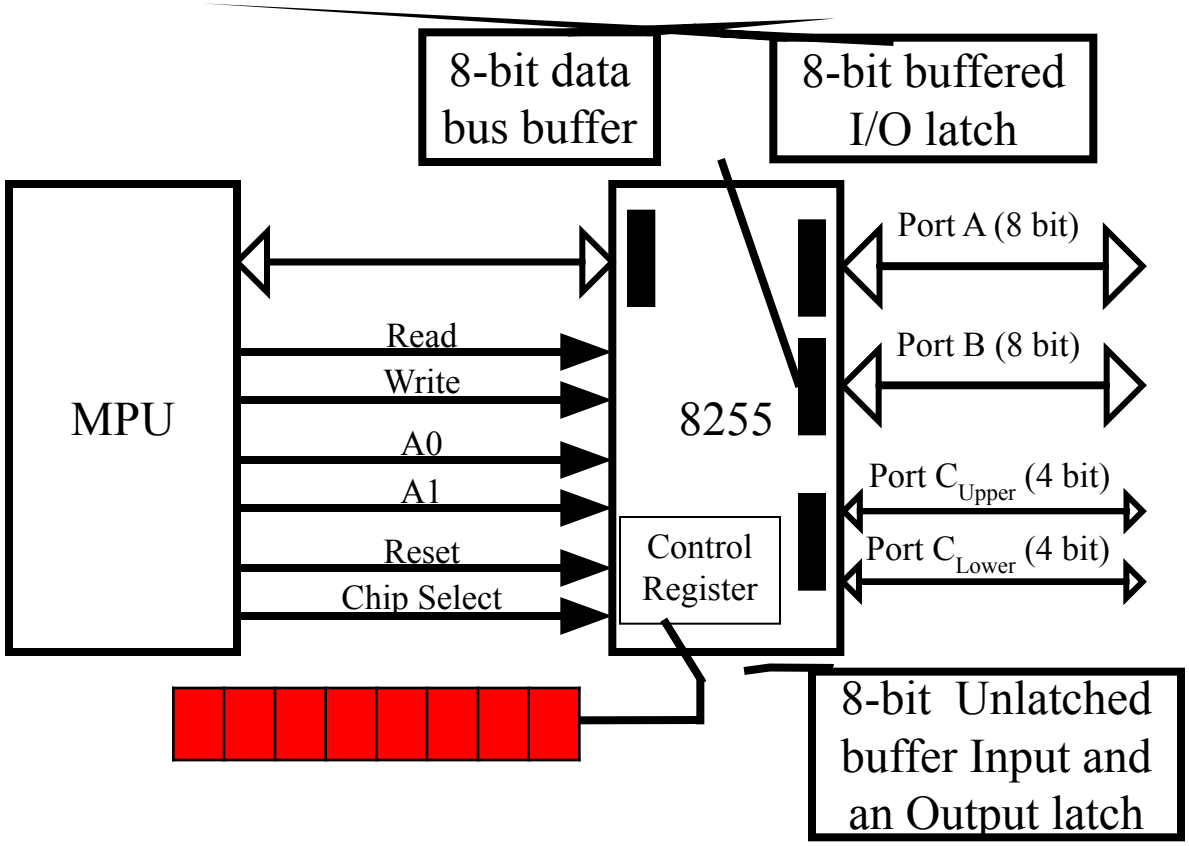


Control word format

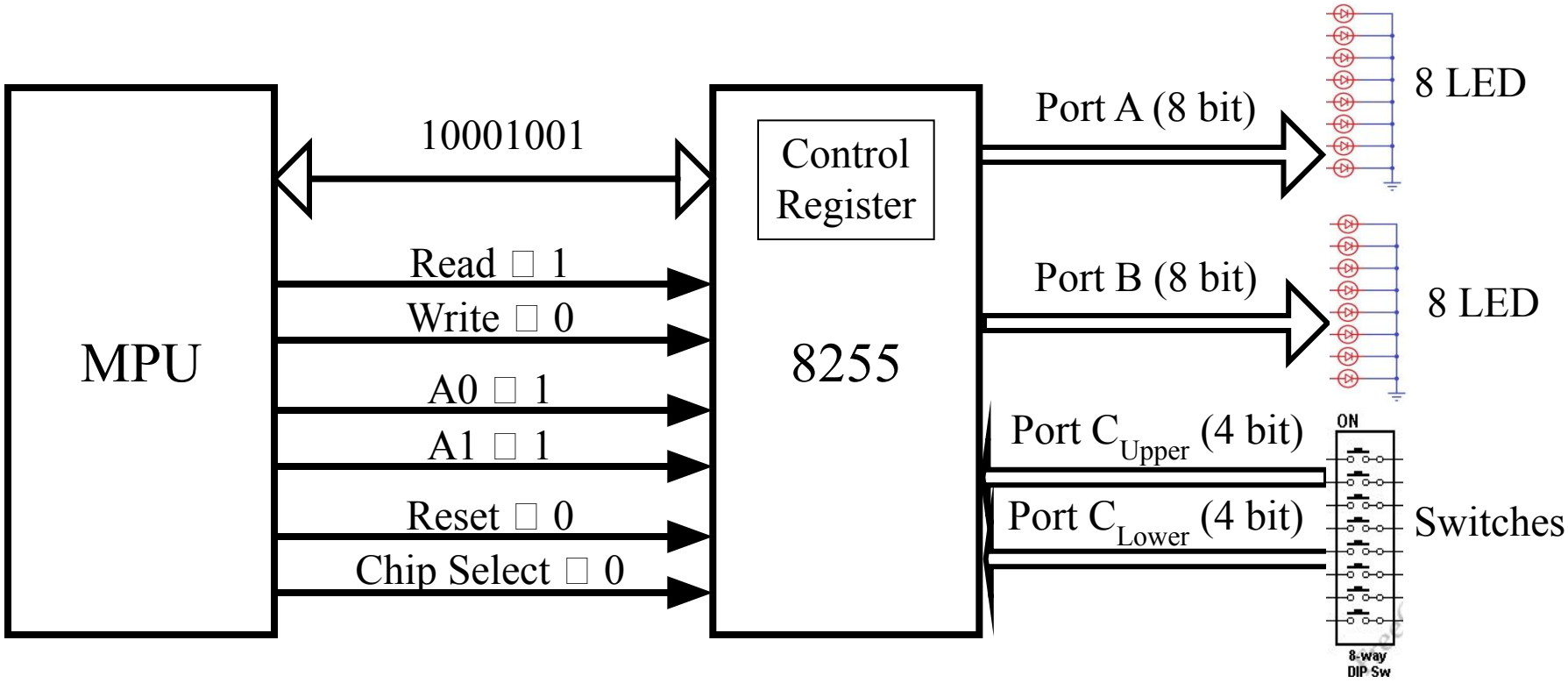
Bit Set-reset/
IO Operation



Details connections of 82C55



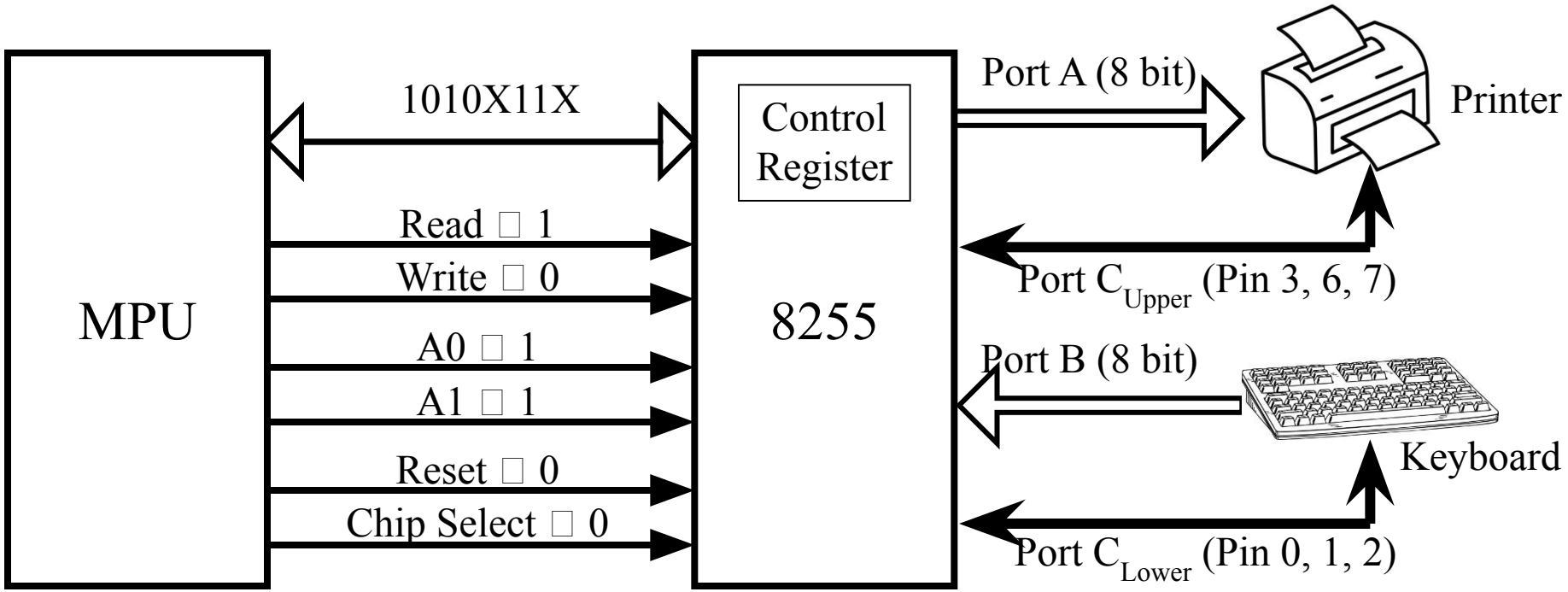
Writing to Control word for Mode-0



1	0	0	0	1	0	0	1

Control Register

Writing to Control word for Mode-1

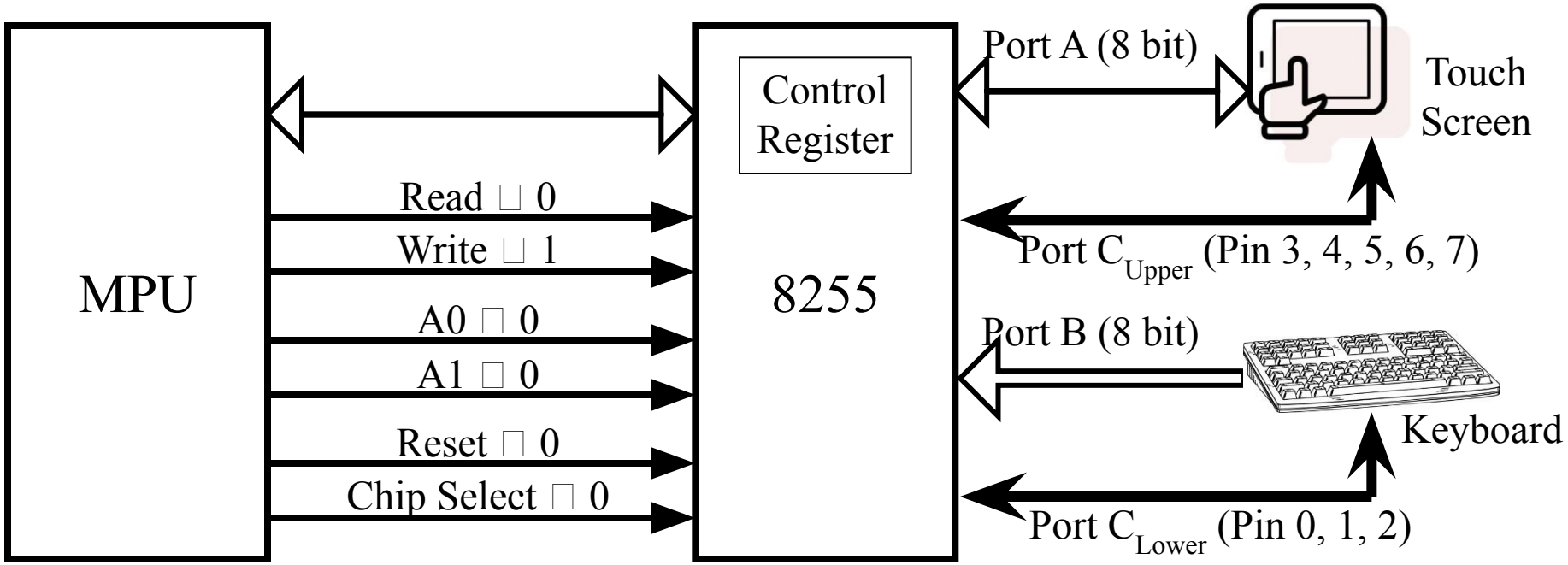


1	0	1	0	X	1	1	X

Control Register

Writing to Control word for Mode-2

1. **Control Register configure**
2. **Input from Keyboard**
3. **Print that to touch screen**
4. **Also read from touch screen**



A1	A0	Function
0	0	Port A
0	1	Port B
1	0	Port C
1	1	Command Registers

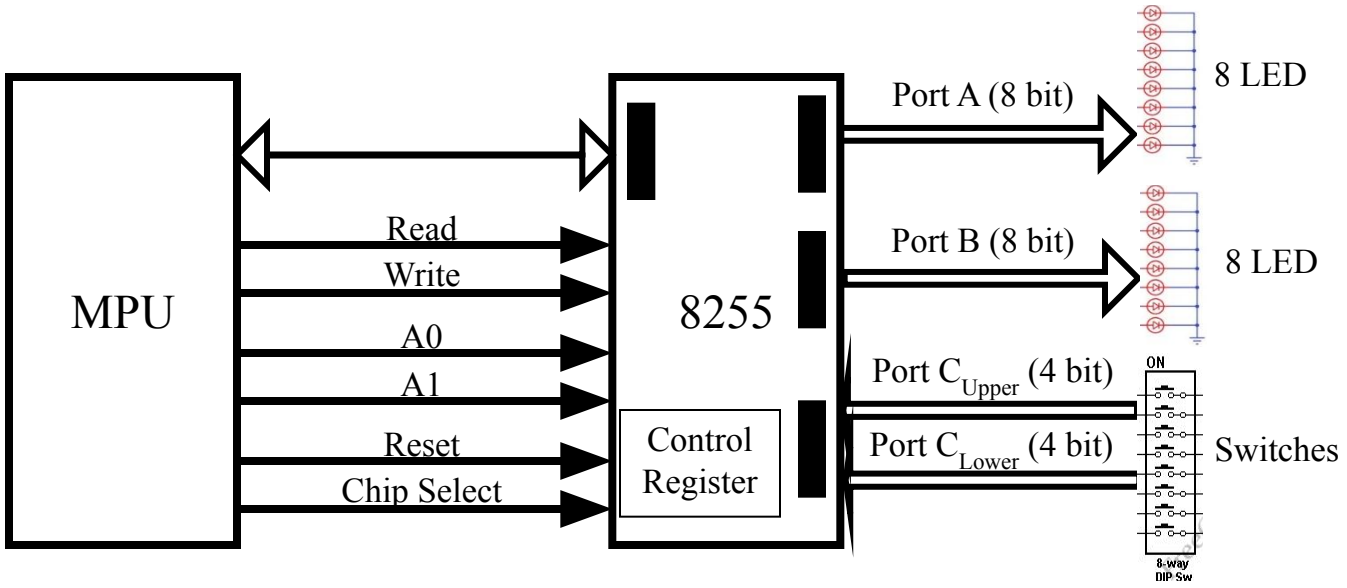
1	1	X	X	X	1	1	X

Control Register

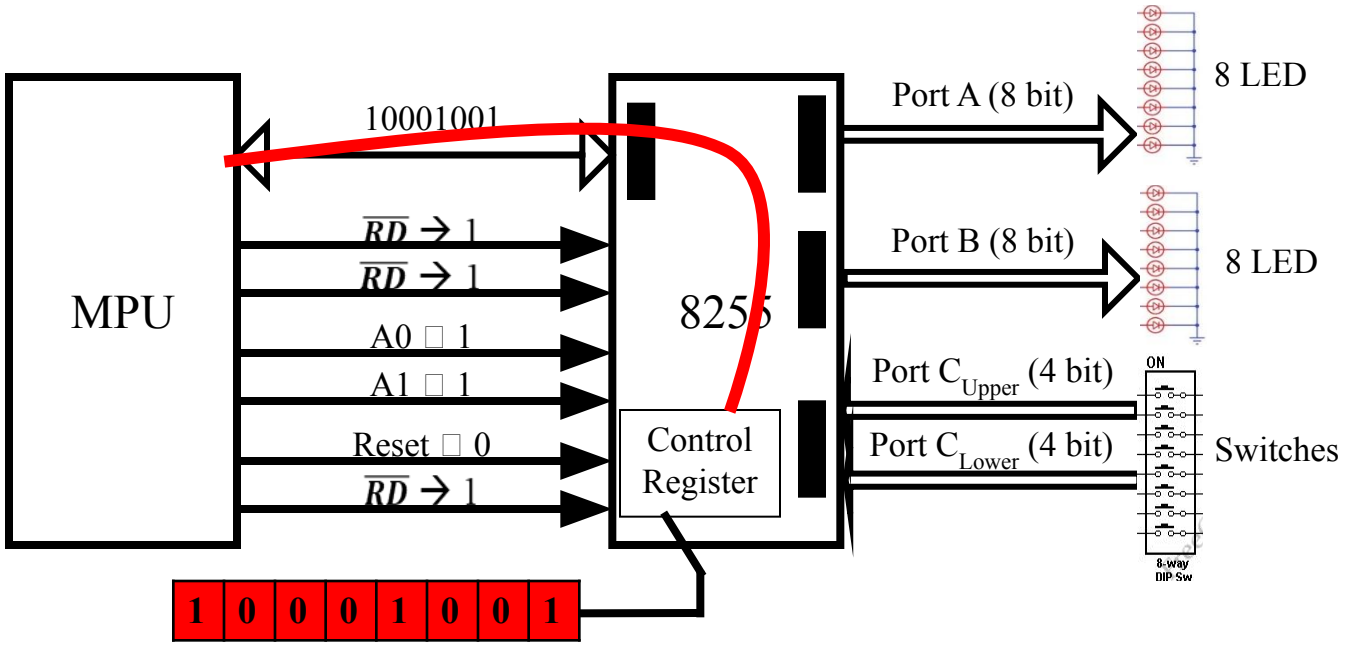
Following Table gives the basic operation,

A_1	A_0	$\overline{RD}$	$\overline{WR}$	$\overline{CS}$	Input operation
0	0	0	1	0	PORT A ⟶ Data bus
0	1	0	1	0	PORT B ⟶ Data bus
1	0	0	1	0	PORT C ⟶ Data bus
					Output operation
0	0	1	0	0	Data bus ⟶ PORT A
0	1	1	0	0	Data bus ⟶ PORT B
1	0	1	0	0	Data bus ⟶ PORT C
1	1	1	0	0	Data bus ⟶ control

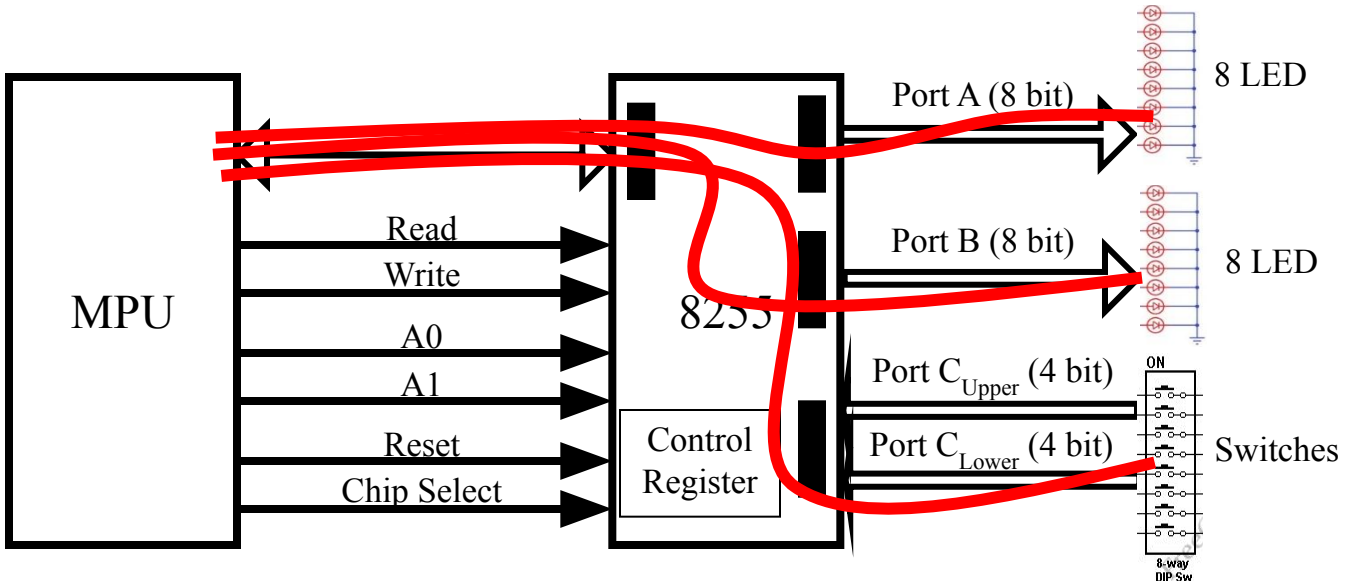
I/O Operation in Mode-0



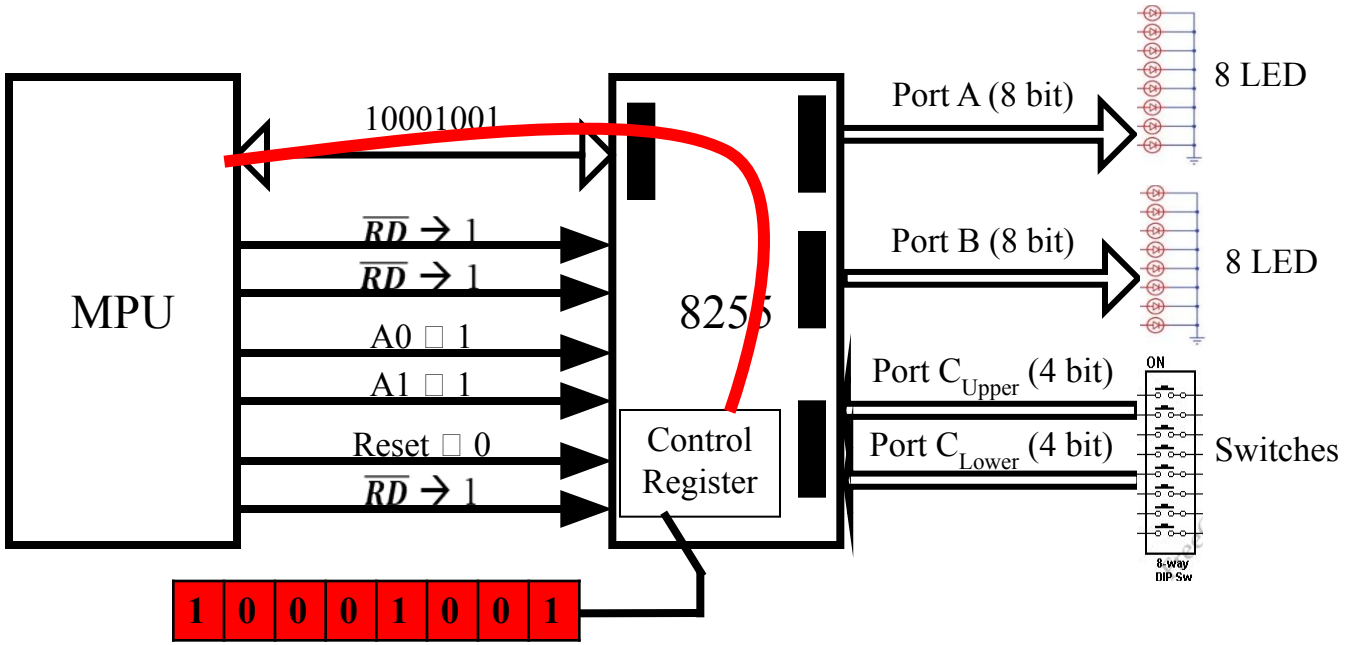
First write to the control register to configure



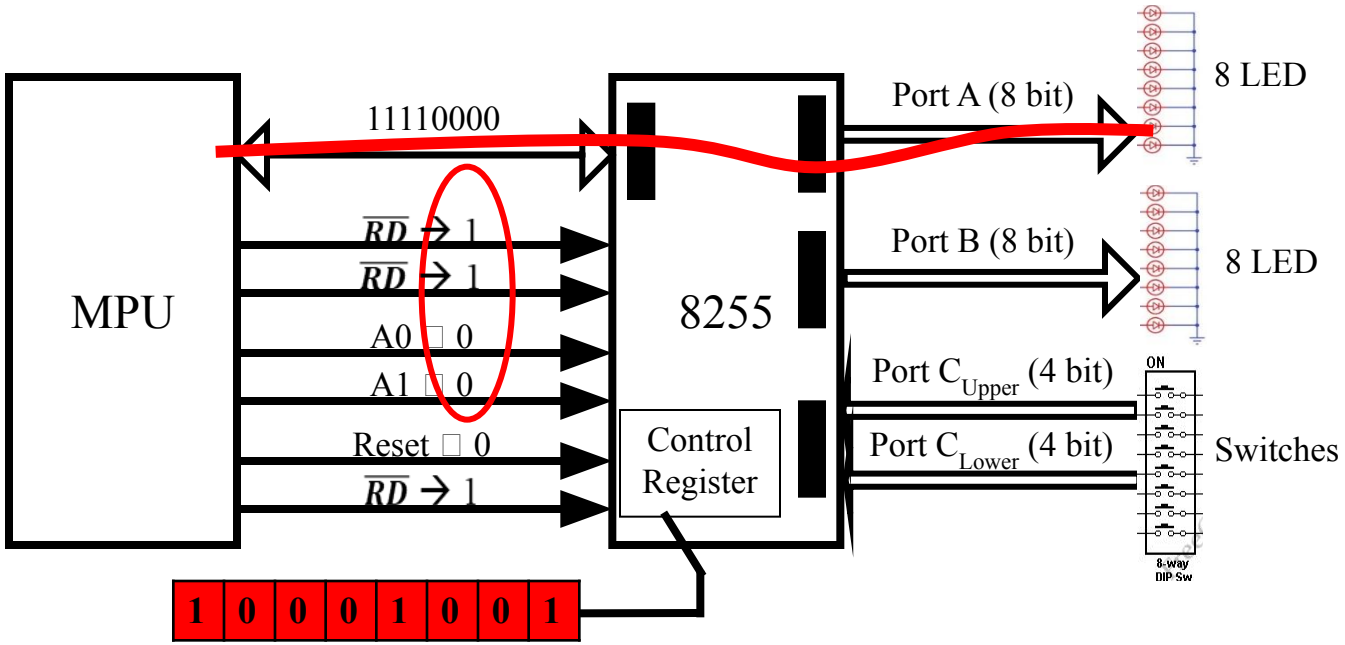
Then IO operation



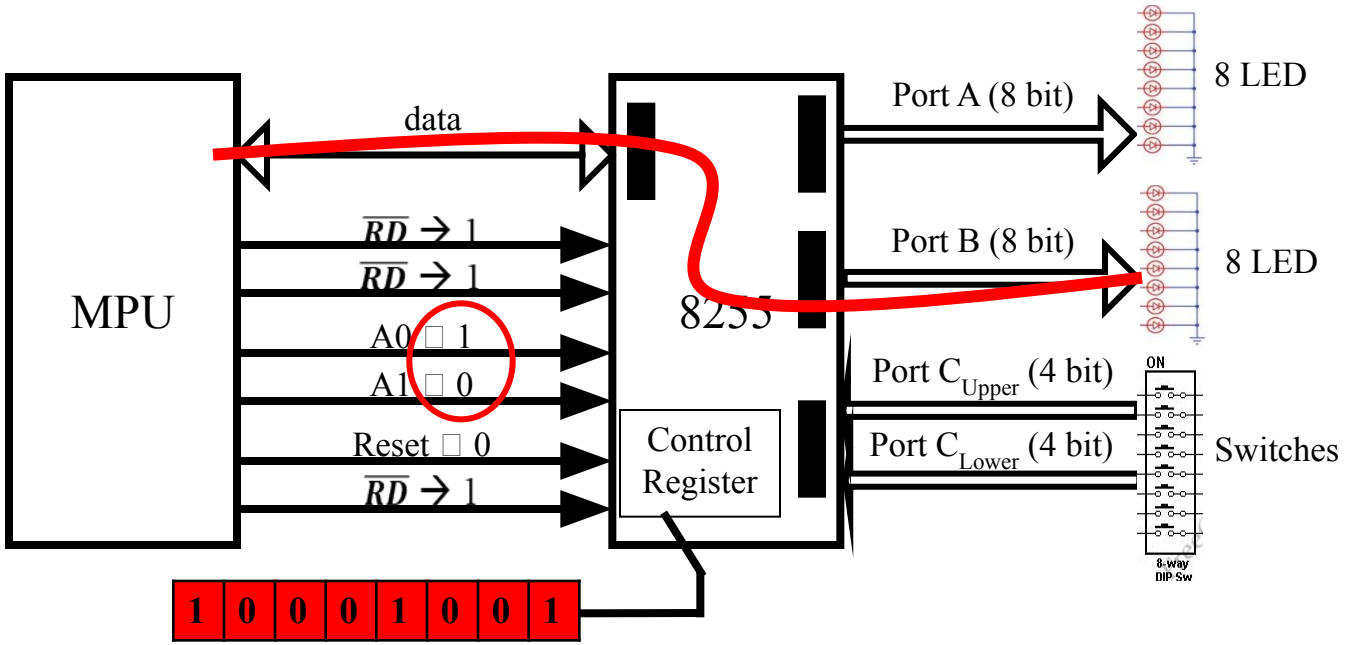
First write to the control register to configure



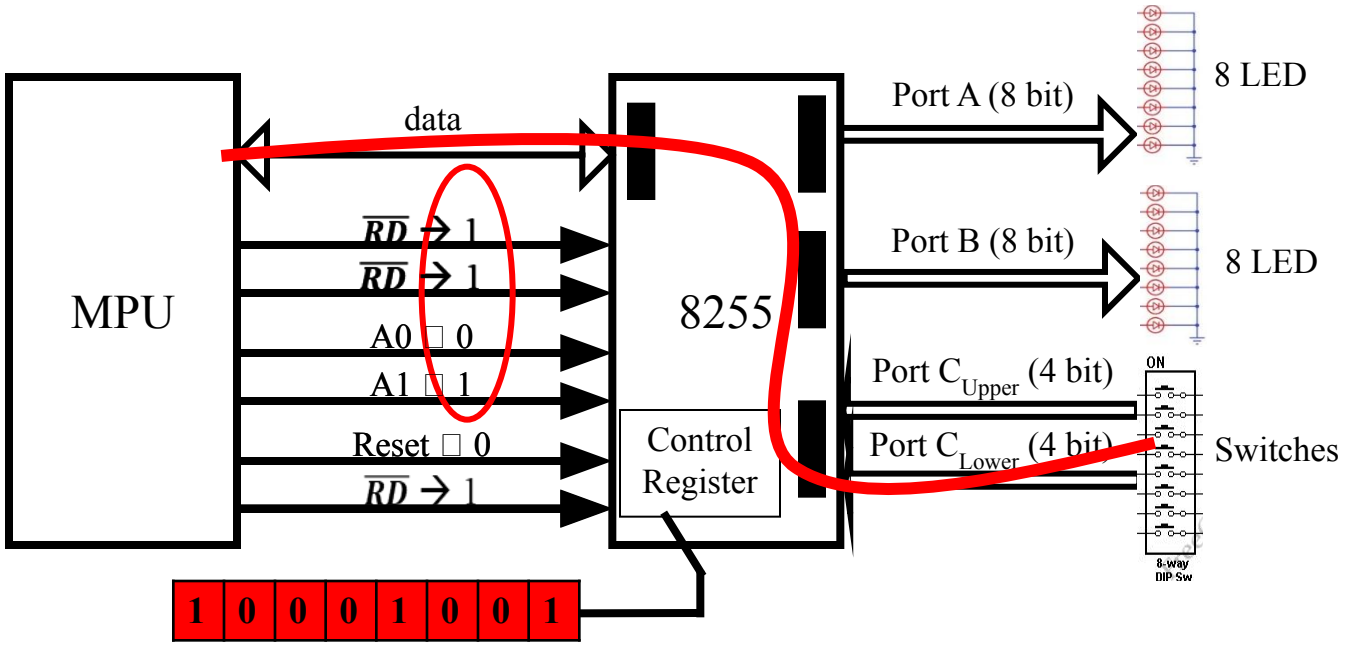
IO operation (in this cycle: MPU□Port A)



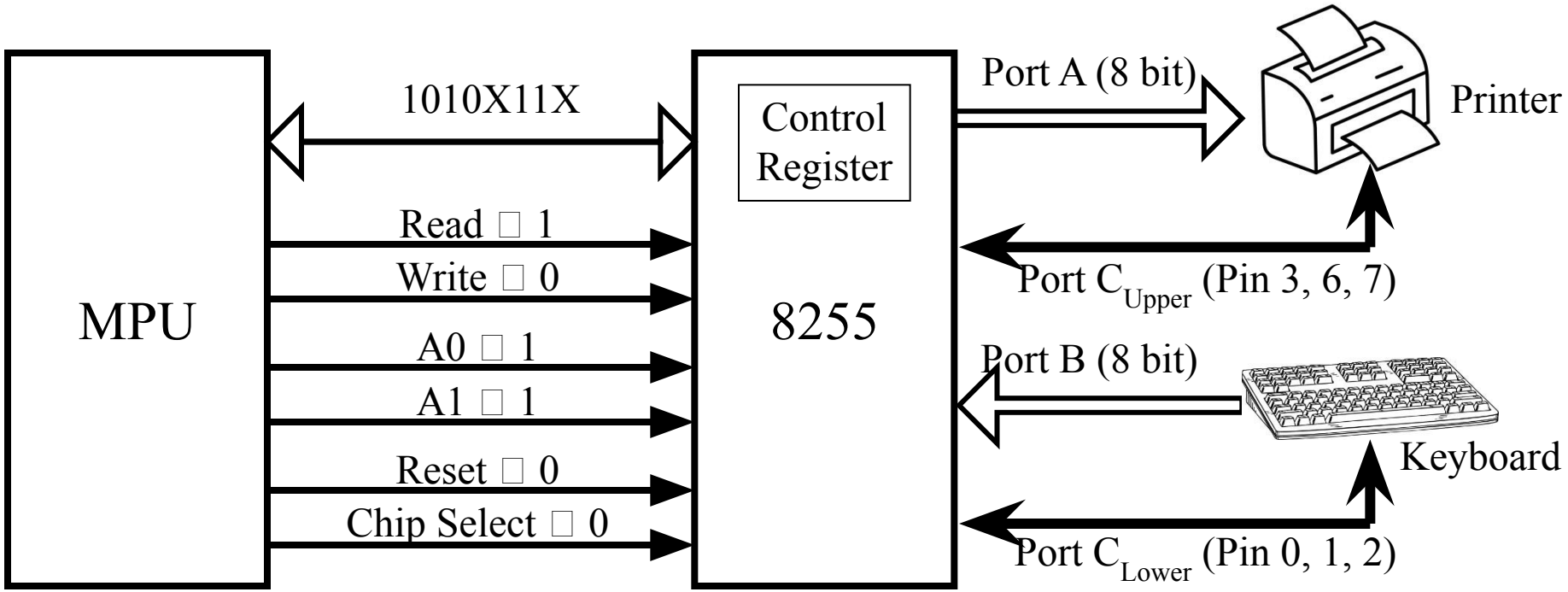
IO operation (in this cycle: MPU□Port B)



IO operation (in this cycle: Port C□MPU)



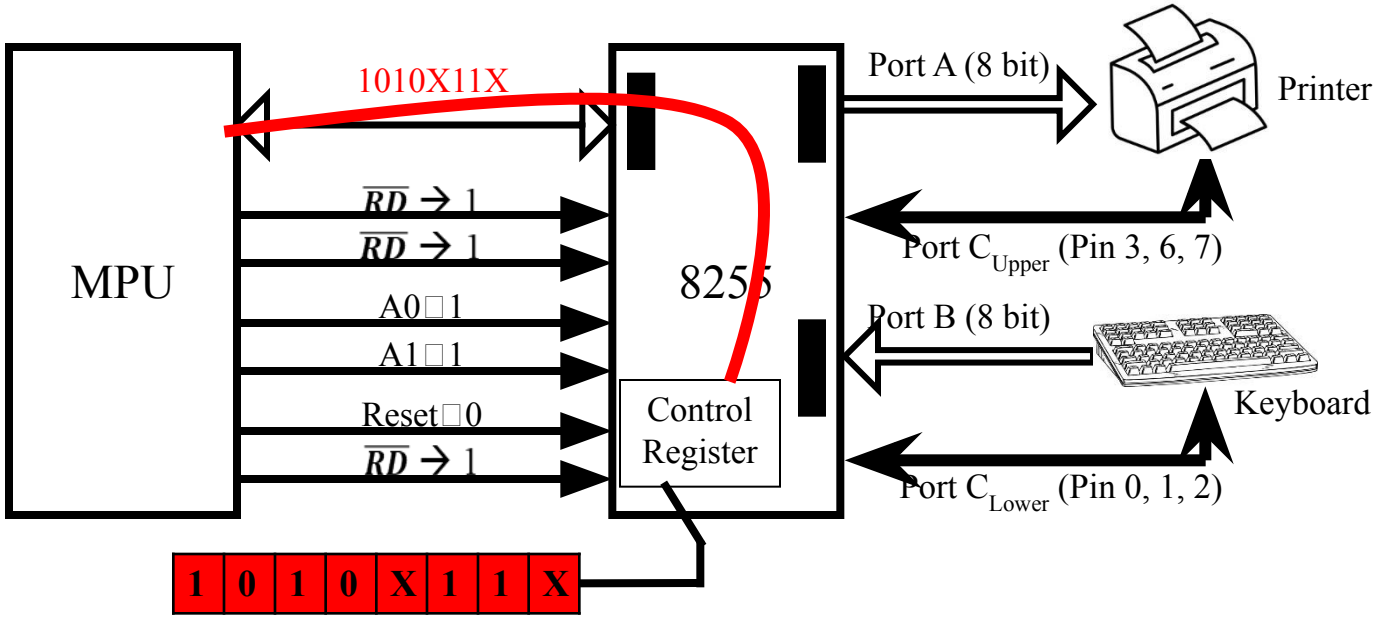
Writing to Control word for Mode-1



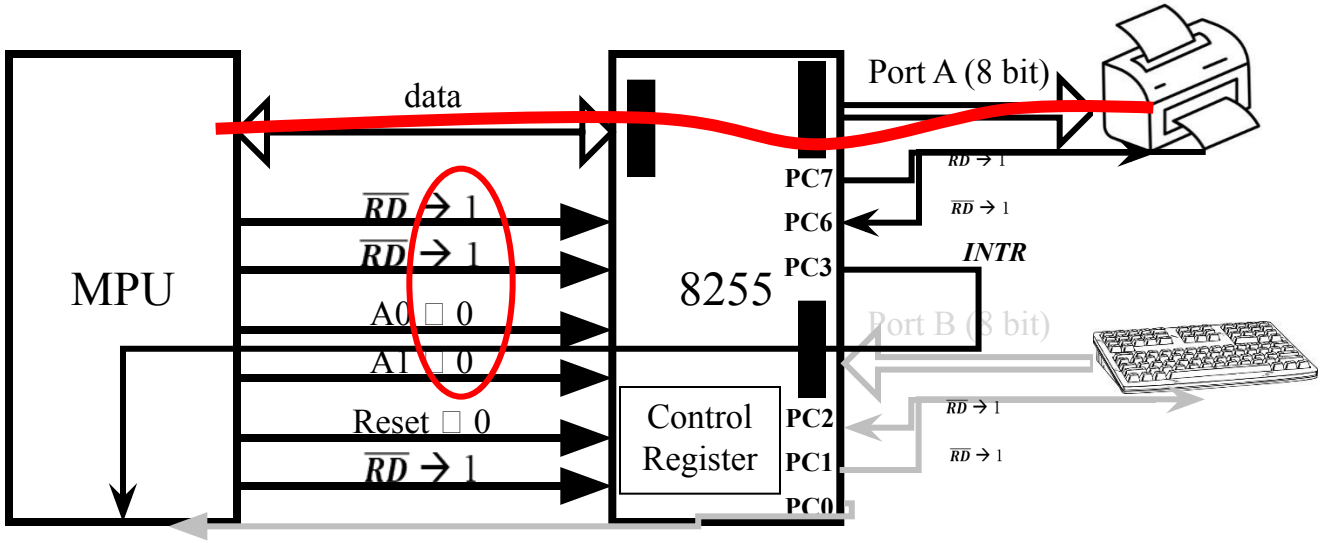
1	0	1	0	X	1	1	X

Control Register

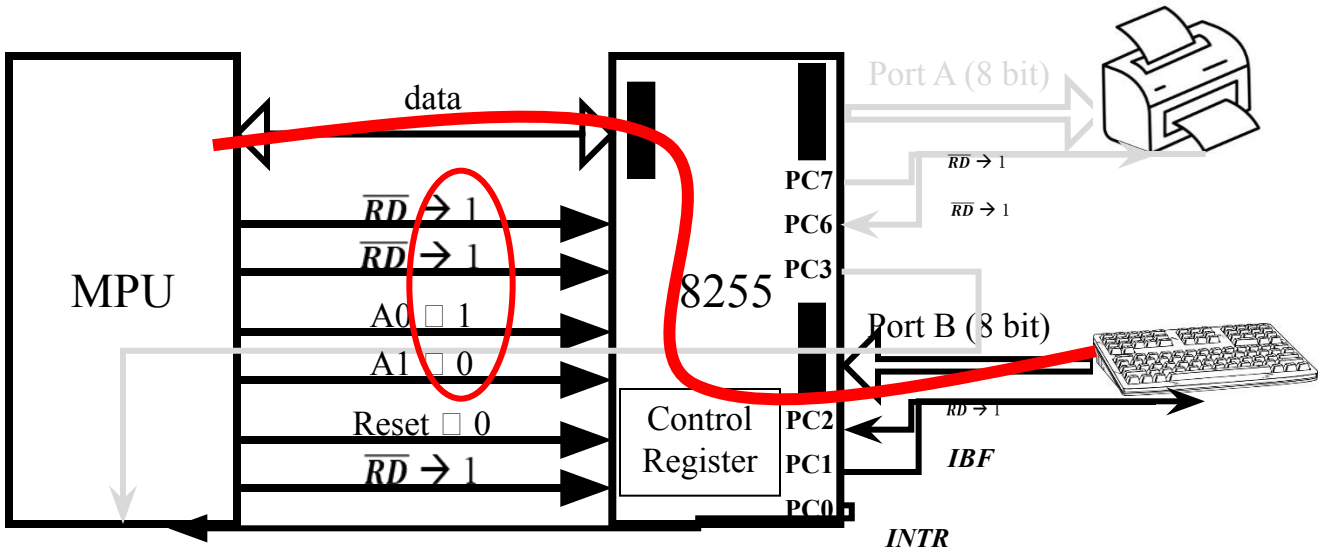
Write to the control register



Handshaking OUT operation with Port A

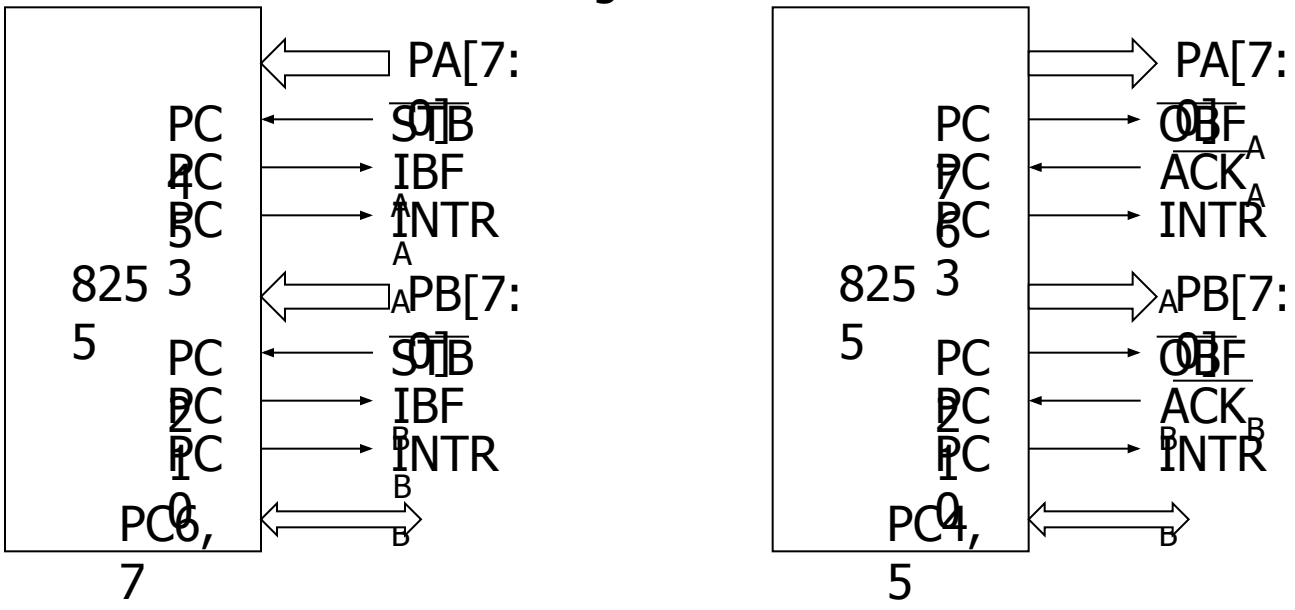


Handshaking IN operation with Port B



Programming 8255

- Mode 1:
  - — Ports A and B are programmed as input or output ports
  - — Port C is used for handshaking



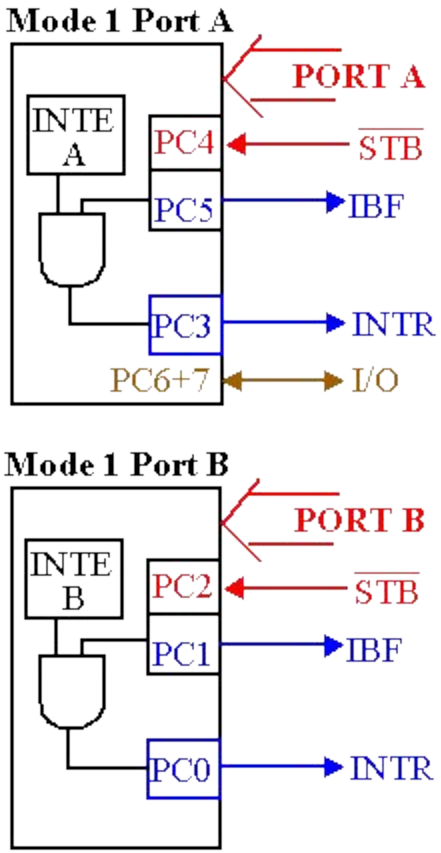
$\overline{\text{STB}}$ The strobe input loads data into the port latch on a 0-to-1 transition

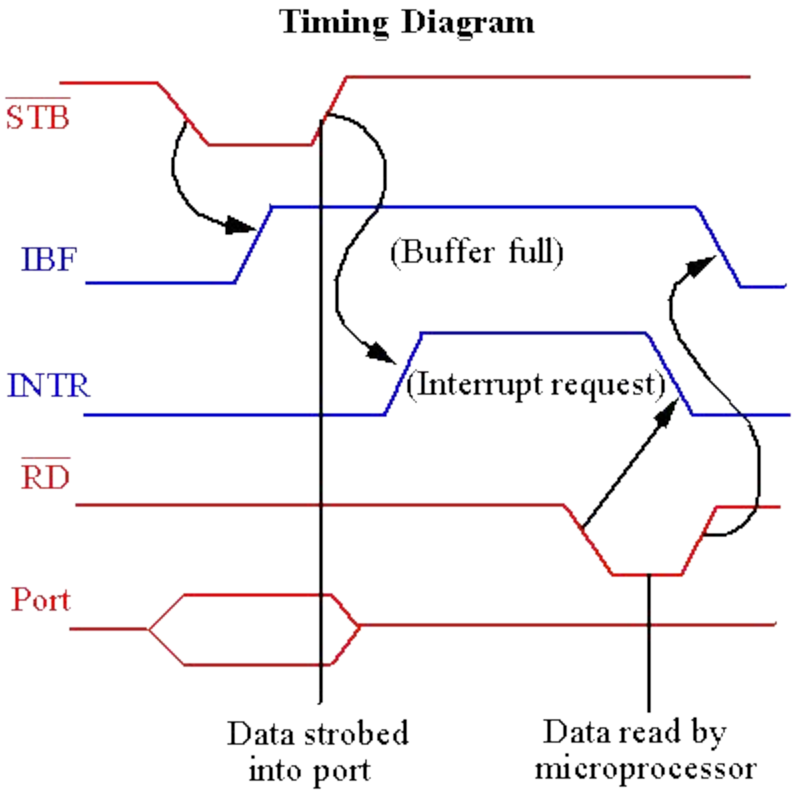
IFB **Input buffer full** is an output indicating that the input latch contain information

INTR **Interrupt request** is an output that requests an interrupt

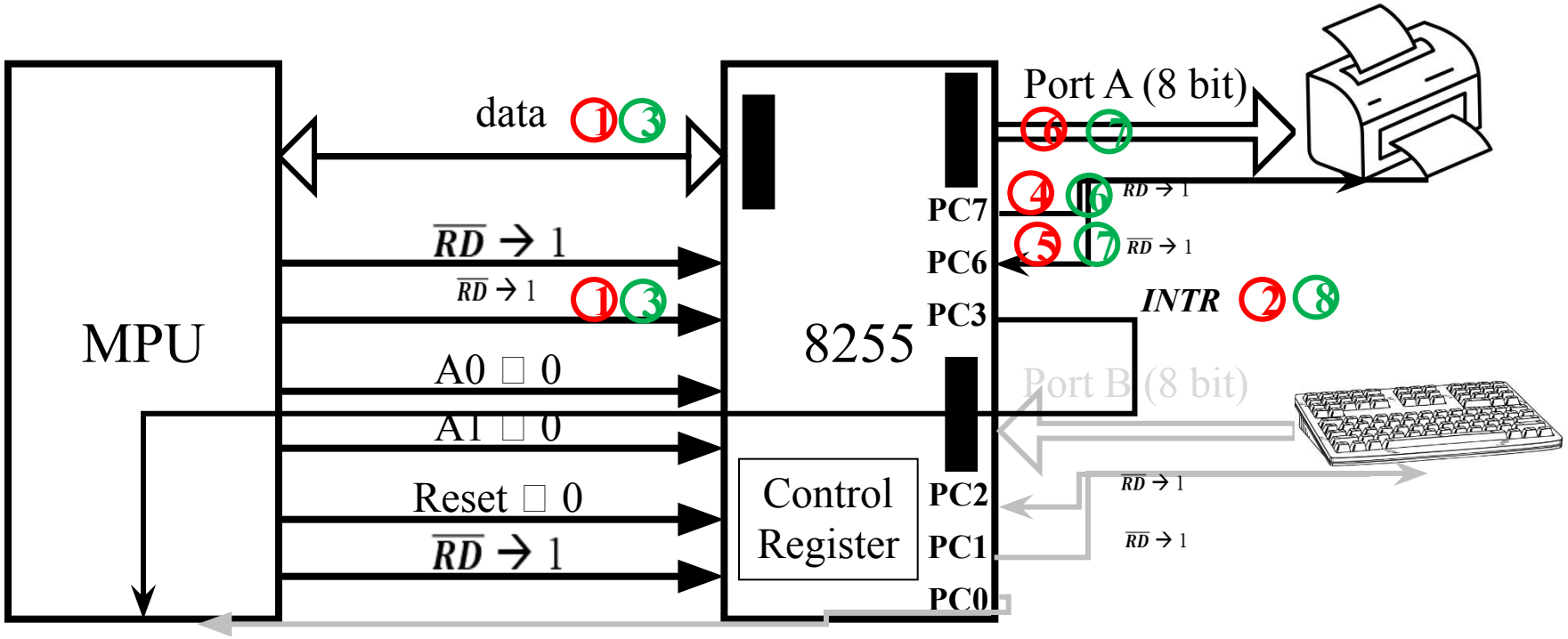
INTE The **interrupt enable signal** is neither an input nor an output; it is an internal bit programmed via the PC4(port A) or PC2(port B) bits.

PC7,PC6 The port C pins 7 and 6 are general-purpose I/O pins that are available for any purpose.





Handshaking out operation with Port A



$\overline{\text{OBF}}$ **Output buffer full** is an output that goes low when data is latched in either port A or port B. Goes low on $\overline{\text{ACK}}$.

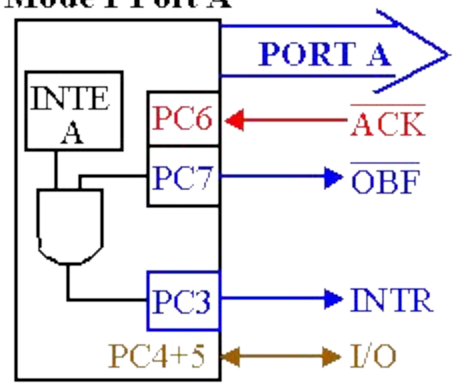
$\overline{\text{ACK}}$ The **acknowledge** signal causes the $\overline{\text{OBF}}$ pin to return to 0. This is a response from an external device.

INTR **Interrupt request** is an output that requests an interrupt

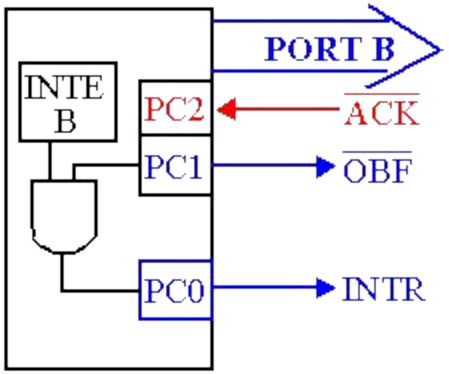
INTE The **interrupt enable signal** is neither an input nor an output; it is an internal bit programmed via the PC6(port A) or PC2(port B) bits.

PC5,PC4 The port C pins 5 and 4 are general-purpose I/O pins that are available for any purpose.

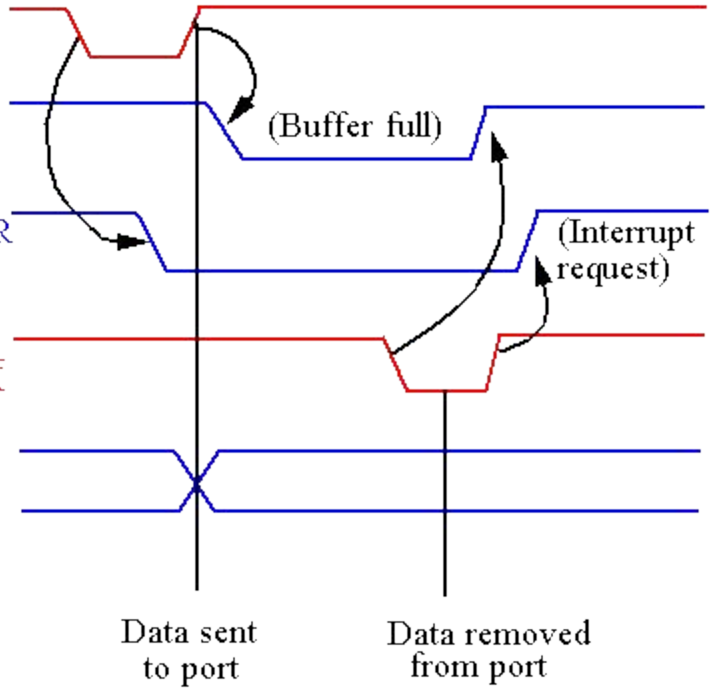
Mode 1 Port A



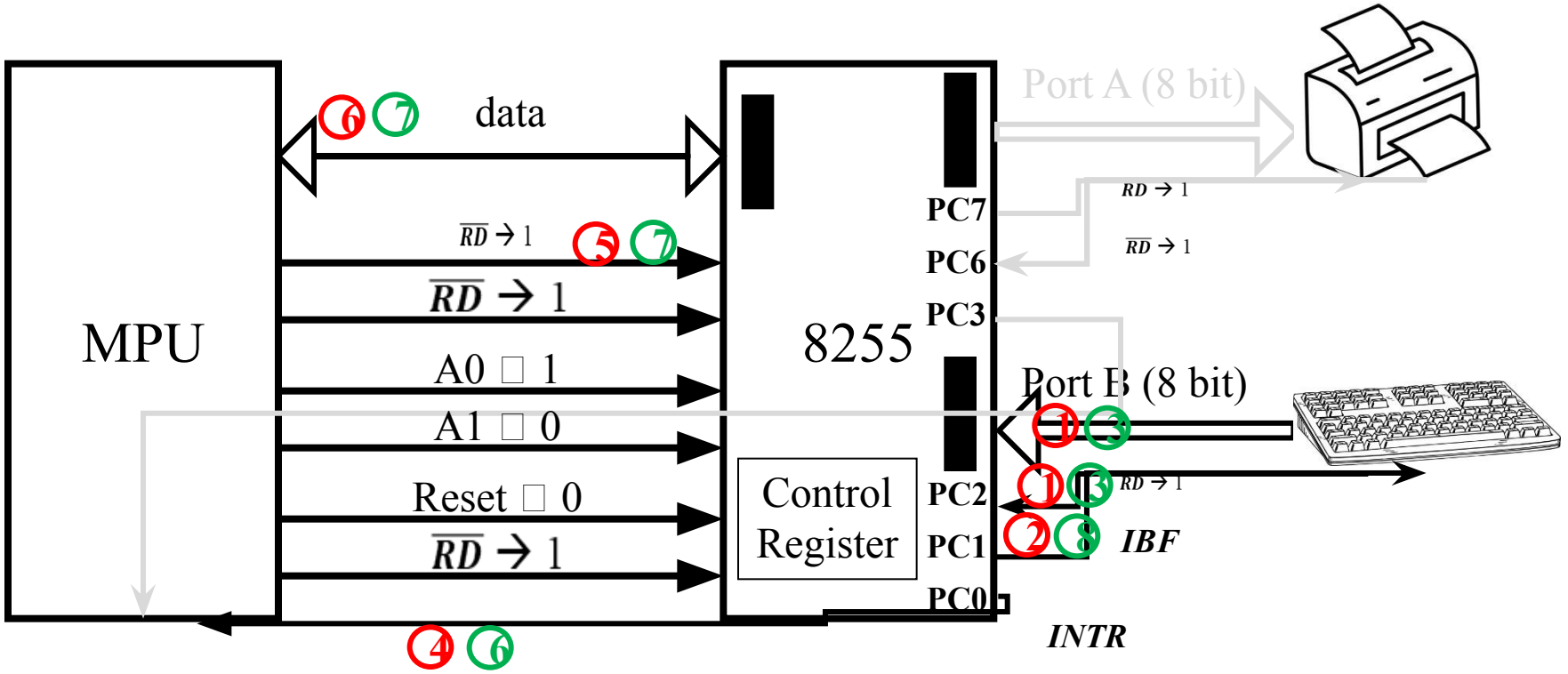
Mode 1 Port B



Timing Diagram

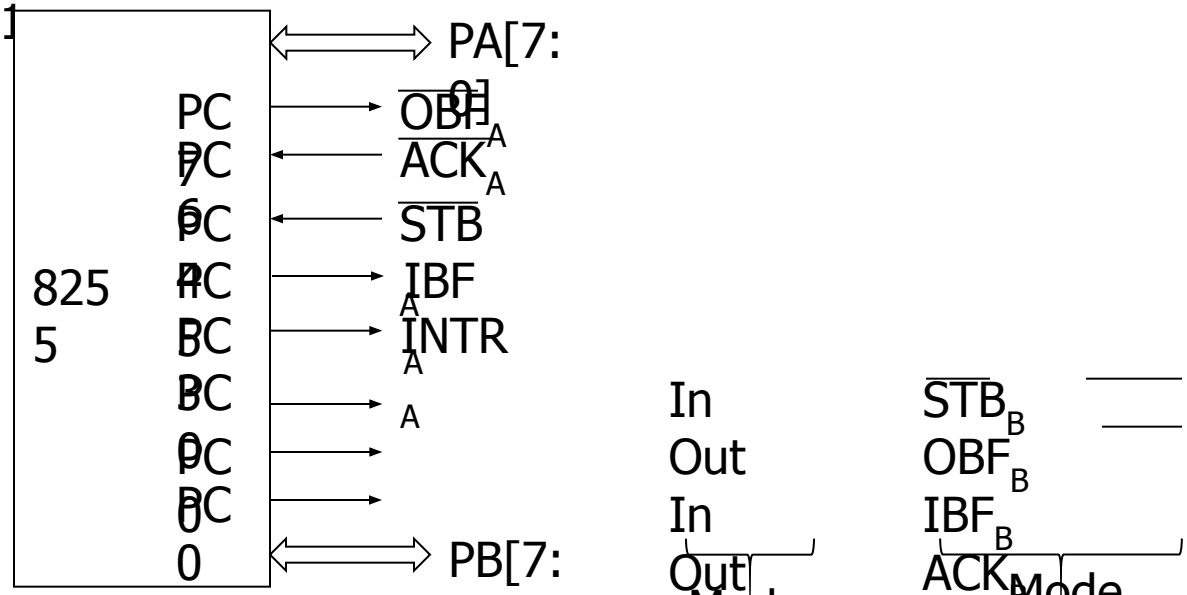


Handshaking in operation with Port B



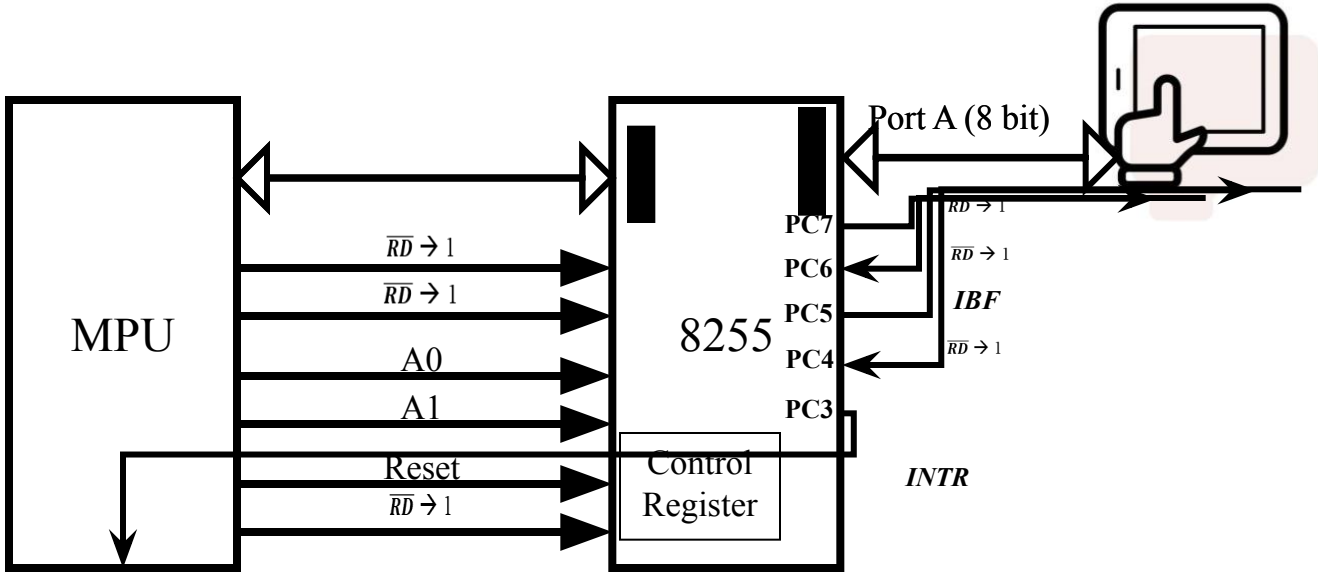
Mode-2

- Mode 2:
  - — Port A is programmed to be bi-directional
  - — Port C is for handshaking
  - — Port B can be either input or output in mode 0 or mode 1

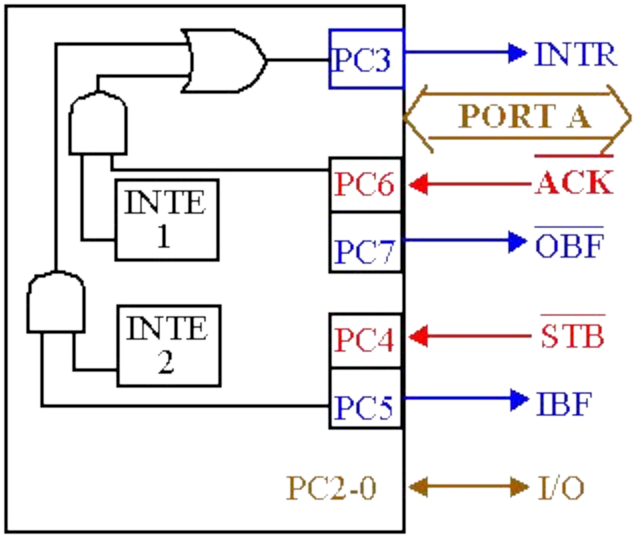


1. Can you design a decoder for an 8255 chip such that its base address is 40H?
2. Write the instructions that set 8255 into mode 0, port A as input, port B as output, PC0-PC3 as input, PC4-PC7 as output ?

Handshaking I/O operation

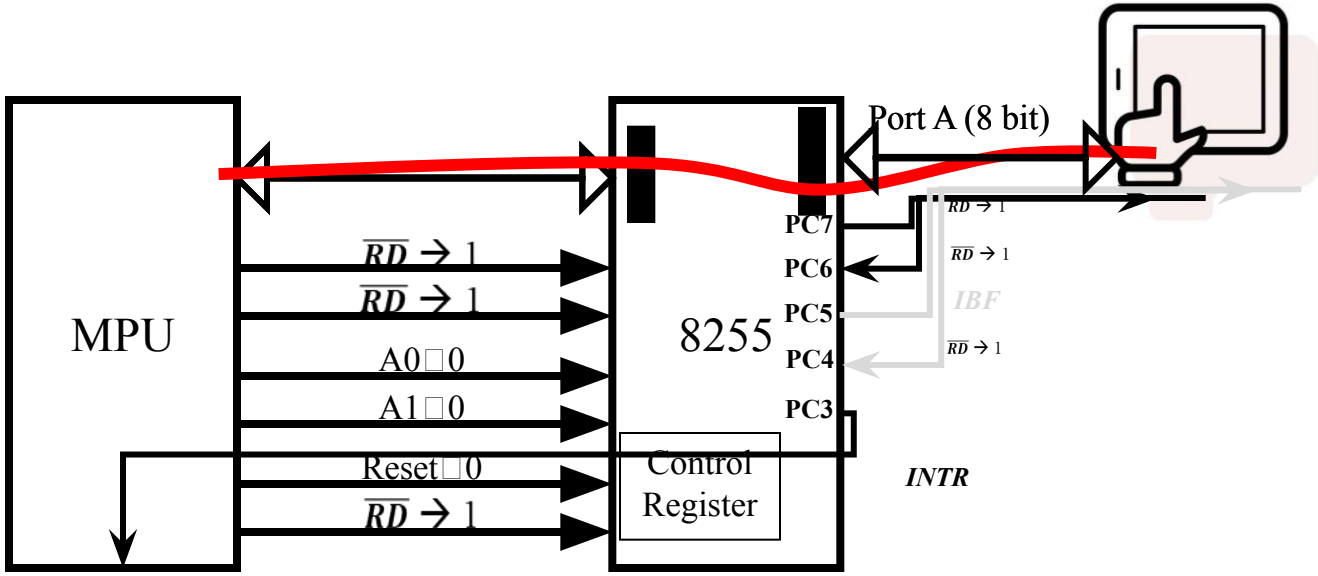


INTR	**Interrupt request** is an output that requests an interrupt
$\overline{\text{OBF}}$	**Output buffer full** is an output indicating that the output buffer contains data for the bi-directional bus
$\overline{\text{ACK}}$	**Acknowledge** is an input that enables tri-state buffers which are otherwise in their high-impedance state
$\overline{\text{STB}}$	The strobe input loads data into the port A latch
IFB	**Input buffer full** is an output indicating that the input latch contains information for the external bi-directional bus
INTE	**Interrupt enable** are internal bits that enable the INTR pin. Bit PC6(INTE1) and PC4(INTE2)
PC2,PC1 and PC0	Theses port C pins are general-purpose I/O pins that are available for any purpose.

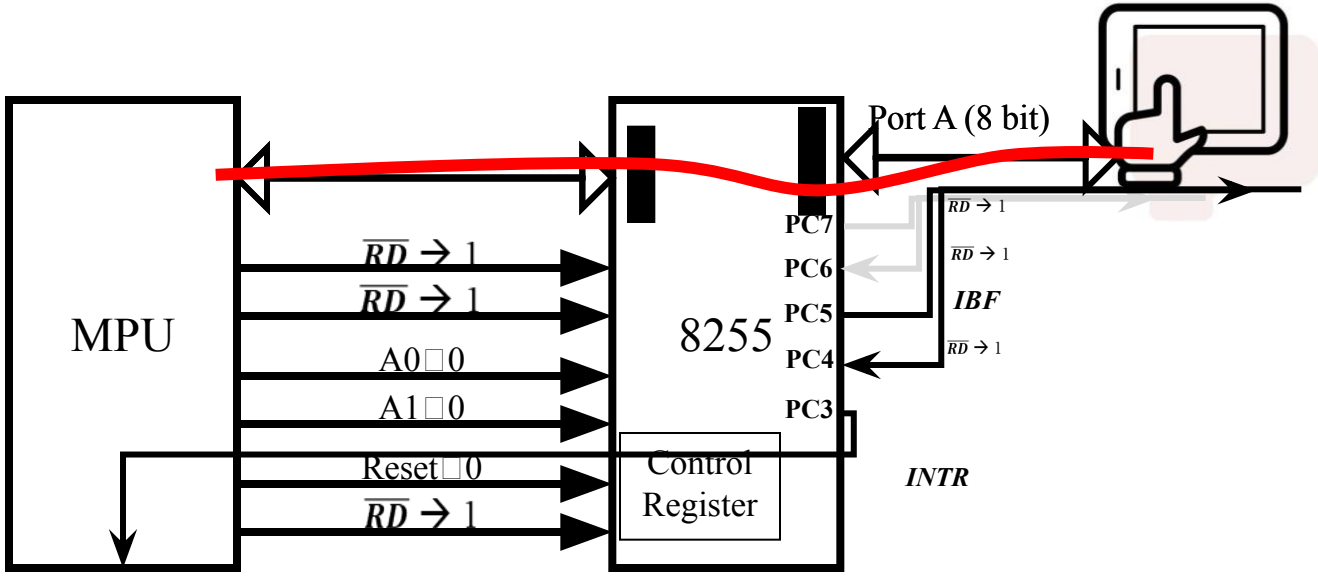


Timing diagram is a combination of the Mode 1 Strobed Input and Mode 1 Strobed Output Timing diagrams.

Handshaking I/O operation (OUT)



Handshaking I/O operation (IN)



Thank you

Q&A