Final Lab Assessment

CSE360: Computer Interfacing

Department of Computer Science and Engineering

Total Marks: 10

[Complete all the blanks and commands with necessary information in the given C type file. Also answer ALL 4 short questions.]

i) .C file **0.5 x 12 = 6**

[Port A pin 9 for SCL and pin 10 for SDA]

```
void I2C_Acknowledgement_Check()
{
    // Handle Acknowledge Failure
    if (I2C2->SR1 & (a)  (1<<10)  ) // I2C_SR1_AF
    {
        I2C2->SR1 (i)  &=~  (b)  (1<<10)  ; // Clear the AF flag
        I2C2->(j)  CR1  |= ((c)  1<<9  ); // Generate a stop
condition
    }
}

void I2C_Init()
{
   // Enabling Clock for I2C2
   RCC->APB1ENR |= ((d)  1<<22  )); // RCC_APB1ENR_I2C2EN

   // Reset I2C2
   I2C2->CR1 |= ((e)  1<<15  ); // I2C_CR1_SWRST
   I2C2->CR1 &= ~((f)  1<<15  ); // Clear the SWRST bit

   I2C2->CCR |= ((g)  1<<15  ); // Setting F/S bit for Fast Mode

   I2C2->CR2 =(h)  32<<0  ; // Set APB1 clock frequency in  32 MHz
```

```
    I2C2->CCR =27;
    I2C2->TRISE =11;
}
void check_I2C2_mode(void)
{
    // Check if I2C is in master mode or slave mode (observe SR2
register)
    if (I2C2->(k)__SR2__ & ((l)__1<<0__))
   {
      printf("I2C2 is in Master mode”);
   }
    else
    {
        printf("I2C2 is in Slave mode");
    }
}
```

ii) Short Questions

1 x 4 = 4

a) Why is CCR value needed for I2C communication? What is its significance ?

Ans: The CCR value is needed for generating the high and low level of SCL clock which determines the period, and the frequency of the SCL. This frequency is later used in synchronizing the internal APB clock of the microcontroller by using this CCR value. When the slave stretches the SCL line, the SCL input checks the data passed via the data bus from the peripheral devices after raising the edge generation. This edge generation is achieved by CCR value.

b) What is the significance of TRISE value ? What can happen if an incorrect TRISE value is set ?

Ans: The TRISE value helps in rising edge generation by providing enough time for SCL feedback loop which in turn provides consistent SCL clock frequency. This value also helps in slave stretching tolerance where the master can tolerate the slave stretching when the slave delays the acknowledgement on receiving a specific byte.

An incorrect TRISE value results in unstable SCL clock frequency which provides incorrect data communications and corruption in the data. If the TRISE value is not set at a value which is greater than or equal to the time taken by the slave to stretch, then the master will not be able to tolerate slave

stretching, which can cause failures in communication.

c) What is the role of the CR2 register in I2C2 communication?

Ans: The roles of CR2 register in I2C2 include - checking packet error by PECBYTE, setting automatic end mode for master by AUTOEND, Nbytes reload mode by RELOAD,, number of bytes transmitted/ received in the program by NBYTES[7:0], generating NACK for slave by NACK, generating stop condition for master mode by STOP, generating start condition by START, storing 10 bit of slave address in read sequence by HEAD10R, assigning 10 bit addressing mode for master by ADD10, setting write transfer or read transfer for the master by RD_WRN and setting which slave address will be sent by SADD[9:0.

d) Why is the STOPF flag cleared before activating acknowledgement ? Explain

Ans: STOPF checks for a stop condition before it delivers an acknowledgement as a response to the data received by it. If the STOPF flag is not cleared before activating acknowledgment, then there will be a delay in detection of the stop condition in the data and delivery of acknowledgement. Also, if there is any acknowledgement present in the uncleared STOPF flag, then it will work as another stop condition resulting in the transmission of multiple acknowledgements by mistake.