CSE360 Assignment

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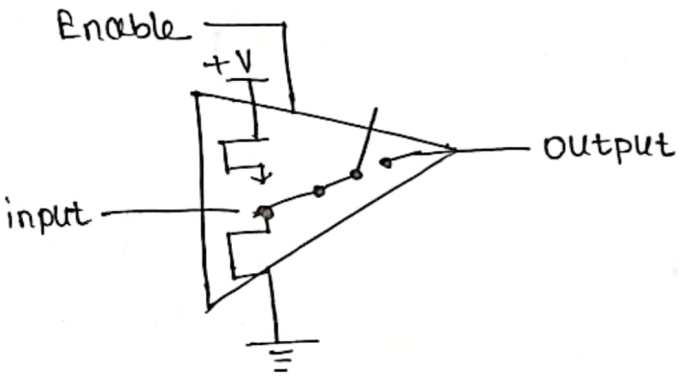
SECTION: 05

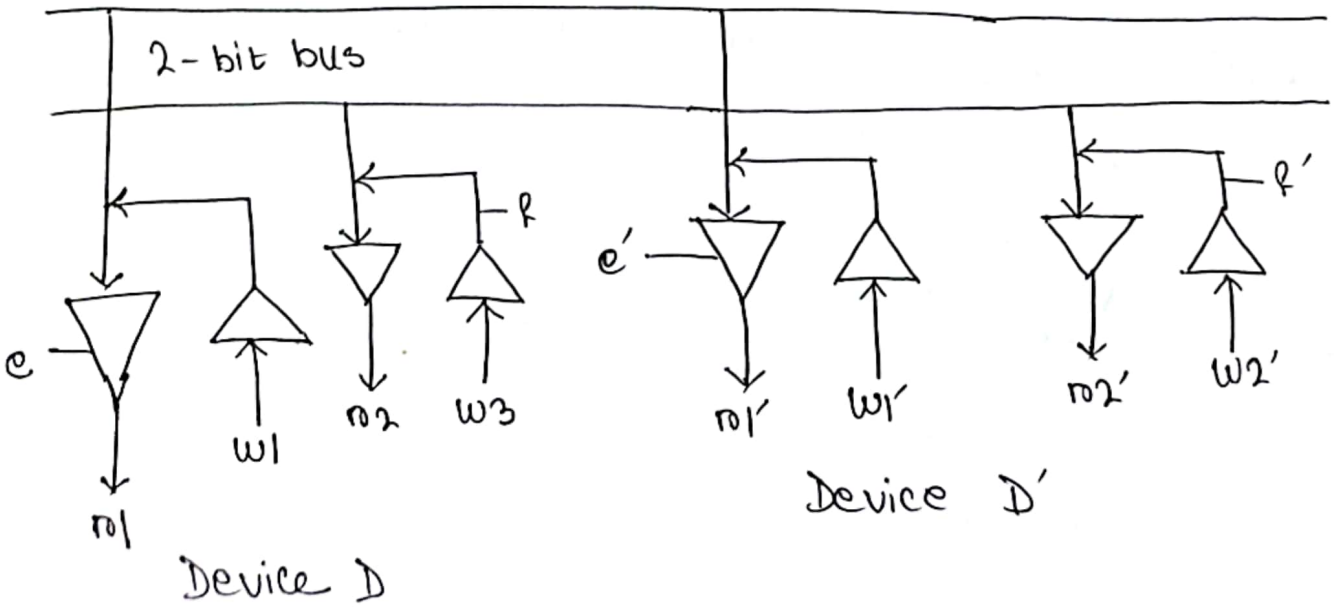
PROBLEM 1

(a) A tri-state is a logic circuit which has an output of 3 states: zero, open or high-impedence. (High - Z)

enable	input	output
0	x	Z
1	0	0
1	1	1



When output = Z, tri state is in High - Z state, which removes the device influence on the rest of the circuit. Only one device can access tri-state at a time.



① D is writing to D'
$e = 0, f = 1, e' = 1, f' = 0$

② D' is writing to D
$e = 1, f = 0, e' = 0, f' = 1$

③ $e = f = 0 \rightarrow$ D is tri-stated
D is disconnected from bus.

(b) When more than 1 device wants to access the data bus at the same time for output, then bus conflict/bus errors occur.

Causes of bus error/conflict:

(1) Caused by multiple device using the bus as output.

(2) Wait states are not maintained.

(3) If an I/O device causes the bus pin to stuck at 1 or 0.

(4) Caused by glitch.

4) USB type-C is most widely used because:

(1) It is reversible.

(2) Has high speed power delivery

(3) High speed data transfer

(4) Is slim, compact and symmetrical in size and shape.

Examples include all latest laptops, smartphones and tablets.

(d) The comparisons between serial and parallel transmission are as follows:-

Serial	Parallel
(1) Uses a single communication line to transit data bit-by-bit in a sequence.	(1) Uses multiple communication lines to transmit data, usually 8-bit) at a time.
2) Is slower	(2) Is faster
3) Efficient for long distance data transfer	(3) Not efficient for long distance data transfer

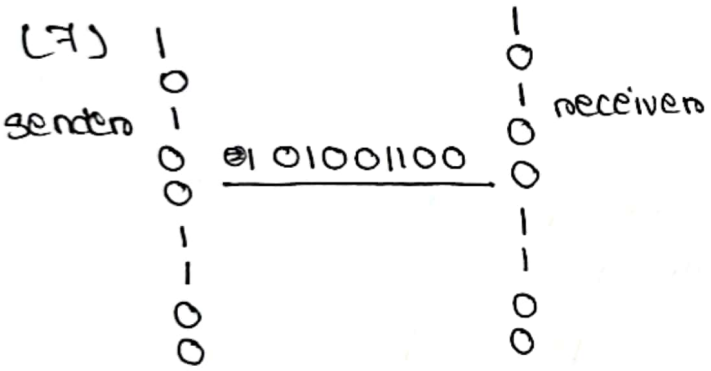
Serial

(4) Provides high security during data transfer.

(5) No data loss occurs.

(6) Data buffers are required.

(7)



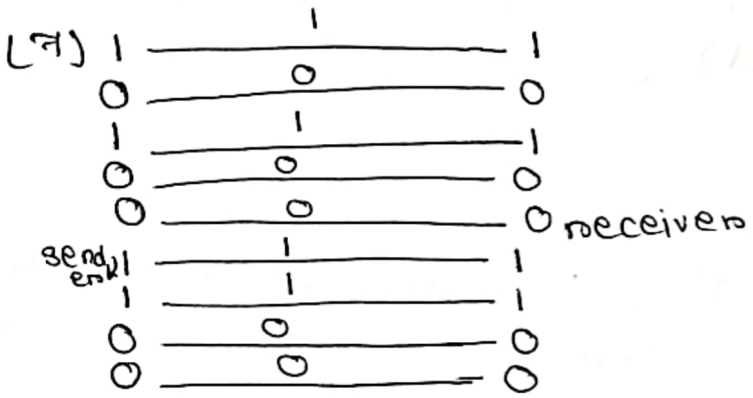
Parallel

(4) Provides no security during data transfer.

(5) Data loss occurs.

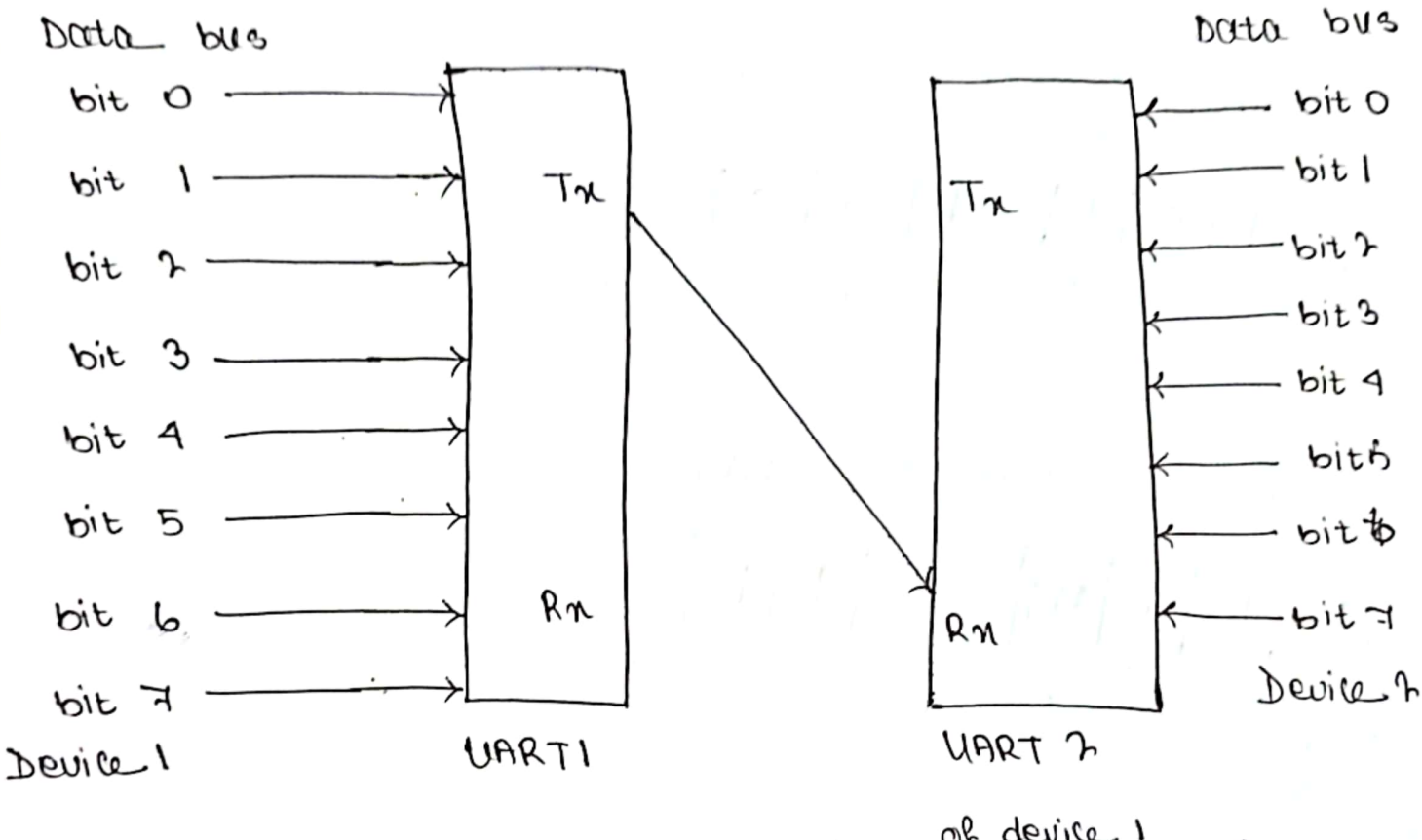
(6) No data buffers are required.

(7)



PROBLEM 2

(a) The second protocol used is UART (Universal Asynchronous Receiver/Transmitter



(1) 8 bit data from the data bus of device 1 is transferred into UART 1 where the parallel data is converted into parallel.

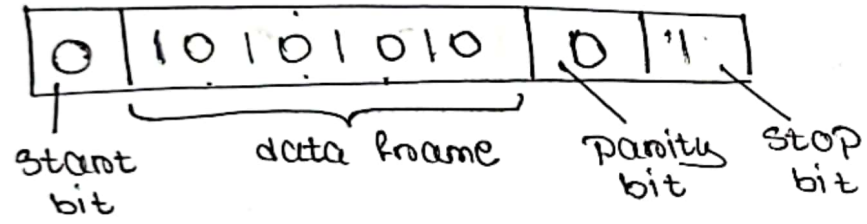
(2) Start bit and stop bit are added to the data frame by UART 1.

(3) This packet is passed to the Rx pin of UART 2 from Tx pin of UART 1.

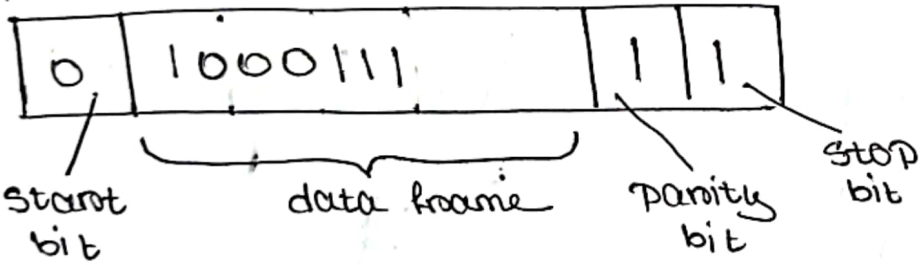
(A) Start and stop bits are removed in UART 2.

(B) The transferred serial data is converted again in parallel and passed via data bus to device 2

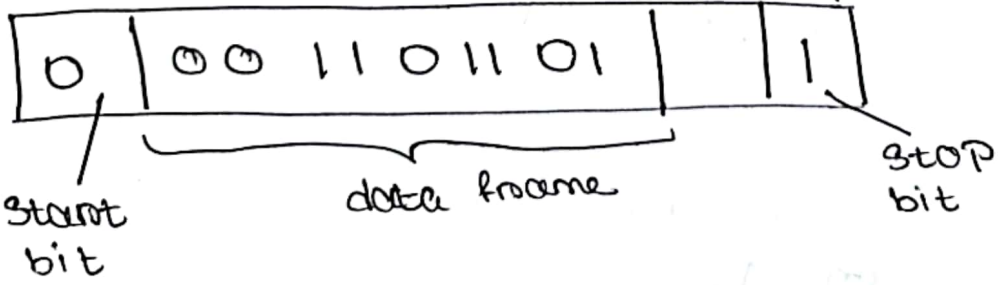
(b) 1st data packet (10101010)



2nd data packet (10001111)



3rd data packet (0011011101)



(c) Comparisons between I2C and UART are :

I2C	UART
(1) Has synchronous transmission.	(1) Has asynchronous
(2) Full duplex	(2) Half duplex
(3) Fasten	(3) Slower
(4) No master slave	(4) Multiple masters and slaves
(5) Can connect up to $2^{7/10}$ devices	(5) Can connect up to 2 devices.
(6) 2 pins — Tx, Rx	(6) 2 pins — SDA, SCL

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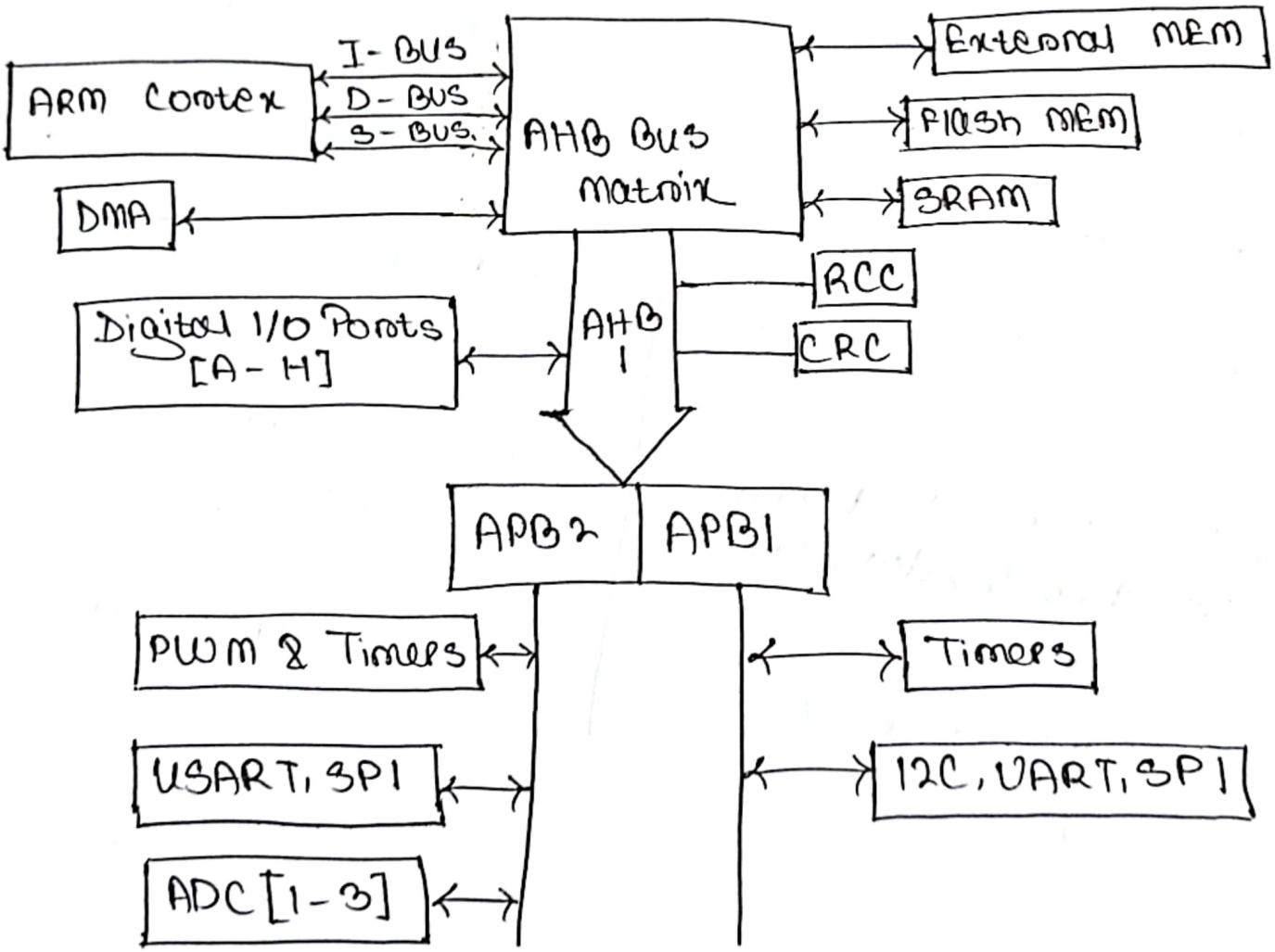
PROBLEM 3

(a) Simplied system architecture of STM32 MC



(b) The registers that are required for the GPIO operations in STM32 are:

(1) Configuration registers
- GPIOx_MODER, GPIOx_OTYPER, GPIOx_OSPEEDR, GPIOx_PUPDR

(2) Data registers
- GPIOx_IDR, GPIOx_ODR

(3) Set/Reset register
- GPIOx_BSRR

(4) Locking register
- GPIOx_LCKR

(5) Alternate function selection
- GPIOx_AFRH, GPIOx_AFRL

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(c) (i) Activate the port C of STM32

RCC → AHBIENR |= 1<<3

(ii) Pin 7 of port C will be used

I/O direction mode = output

GPIOC → MODER |= 1<<14

I/O output speed = high speed

GPIOC → OSPEED |= 3<<14

Output Type of I/O port = open drain

GPIOC → OTYPER |= 1<<7

(iii) Pin 9 of port C will be used

I/O direction mode = input

GPIOC → MODER |= 0<<18

I/O pull up or pull down = pull up

GPIOC → PUPDR |= 0<<18

(a) RCC → AHBIEN |= 1<<3

7	6	5	4	3	2	1	0
0	0	0	0	1	0	0	0

→ (I)

RCC → AHBIEN &= ~(0<<5)

7	6	5	4	3	2	1	0
0	0	1	1	1	1	1	1

→ (II)

(I) AND (II).

RCC → AHBIEN |= (1<<1) |= (1<<0)

7	6	5	4	3	2	1	0
0	0	0	0	0	0	1	1

→ (III)

((I) AND (II)) OR (III)

```
0 0 0 0 1 0 0 0   } (I) AND (II)
0 0 0 1 1 1 1 1   }
-----------------
0 0 0 0 1 0 0 0   } ((I) AND (II)) OR (III)
0 0 0 0 0 0 1 1   }
-----------------
0 0 0 0 1 0 1 1
H G F E D C B A
      ✓   ✓ ✓
```

Activated ports → A, B, D