Course Details

Course Name:	**Digital Design**	**Course Code:**			**ECSE104L**
Department :	**CSE**	**Type:**			• Core
L-T-P Structure	**3-1-2**	**Credits**	**5**	**Pre-requisite:**	**None**
Course Objectives	***Main Objectives of the course are:*** Explain the elements of digital system abstractions such as digital representations of information, digital logic, Boolean algebra, state elements and finite state machine (FSMs). Design simple digital systems based on these digital abstractions, using the "digital paradigm" including discrete sampled information. Use the "tools of the trade": basic instruments, devices and design tools.				
Course Outcome	At the end of the course students will be able to: 1. Understand how analog signals are used to represent digital values in different logic families, including characterization of the noise margins. 2. Create the appropriate truth table and gate level implementation from a description of a combinational logic function. 3. Draw a circuit diagram for a sequential logic circuit and analyze its timing properties (input setup and hold times, minimum clock period, output propagation delays) and implement a substantial digital system on an FPGA.				

Course Contents :	**Topics**	**No. of Hours**
	Digital Systems; Data representation and coding; Logic circuits, integrated circuits; Analysis, design and implementation of digital systems; Introduction of CAD tools. Number system; Representation of signed numbers;	3
	Fixed and floating-point numbers; BCD; Gray codes; parity check codes and Hamming code; Definition and specification; Truth table; Basic logic operation and logic gates.	3
	Basic Boolean algebra; Standard representation and simplification of logic functions - K-map and tabular methods.	3
	Decoders, encoders, multiplexers, demultiplexers and their applications; Parity circuits and comparators;	3
	Arithmetic modules- adders, CLA, multiplier, subtractors ALU Design examples.	3

	Definition of state machines, state machine as a sequential controller; Basic sequential circuits- latches and flip-flops: SR-latch, D-latch, Edge trigger and level trigger	3
	D flip-flop, JK flip-flop, T flip-flop; Timing hazards and races; Analysis of state machines using D flip-flops and JK flip-flops;	3
	Multi-bit latches and registers, counters, shift register, application examples.	3
	Design of state machines - state table, state assignment, transition/excitation table, excitation maps and equations, logic realization;	3
	Read-only memory, PROM, read/write memory - SRAM and DRAM	3
	PLAs, PALs and their applications; Sequential PLDs and their applications;	3
	Designing state machine using ASM charts; Designing state machine using state diagram;	3
	Design examples State-machine design with sequential PLDs;	3
	Introduction to different logic families; TTL inverter - circuit description and operation; CMOS inverter - circuit description and operation; propagation delay, transition time, power consumption and power-delay product.	3
Lab Instructions	In this course students will start with basic digital components such as Arithmetic and logical operation, Memory etc. Then finally design soft IP. The Lab will use Altera Quartus prime Lite tool for design and FPGA Altera DEII utilize for physical implementation.	
Text Book:	Digital Design: with an Introduction to the Verilog HDL – 2014 by M. Morris Mano	
References:	Digital Design and Computer Architecture, 2nd ed.," by D. M. Harris and S. L. Harris (Morgan Kaufmann, 2012). Verilog HDL: A Guide to Digital Design and Synthesis, 2nd ed.," by S. Palnitkar (Prentice Hall, 2003)	

Evaluation Components

Components of Course Evaluation	Percentage
Minor-1 Examination	**20%**
Assignment	**10%**
Quiz	**10%**
End-term Examination	**30%**
Laboratory Evaluation	**30%**