

PROJECT REPORT

SYNTHESIS OF SIGMOID FUNCTION USING PIECEWISE NONLINEAR APPROXIMATION

INDIAN INSTITUTE OF INFORMATION TECHNOLOGY ALLAHABAD



PROJECT MENTOR:

Dr. Prasanna Kumar Misra

GROUP MEMBERS:

- | | |
|------------------|------------|
| 1. VIVEK RAJ | IEC2017002 |
| 2. RITIK RANJAN | IEC2017005 |
| 3. ANIKET DUKARE | IEC2017058 |

ABSTRACT —

Efficient implementation of the activation function is important in the hardware design of artificial neural networks. Sigmoid are the most widely used activation functions for this purpose. There are various methods to implement this function. But some of them require huge area due to the use of multipliers and dividers. So in this report, we present a simple and efficient architecture that avoid the use of multipliers and dividers on implementing this function on hardware.

Index terms —

Sigmoid function, Hardware implementation.

INTRODUCTION

The sigmoid function is a non linear curve with an "S" shape. The main reason why we use sigmoid function is because it exists between (0 to 1). Therefore, it is especially used for models where we have to predict the probability as an output. Since probability of anything exists only between the range of 0 and 1, sigmoid is the right choice.

So it is used as an activation function in artificial neural networks. An activation function is used at the output of every neuron. Other activation functions are available today including the sigmoid, hyperbolic tangent (tanh), and step functions.

Some of the ways of implementing the sigmoid function are by using table lookup method and through polynomial expansions (Taylor Series expansion). The above mentioned methods require large number of multiplications or divisions and additions or subtractions. Our approach provides a better solution for its hardware implementation with high accuracy and low cost in terms of required lookup table (LUT) size.

MOTIVATION

Our proposed algorithm of approximated function aims to avoid the use of exponential function and minimise the multipliers and dividers thereby reducing power consumption. Thus it is appropriate for execution in application on processor chips.

HARDWARE & SOFTWARE REQUIREMENTS —

- For simulation, synthesizing, implementation, I/O planning (mapping with hardware) and for dumping our code into hardware we are using vivado software.
- We have used FPGA (Nexys 4 DDR) kit to implement it on hardware.
- Genus Synthesis Software for optimized Power and Area report.
- Origin Software for plotting Graph.

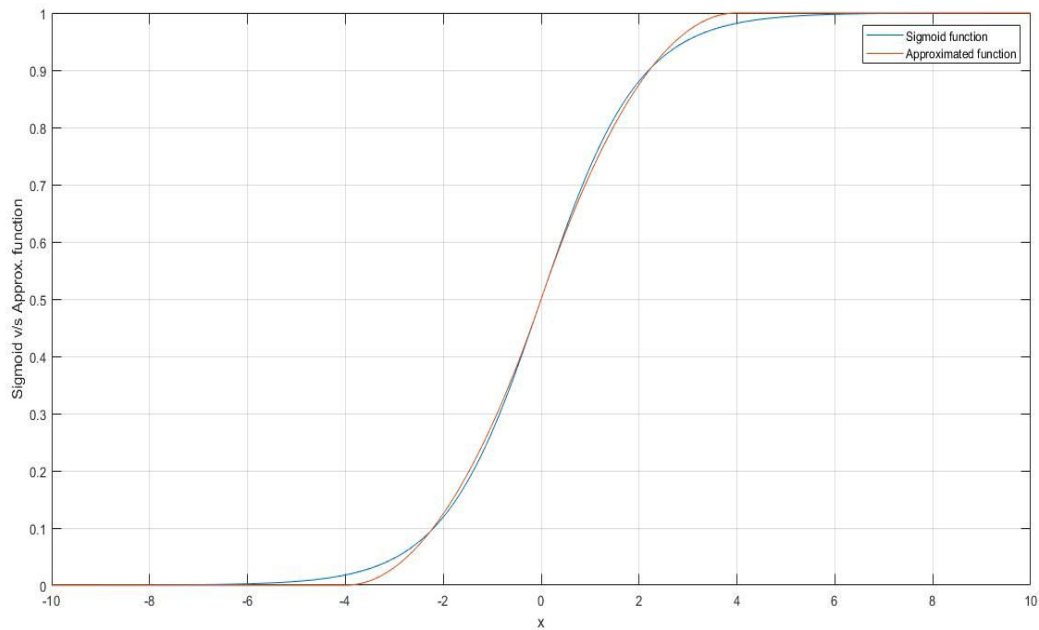
SIGMOID FUNCTION

$$f(x) = \frac{1}{1+e^{-x}} \quad \forall x \in \mathbb{R}$$

PIECEWISE NONLINEAR APPROXIMATION

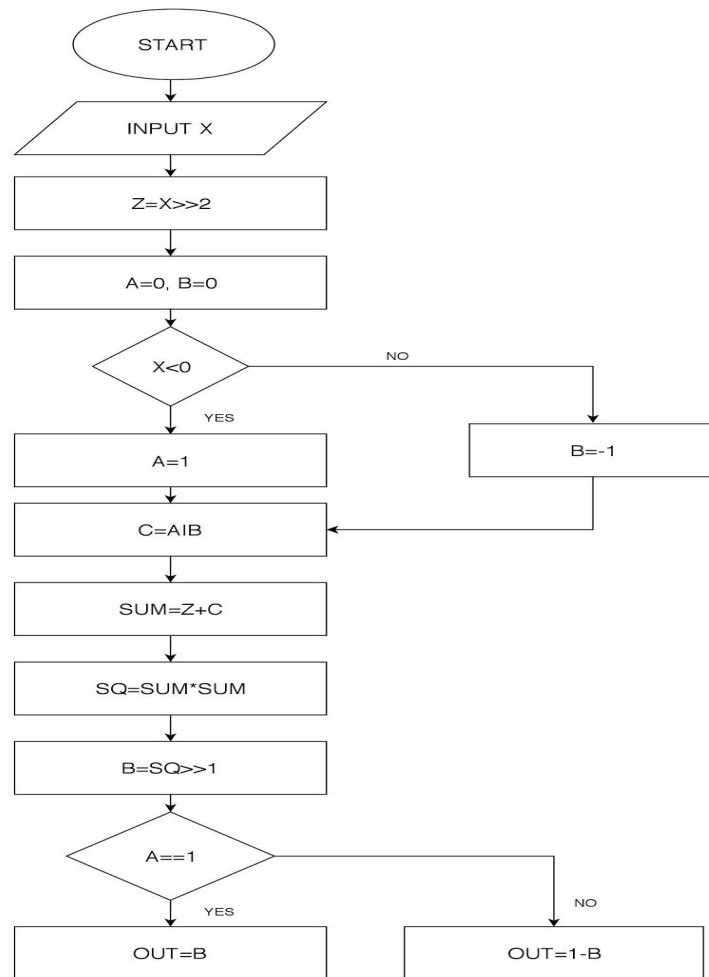
$$f(x) = \begin{cases} 1 - \frac{1}{2} \left(\frac{x}{4} + 1 \right)^2 & \text{if, } 0 \leq x \leq 4 \\ 1 & \text{if, } x > 4 \end{cases}$$

For $x < 0$, $f(x)$ can be simply written as $(1-f(-x))$



Piecewise Second Order V/S Sigmoid Function

PROPOSED METHODOLOGY



The proposed methodology aims to avoid the use of exponential function and minimise the multipliers and dividers. Our approximated expression uses multiplication or division with constants which is power of 2. This can be easily achieved through the use of shifters rather than multipliers. So we are shifting a number by n places in order to multiply by 2^n (left shift) or divide by 2^n (right shift).

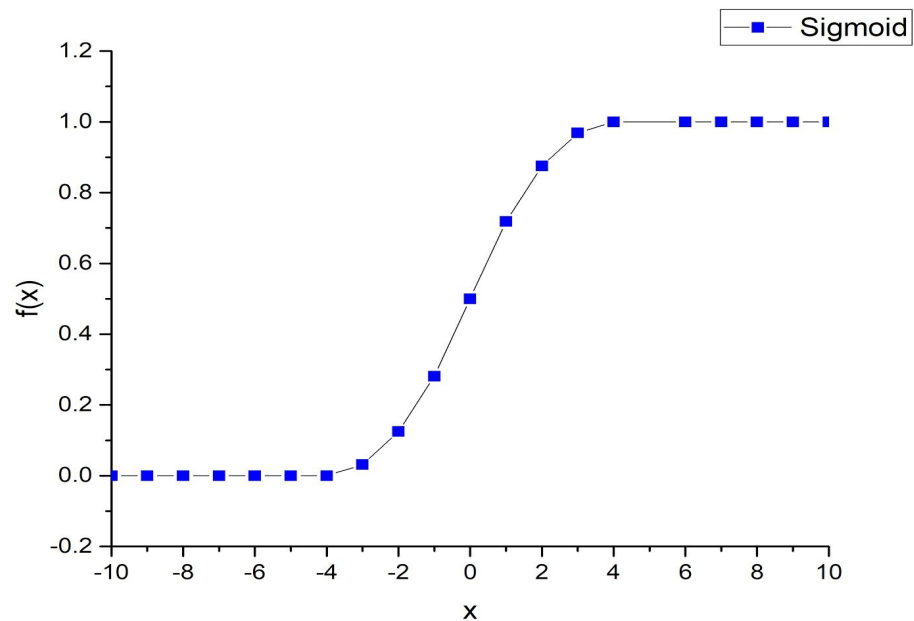
Results:

Simulation result:

Value		10 ns	10 ns	20 ns	30 ns	40 ns	50 ns	60 ns	70 ns	80 ns
4.0		-4.0	-3.0	-2.0	-1.0	0.0	1.0	2.0	3.0	4.0
1.0		0.0	0.03125	0.125	0.28125	0.5	0.71875	0.875	0.96875	1.0

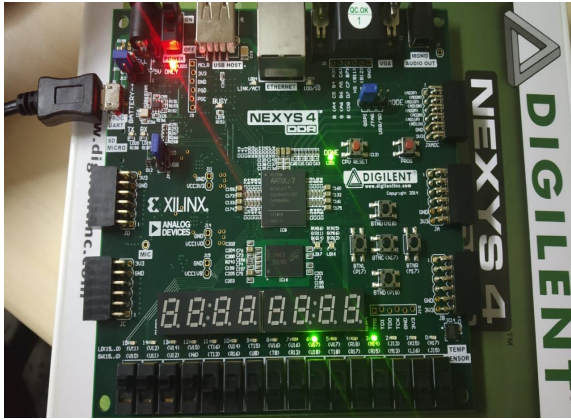
POWER AND AREA :

Total Cells	Dynamic power(nw)	Total Power(mW)	Total Area(m^2)	Power(mW)
748	10.885	0.639744229	0.015486480	0.639755114

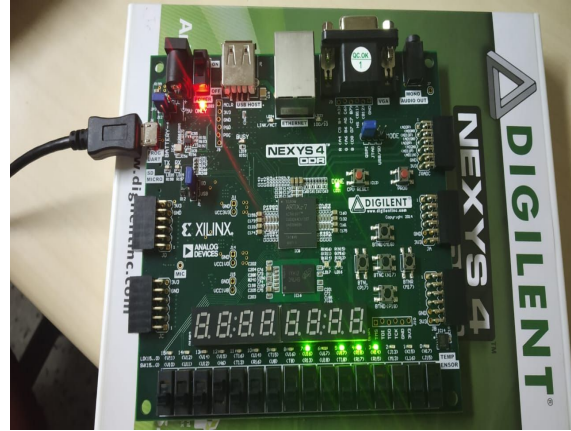


Resultant Plot (From Origin)

FPGA Results:



$x=-1$ ($Y=0.28125$)



$x=1$ ($Y=0.71875$)

First 8 bits represent decimal part, next 8 bits represent fractional part.

Advantages:

- This algorithm provides high performance with low implementation cost (requires less no. of cells); thus, it is suitable for hardwired cost effective neural emulators.
- The proposed method avoids the use of exponential function.
- Our method provides minimum power consumption with highly accurate results.

Limitations:

- This method requires the use of one multiplier .
- Number of gates required is more as compared to piecewise linear function.

REFERENCES

- [1].DIGITAL IMPLEMENTATION OF THE SIGMOID FUNCTION FOR FPGA CIRCUITS Alin TISAN, *Stefan ONIGA, Daniel MIC, Attila BUCHMAN* Electronic and Computer Department, North University of Baia Mare, Baia Mare, Romania Str. Dr. Victor Babeş, nr. 62A, tel. 0362-401265 ext. 234, alin.tisan@ubm.ro
- [2].Syahrulanuar Ngah, Rohani Abu Bakar”Sigmoid Function Implementation Using the Unequal Segmentation of Differential Lookup Table and Second Order Nonlinear Function” Vol 9, No 2-8 page no.-103-108
- [3].Ashkan Hosseinzadeh Namin, Karl Leboeuf, Roberto Muscedere, Huapeng Wu, and Majid Ahmadi,”Efficient hardware implementation of the hyperbolic tangent sigmoid function” **Publisher: IEEE Published in: 2009 IEEE International Symposium on Circuits and Systems**
- [4]. Zhang, M., et al.: “Sigmoid generators for neural computing using piecewise approximations”, *IEEE Trans. Comput.*, 45, (9), pp. 1045–1049, 1996.
- [5]. Basterretxea, K., et al.: “Digital design of sigmoid approximator for artificial neural networks”, *Electron. Letters*, 38, (1), pp. 35–37, 2002.

Comments and Suggestions: