

Mission 008: Week 4 Quiz Graded Quiz • 30 min



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Mission 008: Week 4 Quiz

LATEST SUBMISSION GRADE

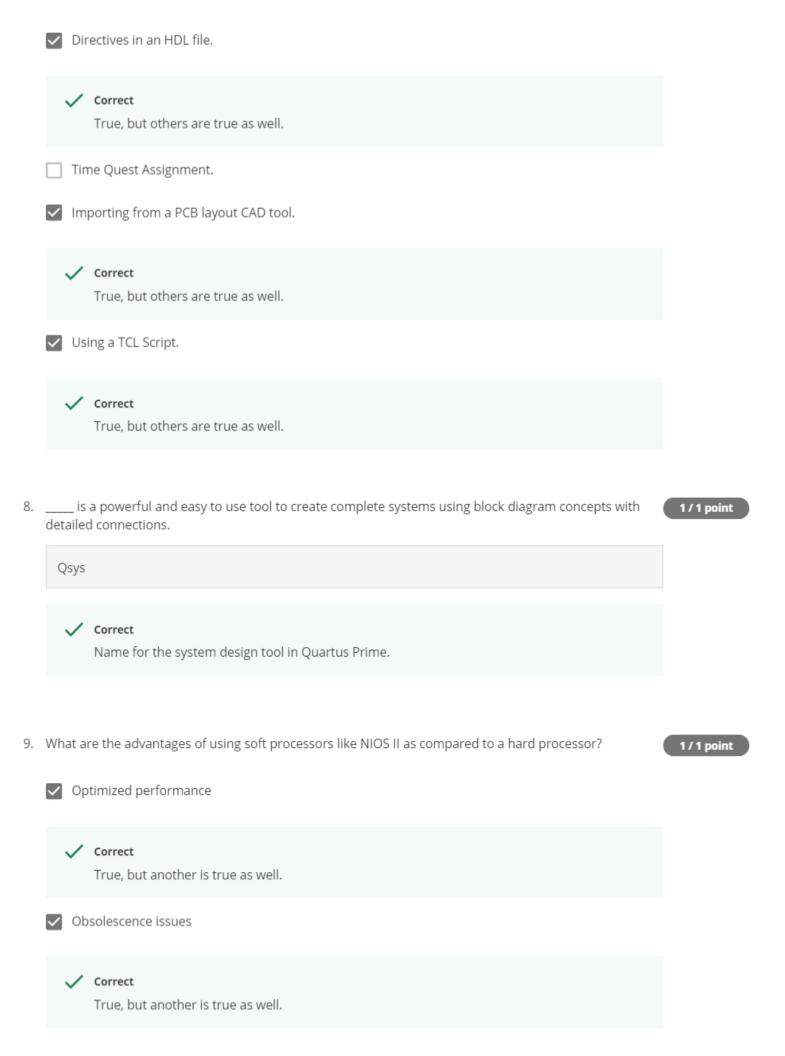
95%

1.	Mark the section under which you can find basic Arithmetic IP Blocks in Quartus Prime?	1/1 point
	○ IP Catalog->Library->University Programs	
	○ IP Catalog->Library->Interface Protocols	
	IP Catalog->Library->Basic Functions	
	○ IP Catalog->Library->DSP	
	✓ Correct Correct. Arithmetic IP Blocks are found in the Basic Functions.	
2.	What are the advantages of using IP blocks ? (Mark all that apply)	2/2 points
	Improves productivity	
	✓ Correct True, but another is true as well.	
	Fewer timing issues	
	Simplifies design entry	
	✓ Correct True, but another is true as well.	

3.	Which o	f the following are correct regarding pipelining ? (Mark all that apply)	1.5 / 2 points
	✓ Imp	proves the speed of the design.	
	*	Correct True, but others are true as well.	
	Can	n be applied in some cases.	
	✓ Tim	ne Quest in Quartus Prime is used to identify critical paths that may benefit from pipelining.	
	•	Correct True, but others are true as well.	
	☐ Hel	ps in mitigating latency of the system.	
	Yo	ou didn't select all the correct answers	
4.	Which o	of the following are a differential I/O standard? (Mark all that apply)	1/1 point
		CMOS	
	✓ LVD	DS .	
	*	Correct True, but others are true as well.	
	✓ LVP	PECL	
	*	Correct True, but others are true as well.	
	LVT	TL	

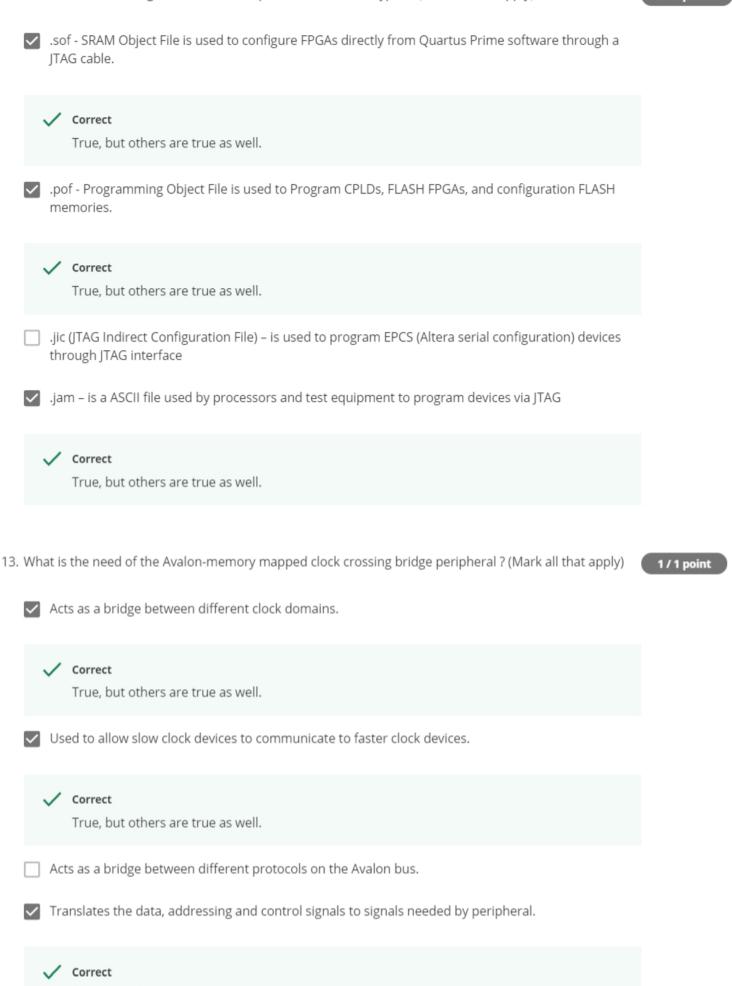
5. True or False: Single ended signals have different voltage swings at the same voltage depending on whether they are TTL or CMOS.

	TrueFalse					
	~	Correct CMOS usually has wider voltage swings than TTL at the same operating voltage.				
6.	Which	of the following are advantages of using logic standards such as LVDS and LVPECL? (Mark all that)	0.5 / 1 point			
	✓ B	etter noise immunity				
	~	Correct True, but another is true as well.				
	✓ D	eterministic				
	!	This should not be selected Any type of logic can have deterministic timing, so this is not an advantage.				
	✓ L	esser pin requirement				
	!	This should not be selected Differential I/O requires twice as many pins.				
	✓ H	igher speed				
	~	Correct True, but another is true as well.				
7.	Which	of the following is a technique to assign pins in Quartus Prime ?	2/2 points			
	✓ T	he Pin Planner or Assignment Editor.				
	~	Correct True, but others are true as well.				



Resource usage efficiency	
✓ Correct True, but another is true as well.	
10. Which of the following correctly define these activities?	1/1 point
Programming - the action of placing into memory the contents of a file that will be used to define the behavior of the device, whether it be a microcontroller or a programmable logic device.	
✓ Correct True, but others are true as well.	
Configuration - the process of unloading that memory into the device to establish the characteristic behavior.	
Configuration - the process of loading programmed memory into the device to establish the characteristic behavior.	
✓ Correct True, but others are true as well.	
11. Which of the following is not a configuration mode available in Quartus Prime?	1/1 point
☐ JTAG	
Configuration via Parallel	
 Correct Correct, this is not a configuration mode in Quartus. 	
Active and Passive Serial	
Configuration via Protocol	
Fast Passive Parallel	

True but others are true as well



14	4. How many gates does it take to create a 4 bit adder using the ripple carry method?			
	O 4			
	O 12			
	20			
	O 15			
	~	Correct A full 1-bit adder takes 5 gates, and with the ripple carry method these can be replicated for each added bit.		
15	. Pipelini	ing is useful to	1/1 point	
		ow down designs that are too fast		
	_	ansport data from input to output instantaneously		
	Break	eak up long delays, allowing faster clock speeds.		
	✓	Correct. Pipelining allows faster clocks by creating smaller sections between registers.		
16	. The be	st single-ended logic type for low power applications is	1/1 point	
	3.3	Bv LVCMOS		
) 1.8	By LVCMOS		
	1.5	SV LVCMOS		
	3.3	By LVTTL		
	~	Correct Among these, CMOS is lower power than TTL, and the lowest voltage will have the lowest overall I*V power.		

rrue, put others are true as well.