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Mission 008: Week 4 Quiz

LATEST SUBMISSION GRADE

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1. Mark the section under which you can find basic Arithmetic IP Blocks in Quartus Prime ?

1 / 1 point

- ○ IP Catalog->Library->University Programs
- ○ IP Catalog->Library->Interface Protocols
- ◉ IP Catalog->Library->Basic Functions
- ○ IP Catalog->Library->DSP

Correct

Correct. Arithmetic IP Blocks are found in the Basic Functions.

2. What are the advantages of using IP blocks ? (Mark all that apply)

2 / 2 points

- ☑ Improves productivity

Correct

True, but another is true as well.

- ☐ Fewer timing issues
- ☑ Simplifies design entry

Correct

True, but another is true as well.

- ☐ Decreases reusability

3. Which of the following are correct regarding pipelining ? (Mark all that apply) **1.5 / 2 points**

- [x] Improves the speed of the design.

  ✓ **Correct**
  True, but others are true as well.

- [ ] Can be applied in some cases.

- [x] Time Quest in Quartus Prime is used to identify critical paths that may benefit from pipelining.

  ✓ **Correct**
  True, but others are true as well.

- [ ] Helps in mitigating latency of the system.

  You didn't select all the correct answers

4. Which of the following are a differential I/O standard? (Mark all that apply) **1 / 1 point**

- [ ] LVCMOS
- [x] LVDS

  ✓ **Correct**
  True, but others are true as well.

- [x] LVPECL

  ✓ **Correct**
  True, but others are true as well.

- [ ] LVTTL

5. True or False: Single ended signals have different voltage swings at the same voltage depending on whether they are TTL or CMOS. **1 / 1 point**

- (●) True
- ( ) False

✓ **Correct**
CMOS usually has wider voltage swings than TTL at the same operating voltage.

6. Which of the following are advantages of using logic standards such as LVDS and LVPECL? (Mark all that apply) **0.5 / 1 point**

- [x] Better noise immunity

✓ **Correct**
True, but another is true as well.

- [x] Deterministic

! **This should not be selected**
Any type of logic can have deterministic timing, so this is not an advantage.

- [x] Lesser pin requirement

! **This should not be selected**
Differential I/O requires twice as many pins.

- [x] Higher speed

✓ **Correct**
True, but another is true as well.

7. Which of the following is a technique to assign pins in Quartus Prime ? **2 / 2 points**

- [x] The Pin Planner or Assignment Editor.

✓ **Correct**
True, but others are true as well.

- [x] Directives in an HDL file.

Correct
True, but others are true as well.

- [ ] Time Quest Assignment.
- [x] Importing from a PCB layout CAD tool.

Correct
True, but others are true as well.

- [x] Using a TCL Script.

Correct
True, but others are true as well.

8. _____ is a powerful and easy to use tool to create complete systems using block diagram concepts with detailed connections. **1 / 1 point**

Qsys

Correct
Name for the system design tool in Quartus Prime.

9. What are the advantages of using soft processors like NIOS II as compared to a hard processor? **1 / 1 point**

- [x] Optimized performance

Correct
True, but another is true as well.

- [x] Obsolescence issues

Correct
True, but another is true as well.

- [x] Resource usage efficiency

Correct
True, but another is true as well.

10. Which of the following correctly define these activities? **1 / 1 point**

- [x] Programming - the action of placing into memory the contents of a file that will be used to define the behavior of the device, whether it be a microcontroller or a programmable logic device.

Correct
True, but others are true as well.

- [ ] Configuration - the process of unloading that memory into the device to establish the characteristic behavior.
- [x] Configuration - the process of loading programmed memory into the device to establish the characteristic behavior.

Correct
True, but others are true as well.

11. Which of the following is **not** a configuration mode available in Quartus Prime? **1 / 1 point**

- [ ] JTAG
- [x] Configuration via Parallel

Correct
Correct, this is not a configuration mode in Quartus.

- [ ] Active and Passive Serial
- [ ] Configuration via Protocol
- [ ] Fast Passive Parallel

12. Which of the following are correct descriptions for these file types? (Mark all that apply.)

12. Which of the following are correct descriptions for these file types ? (Mark all that apply) **2 / 2 points**

- [x] .sof - SRAM Object File is used to configure FPGAs directly from Quartus Prime software through a JTAG cable.

Correct
True, but others are true as well.

- [x] .pof - Programming Object File is used to Program CPLDs, FLASH FPGAs, and configuration FLASH memories.

Correct
True, but others are true as well.

- [ ] .jic (JTAG Indirect Configuration File) – is used to program EPCS (Altera serial configuration) devices through JTAG interface

- [x] .jam – is a ASCII file used by processors and test equipment to program devices via JTAG

Correct
True, but others are true as well.

13. What is the need of the Avalon-memory mapped clock crossing bridge peripheral ? (Mark all that apply) **1 / 1 point**

- [x] Acts as a bridge between different clock domains.

Correct
True, but others are true as well.

- [x] Used to allow slow clock devices to communicate to faster clock devices.

Correct
True, but others are true as well.

- [ ] Acts as a bridge between different protocols on the Avalon bus.

- [x] Translates the data, addressing and control signals to signals needed by peripheral.

Correct
True, but others are true as well.

True, but others are true as well.

14. How many gates does it take to create a 4 bit adder using the ripple carry method? **1 / 1 point**

- 4
- 12
- 20
- 15

Correct
A full 1-bit adder takes 5 gates, and with the ripple carry method these can be replicated for each added bit.

15. Pipelining is useful to _____. **1 / 1 point**

- Slow down designs that are too fast
- Transport data from input to output instantaneously
- Break up long delays, allowing faster clock speeds.

Correct
Correct. Pipelining allows faster clocks by creating smaller sections between registers.

16. The best single-ended logic type for low power applications is _____. **1 / 1 point**

- 3.3v LVCMOS
- 1.8v LVCMOS
- 1.5v LVCMOS
- 3.3v LVTTL

Correct
Among these, CMOS is lower power than TTL, and the lowest voltage will have the lowest overall I*V power.