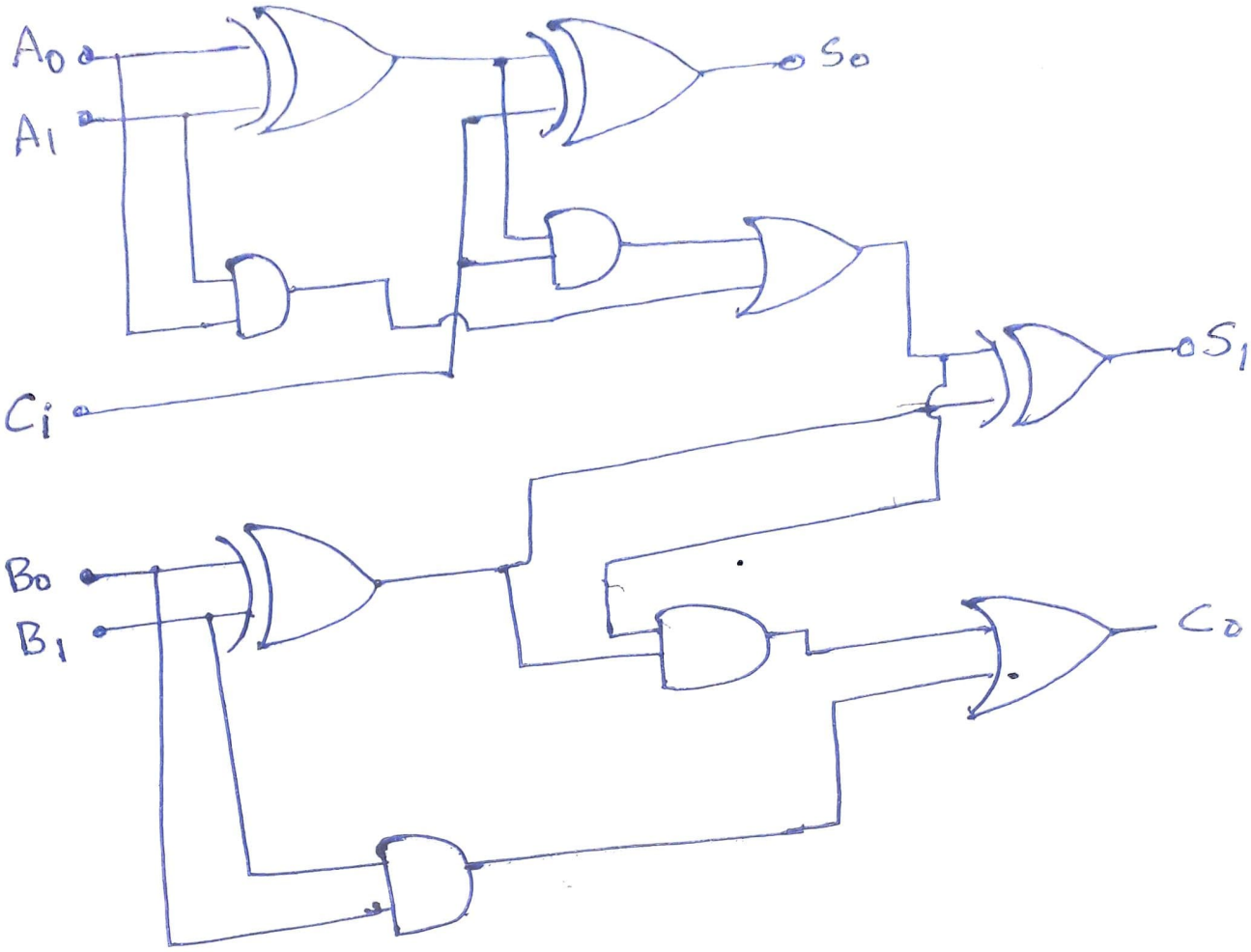
(1) 2-bit full adder.



Boolean Equations

(1)

$$S_0 = A_0 \oplus A_1 \oplus C_i$$

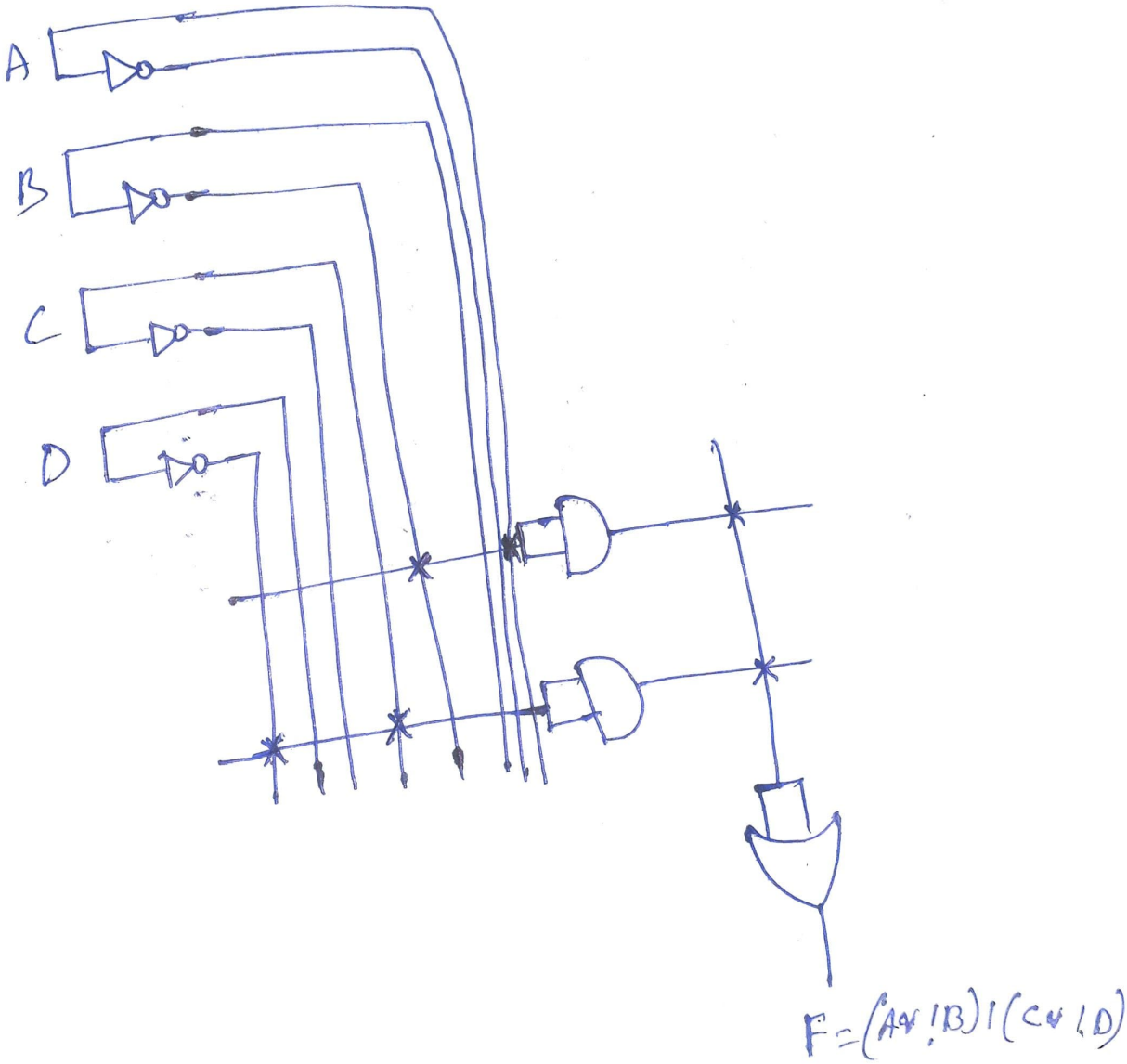
$$S_1 = B_0 \oplus B_1 \oplus [A_0A_1 + C_i[A_0 \oplus A_1]].$$

$$C_0 = B_0B_1 + [(A_0A_1 + C_i[A_0 \oplus A_1])[B_0 \oplus B_1]].$$

Explanation:

A is anded with not(B) and. C is anded with not(D) product the terms are "ored" together is the only possible solution.

Correct PLA fuse pattern



$F = AB' + CD'$

Address		RAM contents		Output data
A	B	C	D	F
0	0	0	0	0
0	0	0	1	0
0	0	1	0	1
0	0	1	1	0
0	1	0	0	0
0	1	0	1	0
0	1	1	0	1
0	1	1	1	0
1	0	0	0	1
1	0	0	1	1
1	0	1	0	1
1	0	1	1	1
1	1	0	0	0
1	1	0	1	0
1	1	1	0	1
1	1	1	1	0