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PES UNIVERSITY

PES University, Bangalore

(Established under Karnataka Act No. 16 of 2013)

UE16CS201

END SEMESTER ASSESSMENT (ESA) B.TECH. 3rd SEMESTER- Dec. 2017

UE16CS201-Digital Design and Computer Organization

Time: 3 Hrs | Answer All Questions | Max Marks: 100

1.	a)	Simplify the following expression to (1) sum-of-products and (2) products-of-sums: F=ACD' + C'D + AB' + ABCD	6
	b)	Design a majority circuit is a combinational circuit whose output is equal to 1 if the input variables have more 1's than 0's. The output is 0 otherwise.	6
	c)	Design a 2X2 bit multiplier. Construct the truth table and simplify the outputs using K-map	8
2.	a)	Design two-to-four line decoder using NOR gates only. Include an enable input.	6
	b)	A sequential circuit has two JK flip-flops A and B, two inputs X and Y, and one output Z. The flip-flop input equations and circuit output equation are: JA=BX+B'Y' ; KA=B'XY' ; JB=A'X ; KB=A+XY' ; Z=AX'Y'+BX'Y' • Tabulate the state table. • Draw the corresponding state diagram.	6
	c)	A PN flip-flop has four operations: clear to 0, no change, complement, and set to 1, when inputs P and N are 00, 01, 10, and 11, respectively (i) Tabulate the characteristic table. (ii) Derive the characteristic equation. (iii) Tabulate the excitation table. (iv) Show how the PN flip-flop can be converted to a D flip-flop.	8
3.	a)	Design a sequential circuit with two D flip-flops A and B and one input x_in. When x_in=0, the state of the circuit remains the same. When x_in=1, the circuit goes through the state transitions from 00 to 01, to 11, to 10, back to 00 and repeats.	8
	b)	Design a counter with T flip-flop that goes through the following binary repeated sequence: 0,1,3,7,6,4.	8
	c)	List out the functional units of a computer.	4
4.	a)	Give the sequence of events involved in handling an interrupt request from a single device. Assuming that interrupt are enabled.	8
	b)	Multiply the following pairs of signed 2's complement numbers using the Booth algorithm. Assume that A is the multiplicand and B is the multiplier. A=110101 and B=011011.	6
	c)	Write a Micro routine for the instruction Branch <0.	6
5.	a)	Write an ALP program that reads a line of characters and displays it.	8
	b)	Write a program that can evaluate the expression (A X B)+ (C X D) In a single-accumulator processor. Assume that the processor has Load, Store, Multiply and Add instructions, and that all values fit in the accumulator.	6
	c)	Write the sequence of control steps required for the single-bus organization of the data path inside a processor for the following instruction: Add the (immediate) number NUM to register R1.	6