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PES University, Bangalore

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UE18CS253

END SEMESTER ASSESSMENT (ESA) B. TECH IV SEMESTER- June 2020
UE18CS253 – Microprocessor and Computer Architecture

Time: 3 Hrs | Answer All Questions | Max Marks: 100

Note: All answers must be precise and to the point.

1.	a)	Differentiate the following. i. Microprocessor and Microcontrollers. ii. RISC and CISC with respect to processor architecture.	4
	b)	Explain logical and arithmetic shift instructions with an example.	4
	c)	Write a general structure of subroutine. Write a Recursive Program to find the factorial of a Number using subroutine.	6
	d)	i. Explain how to encode data processing instructions. ii. Encode the ARM instruction: **ADDS R1, R0, R2 LSR R4** (opcode for ADD is 0100	6
2	a)	Define Pipeline processing. Explain various stages in a Pipeline execution with neat diagram.	6
	b)	Define Latency and throughput with respect to pipeline. Give one example	2
	c)	Consider a non-pipelined processor with a clock rate of 2.5 gigahertz and average cycles per instruction of 4. The same processor is upgraded to a pipelined processor with five stages but due to the internal pipeline delay, the clock speed is reduced to 2 gigahertz. Assume there are no stalls in the pipeline. What is the speed up achieved in this pipelined processor?	4
	d)	Explain in detail, the pipeline hazards.	8
3.	a)	With figure explain about direct mapping cache memory.	4
	b)	A computer system uses 16-bit memory addresses. It has a 2K-byte cache organized in a direct-mapped manner with 64 bytes per cache block. Assume that the size of each memory word is 1 byte. i. Calculate the number of bits in each of the Tag, Block, and Word fields of the memory address. ii. When a program is executed, the processor reads data sequentially from the following word addresses:	6

		128, 144, 2176, 2180, 128, 2176 All the above addresses are shown in decimal values. Assume that the cache is initially empty. For each of the above addresses, indicate whether the cache access will result in a hit or a miss.	
	c)	What is cash miss? Explain the different categories of misses.	4
	d)	Consider a 2-way set associative cache memory with 4 sets and total 8 cache blocks (0-7) and a main memory with 128 blocks (0-127). What memory blocks will be present in the cache after the following sequence of memory block references if LRU policy is used for cache block replacement. Assuming that initially the cache did not have any memory block from the current job? 0 5 3 9 7 0 16 55	6
4.	a)	Explain the cache optimization: Giving priority to Read misses over Write misses to reduce miss penalty.	4
	b)	Write a short note on TLB	4
	c)	Explain in detail the Flynn's classification of computers.	6
	d)	Explain Amdahl's law and Gustafson's law.	6
5.	a)	Define the following terms: i. ILP ii. VLIW iii. Superscalar Processor **iv.** Speculation	4
	b)	What is loop unrolling? Write about limits of loop unrolling.	4
	c)	Explain single core and multicore processor with necessary diagrams.	6
	d)	What is dynamic scheduling? Explain the Dynamic scheduling techniques.	6