Hardware Accelerated Computing
Elective Course (Semester VI)

Motivation

- A few years back...
  - **Intel** bought Altera, an FPGA vendor, for **$17 Billion**
  - **Google** developed Tensor Processing Unit accelerator for **AI/ML** processing
- A few weeks back...
  - **AMD** bought Xilinx, another FPGA vendor, for **$35 Billion**
  - **Amazon** shifted **Alexa** Cloud AI processing to its own Inferentia accelerator
- What is the mystery behind established CPU companies buying these so-called FPGA vendors? And software companies developing hardware accelerators?
- Might such developments impact your career and job prospects?

Hardware Acceleration crucial for compute intensive, big data workloads such as AI/ML

Prerequisites

- Digital Design and Computer Organization

Syllabus

Topics in Hardware Acceleration (4-0-0-0-4)

1. **Introduction** Business and technical motivations (Moore/Dennard scaling challenges and ML / big data computation requirements), illustrative acceleration use case (NFA based regular expression matching)
2. **FPGA hardware and software** Architecture and organization (logic blocks, interconnect, memory and arithmetic blocks) of modern FPGAs (Field Programmable Gate Arrays), HDLs (Hardware Description Languages) and CAD tools
3. **Accelerator Logic** Efficient logic structures for Signed Digit arithmetic, CORDIC, FFT and convolution computations
4. **High Level Synthesis (HLS)** Need for HLS, HLS Languages for FPGA/ASIC (System C and Open CL), FPGA tools for HLS, ASIC tools for HLS, matrix multiplication design and implementation using HLS
5. **Platforms and Case Studies** Hardware acceleration platforms (FPGAs, GPUs and TPUS) and case studies (search engines in data centers and machine learning in cloud)

Reference Material

1. High Level Synthesis: from Algorithm to Digital Circuit, Editors: Coussy Philppe, Morawiec Adam. Springer, 2008
2. Digital Arithmetic (1st Edition) by Milo D. Ercegovac and Tomás Lang, Morgan Kaufmann, 2004
3. Parallel Programming for FPGAs by Ryan Kastner, Janarbek Matai, and Stephen Neuendorffer, Creative Commons, 2018
4. Relevant academic papers and Intel/AMD user manuals

Evaluation Scheme

ISA 1	10
ISA 2	10
Assignments / Mini Project	30
ESA	50

Course Objectives and Outcomes

Course Objectives

To provide a sound understanding of:

1. The motivations for the increasing trend of hardware acceleration
2. The architecture of modern programmable logic devices
3. Efficiencies obtained over software by direct implementation of computation in hardware
4. Modern industry standard development tools

Course Outcomes

The course will be enable the student to:

1. Comprehend the rationale behind and adapt to the shift towards hardware acceleration in mainstream computing
2. Build efficient computation structures to accelerate computation
3. Use industry standard tools to implement accelerator logic
4. Design and implement accelerator logic to speed up an application