ECEN 5613 Fall 2014	Embedded System Design Lab #1 Signoff Sheet - Software	Week #1 8/25/2014

You will need to obtain the signature of your TA on the following items in order to receive credit.

The software portion of Lab #1 should be completed and signed off by **Wed., Sept. 10, 2014** in order to give you time to complete the hardware portion upon receipt of your parts kit. Both signoffs are due by **Wednesday, Sept. 17, 2014**. You need to submit both of your signoff sheets and other required elements by **11:59pm Thurs., Sept. 18, 2014**. Labs completed after the signature due date or submitted after the submission due date will usually receive grade reductions, but there is leniency on Lab #1.

Print your name below and then demonstrate your working hardware/firmware in order to obtain the necessary signatures. All items must be completed to get a signature, but partial credit is given for incomplete labs. Receiving a signature on this signoff sheet does not mean that your work is eligible for any particular grade; it merely indicates that you have completed the work at an acceptable level.

Student Name: ANIKET KUMAR LATA

Checklist

- ☑ Student demonstrates detailed knowledge of simulator (Emily52/EdSim51) (including changing register values, editing data memory, using breakpoints, single stepping, uses /overlay option, etc.)
- ☑ Student assembly program works correctly
- ☑ Student demonstrates detailed knowledge of WinCUPL and WinSim, logic equations correct

Student Answers to Lab Questions

1. **How many bytes of code space does your program require?**
   (Show how you arrived at your answer.)
   Code Size? 39 bytes

2. **How long did your program take to execute, assuming X=0x21 and Y=0x06? Assume an 11.0592 MHz clock and include the instructions executed from the beginning of your code until you reach the END label. Show your detailed calculations on the code listing that you submit with the signoff sheet.**
   Execution Time? 73.7821 uS

Mayuk 9/5/2014.

Instructor/TA Comments: ☐ ☐ ☐ **TA signature and date**

FOR INSTRUCTOR USE ONLY	Not Applicable	Poor/Not Complete	Meets Requirements	Exceeds Requirements	Outstanding
SPLD code	☐	☐	☑	☐	☐
Assembly Language Code Style	☐	☐	☑	☐	☐
Required Elements functionality	☐	☐	☑	☐	☐
Sign-off done without excessive retries		☐	☑		
Student understanding and skills	☐	☐	☐ ✓	☐	☐
Overall Demo Quality	☐	☐	☑	☐	☐

Comments: → LST file not shown during signoff.

NOTE: This submission sheet should be the top/first sheet of your submission.

F14 LAB#1 CODE LISTING ANIKET KUMAR LATA

	MNEMONICS	MACHINE CYCLES	EXECUTION TIME
BEGIN:	MOV R0,#0h	1	1.085 μs
	MOV R2,#03h	1	1.085 μs
	XCH A,B	1	1.085 μs
	CJNE A,#0h, LO	2	2.1701 μs
	MOV 30h,#01h	2	
	MOV 20h,#0h	2	
	MOV 21h,#0h	2	
	MOV 22h,#0h	2	
	SJMP END	2	
LO:	XCH A,B	1	1.085 μs
PROC:	SUBB A,B	1	1.085 μs x 6
	JC L1	2	2.1701 μs x 6
	INC R0	1	1.085 μs x 5
	MOV R3,A	1	1.085 μs x 5
	JNZ PROC	2	2.1701 μs x 5
L1:	MOV 20h,R0	2	2.1701 μs
	MOV 21h,R3	2	2.1701 μs
	MOV A,R0	1	1.085 μs
	CLR C	1	1.085 μs
L2:	RLC A	1	1.085 μs x 3
	JNC L3	2	2.1701 μs x 3
	MOV 30h,#02h	2	
	MOV 22h,A	1	
	SJMP END	2	
L3:	DJNZ R2,L2	2	2.1701 μs x 3
	MOV 22h,A	1	1.085 μs
	MOV 30h,#0h	2	2.1701 μs
END:	SJMP BEGIN	2	

73.7821 μs

ECEN 5613 Fall 2014	Embedded System Design Lab #1 Signoff Sheet - Hardware	Week #1 8/25/2014

Print your name below, answer the questions, and then demonstrate your working hardware in order to obtain the necessary signatures. All items must be completed to get a signature.

Student Name: ANIKET KUMAR LATA

Checklist

- ☑ Schematic of acceptable quality, Student name on board in permanent ink
- ☑ Pins and signals labeled, decoupling capacitors, and two 28-pin wire wrap sockets present on board:
- ☑ Mounting hardware present (e.g. standoffs or an enclosure)
- ☑ Power switch and LED, voltage regulator functional, power jack present
- ☑ Power-on Reset (RC) and Run-time Reset (pushbutton), C501 bypass cap is present
- ☑ RS-232 connector mounted, 74LS373 transparent latch wired
- ☑ Logic outputs correct (e.g. SPLD generation of /READ and /CSPERIPH; view SPLD code)
- ☑ Student displays good knowledge of oscilloscope
- ☑ Peak to peak noise measured across processor VCC and GND is < 800mV
- ☑ Oscillator functional (check for correct ALE/XTAL2 signals after power on-off cycles)

→ Decap for SPLD

Student Answers to Lab Questions

1. **What voltage is present at the regulator input?** Use a digital multimeter. 7.63 V
2. **What voltage is present at the regulator output?** Use a digital multimeter. 5.01 V
3. **What peak to peak noise is present across the processor VCC and GND?** Use an oscilloscope.

   Measured value at processor package pins on top side of board: 347.00 mV

   Measured value at wire wrap socket pins on bottom side of board: 304.60 mV
4. **How long is the processor held in reset after the run-time reset pushbutton is released?** Use an oscilloscope and try to measure the time between the release of the pushbutton and the time when noise from ALE is observed on the RST signal.

   Measured value: 10ms
5. **What frequency is present at the ALE pin?** Use an oscilloscope. 1.845 MHz

Aniket 09/16/14

TA signature and date

Instructor/TA Comments: ☐ ☐ ☐

FOR INSTRUCTOR USE ONLY	Not Applicable	Poor/Not Complete	Meets Requirements	Exceeds Requirements	Outstanding
Schematics, SPLD code	☐	☐	☑	☐	☐
Hardware physical implementation	☐	☐	☑	☐	☐
Required Elements functionality	☐	☐	☑	☐	☐
Sign-off done without excessive retries		☐	☑		
Student understanding and skills	☐	☐	☐ ✓	☐	☐
Overall Demo Quality	☐	☐	☑	☐	☐

Comments:

Schematics :- $\overline{EA}$ should be grounded GND for volt regulator

Vcc in pullup resistors

- Labelling of SPLD is above the wire-wrapping

NOTE: This submission sheet should be the second sheet of your submission.

Submission Sheet 2

Submission Sheet

Instructions: Print your name below and sign the honor code pledge. Separate the signoff and submission sheets from the rest of the lab and turn in a scan (or clear picture) of these signed forms, the items in the checklist below, and the answers to any applicable lab questions to the TA or instructor in order to receive credit for your work. No cover sheet please. **Submit as many items as possible electronically via Desire2Learn, to reduce paper usage.**

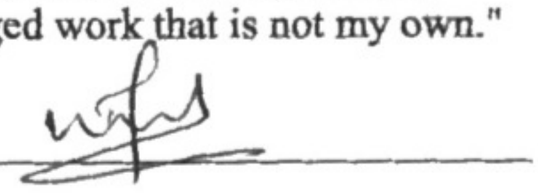
In addition to the items listed on the signoff checklist, be sure to review the lab for additional requirements for submission, including:

- ☑ Scan of signed and dated software signoff sheet as the top sheet (No cover sheet please)
- ☑ Scan of signed and dated hardware signoff sheet as the second sheet
- ☑ Scan of submission sheet with signed honor code pledge as the third sheet
- ☑ Full copy of complete and accurate schematic of acceptable quality (all components shown).
- ☑ Fully, neatly, and clearly commented code in .LST file. Ensure your printout is easy to read.

Make copies of your code, SPLD code, and schematic files and save them as an archive.

Student Name: ANIKET KUMAR LATA

Honor Code Pledge: "On my honor, as a University of Colorado student, I have neither given nor received unauthorized assistance on this work. I have clearly acknowledged work that is not my own."

Student Signature: 

1. **How much power is dissipated in the regulator, assuming a load current of 200mA?** Assume that the regulator is drawing the max quiescent current shown in the data sheet (use the correct data sheet for the regulator you have on your board). Neatly show all your work.

I_Q = Max quiescent current = 6mA ... for voltage regulator 7805CT

Power dissipated in the regulator = $P_{input} - P_{output} = V_i I_i - V_o I_o$

Load current of the regulator is assumed as 200mA

$\therefore I_o = 200mA$, V_o (observed) = 7.63 V V_o (observed) = 5.01 V

Now, $I_i = I_Q + I_o = 6mA + 200mA = 206mA$

Hence, Power dissipated in the regulator = $P_{input} - P_{output}$

$= (7.63 \times 206m) - (5.01 \times 200m)$

$= 569.78mW$

Calculated value: 569.78 mW

Comments: The TA comments for software & hardware signoff have been taken care of by me. This lab provided a good understanding of 8051 basic external circuitry and the internal architecture, memory organisation, instruction set. Programming the SPLD was something new that I learnt. I aim to use the SPLD in the upcoming labs in the decoding logic.

NOTE: This submission sheet should be the third sheet of your submission.