Lab Report

ECEN 5613 | **Embedded System Design** | **Fall 2014**
Lab #2 Signoff Sheet

You will need to obtain the signature of your instructor or TA on the following items in order to receive credit for your lab assignment. Signatures are due by **Friday, September 26, 2014 (Required Elements) and Wednesday, October 1, 2014 (Supplemental Elements)**.

Print your name below, sign the honor code pledge, circle your course number, and then demonstrate your working hardware & firmware in order to obtain the necessary signatures.

Student Name: ANIKET KUMAR LATA

Honor Code Pledge: "On my honor, as a University of Colorado student, I have neither given nor received unauthorized assistance on this work. I have clearly acknowledged work that is not my own."

Student Signature: [signature]

Signoff Checklist

Required Elements

- ☑ Schematic of acceptable quality, correct memory map, SPLD .PLD file
- ☑ Pins and signals labeled, decoupling capacitors, and two 28-pin wire wrap sockets present on board
- ☑ NVRAM (as EPROM substitute), decode logic, and LED functional
- ☑ Understands device programmer.
- ☑ Demonstrated ability to use logic analyzer to capture bus cycles and view fetches from NVRAM. Shows detailed knowledge of both state and timing modes. Captures latched address lines A[15:0], data lines D[7:0], ALE, /PSEN, and NVRAM chip select signal on the logic analyzer display.
- ☑ Shows and discusses logic analyzer screen captures:
- ☑ Assembly program and timer ISR functional:

Freq = 2.28+2

[signature] 09/26/14

TA signature and date

Supplemental Elements (Qualifies ECEN 5613 students for higher grade.)

- ☐ 74LS374 debug port functional
- ☐ Understands timing analysis, setup/hold/propagation

Instructor/TA Comments: ☐ ☐ ☐

TA signature and date

FOR INSTRUCTOR USE ONLY **Required Elements**	Not Applicable	Poor/Not Complete	Meets Requirements	Exceeds Requirements	Outstanding
Schematics, SPLD code	☐	☐	☑	☐	☐
Hardware physical implementation	☐	☐	☑	☐	☐
Required Elements functionality	☐	☐	☑	☐	☐
Sign-off done without excessive retries		☐	☑	☐	☐
Student understanding and skills	☐	☐	☐ ✓	☐	☐
Overall Demo Quality (Required Elements)	☐	☐	☐ ✓	☐	☐

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Student understanding and skills	☐	☐	☐	☐	☐
Overall Demo Quality (Supplemental)	☐	☐	☐	☐	☐

Schematic
- No decoupling for SPLD, ~~EEPROM~~
- Netlabel for Vcc, GND
- ~~Re~~ Update name & doc info

NOTE: This signoff sheet should be the top/first sheet of your submission.

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Mayte 10/1/2014
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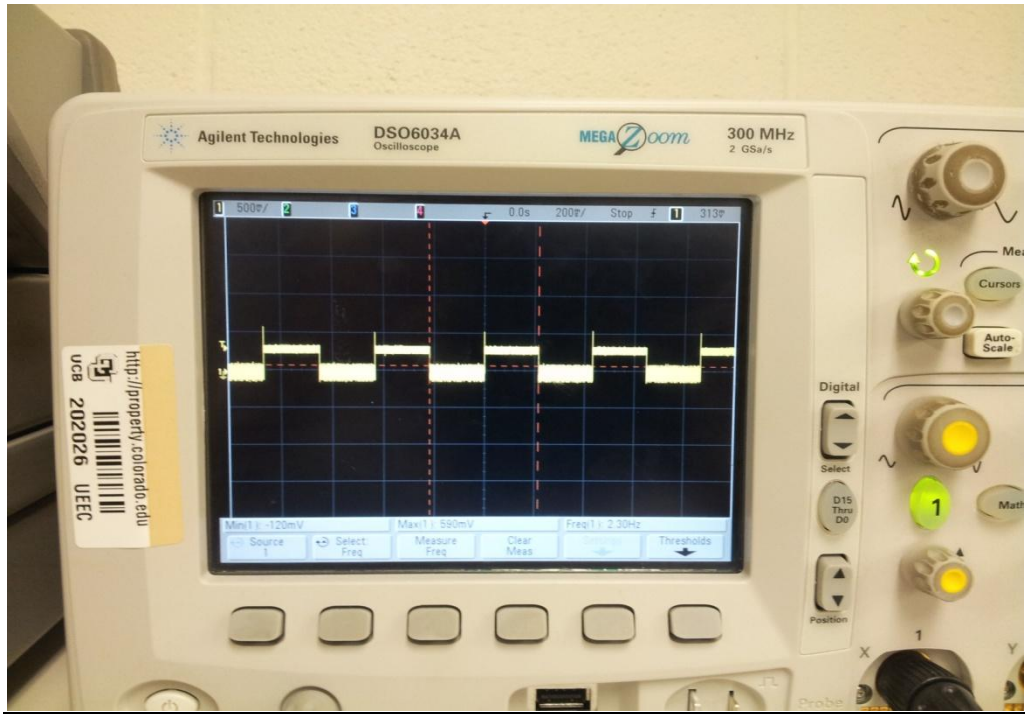
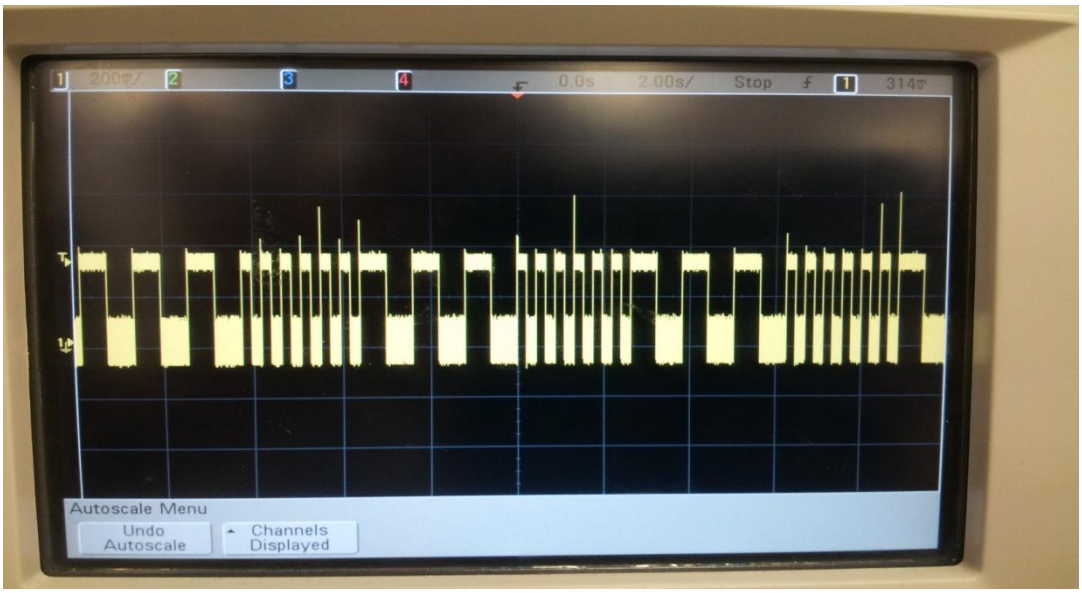
→ Good SOS implementation with 7-segment LED.
→ Submit corrected wold time screenshot

1. Square wave



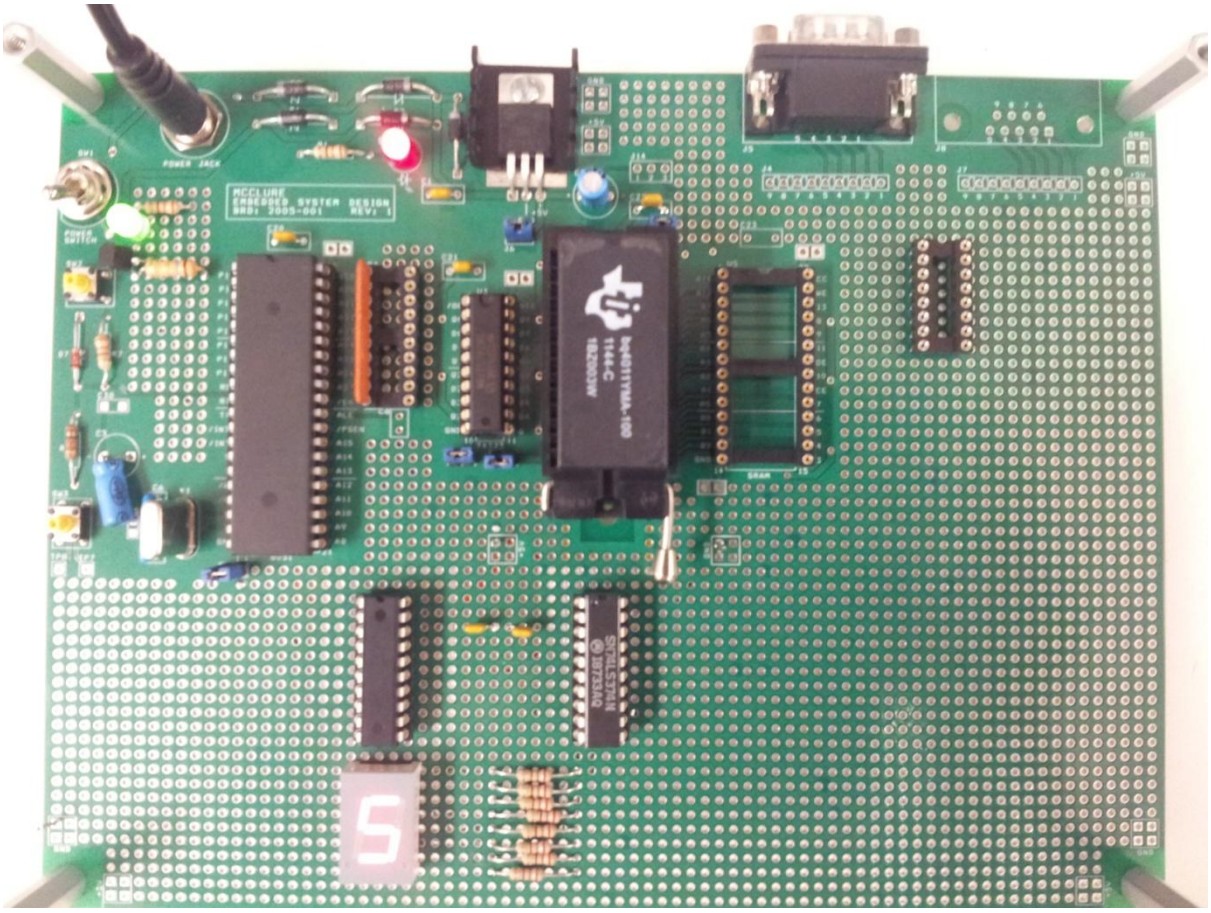
A square wave has been generated as part of Lab2 required element with a frequency of 2.3Hz. Timer 0 Mode 0 was used to generate the delay for square wave.

2. Morse Code 'SOS' signal:



An SOS signal has been generated as an optional element for Lab2.

Morse code SOS implementation on Seven Segment:



3. Using the instruction set summary tables (available in the programmer's guide or instruction set documents), calculate how long the ISR takes to execute once, assuming a clock frequency of 11.0592 MHz. You will likely have some conditional jumps in your ISR code, so make sure to calculate both the longest and shortest time it takes the ISR to execute.

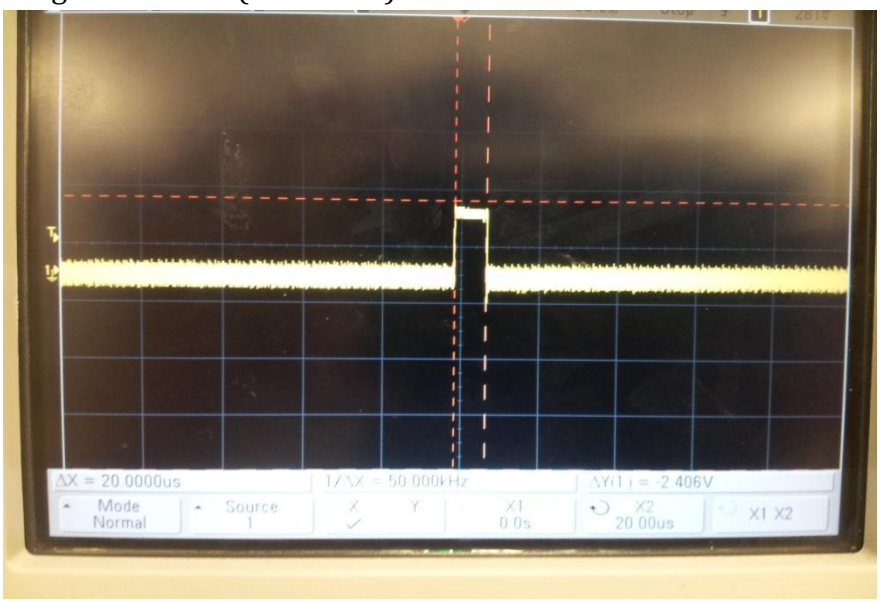
   Longest time for ISR to execute = 1.085us * no. of machine cycles in ISR
   = 1.085us * 18
   = 19.53us

   Shortest time for ISR to execute = 1.085us * no. of machine cycles in ISR
   = 1.085us * 10
   = 10.85us

4. Compare the calculated ISR time to the time measured with the second port pin, which toggles at the beginning and at the end of each ISR execution. Do the calculated and measured times match? Explain any differences you see.

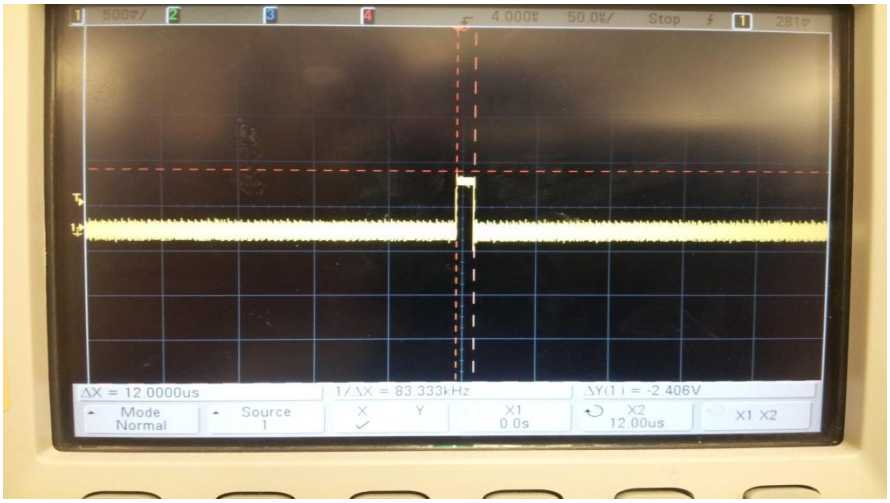
   The ISR times have been calculated from the morse code SOS program.

   Longest ISR time (measured): 20us



   The longest ISR time can be observed when the counter for 217ms has reduced to zero and the instructions within the loop are being executed.

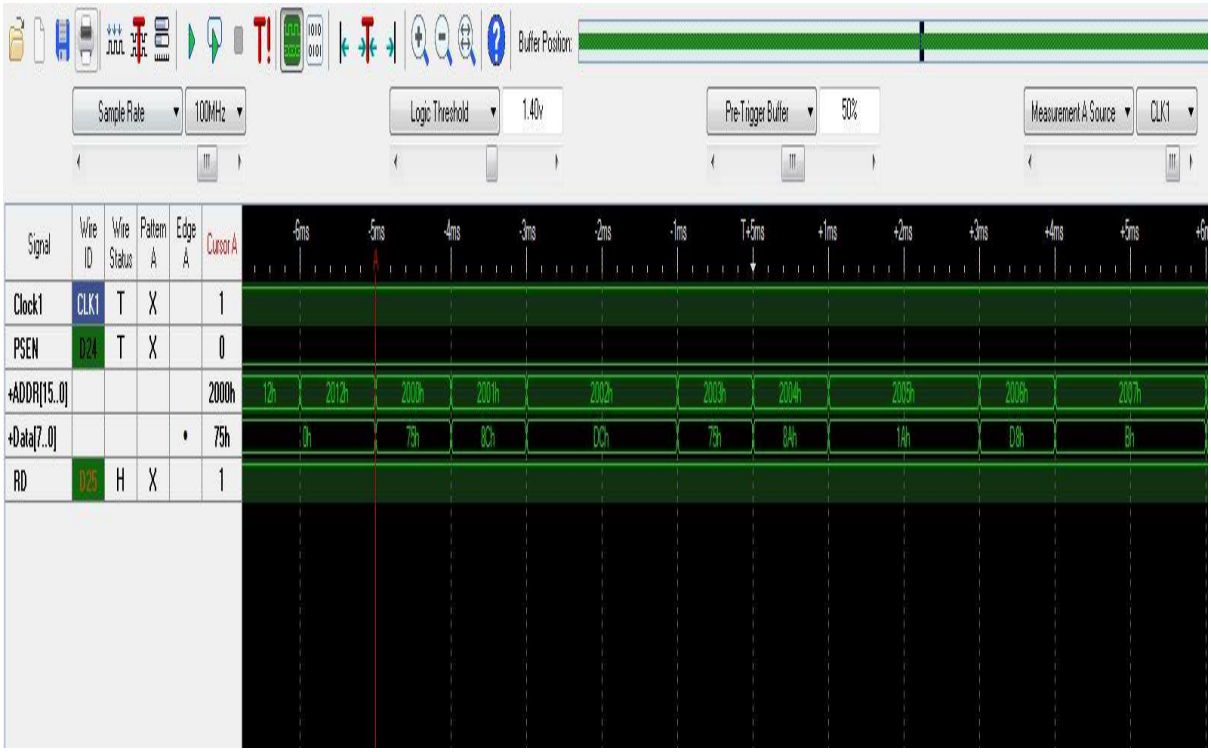
Shortest ISR time (measured): 12us



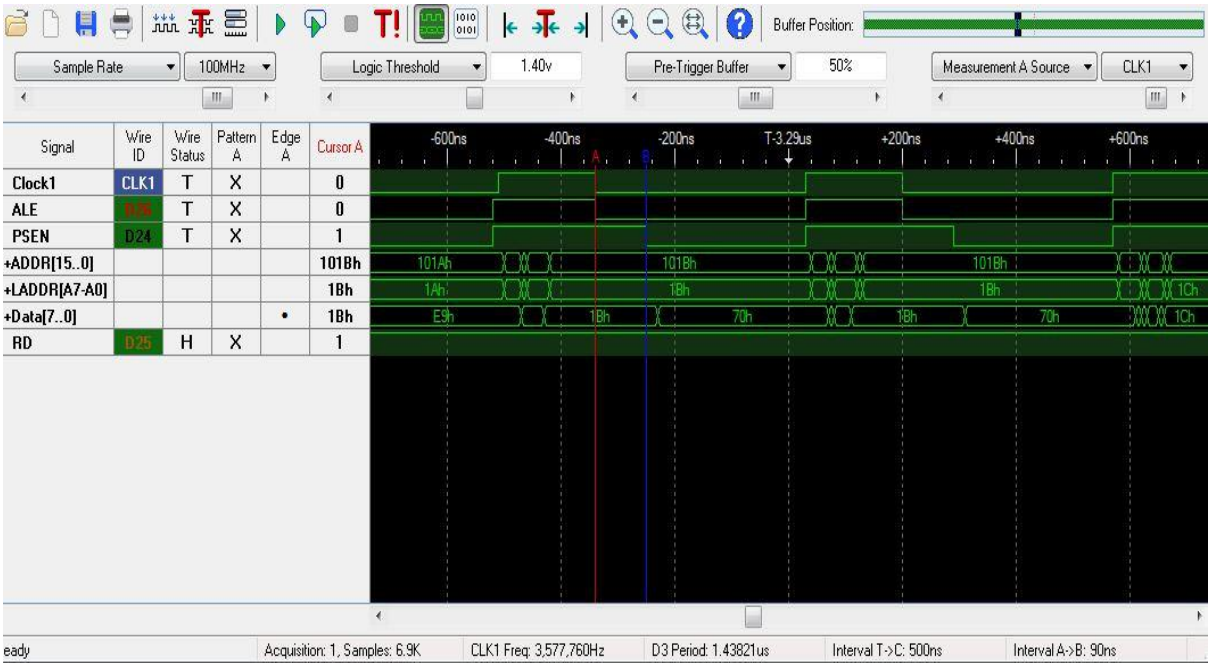
Shortest ISR time is observed when 217ms for the square wave have not elapsed. The ISR time calculated does not match the measured ISR time due to internal propagation delay of components in toggling the port pin.

5. Using the state mode, capture a sequence of instructions and compare the sequence to the listing file for the code being executed. For the state clock, you can investigate using ALE, PSEN or READ signals.

   Below is the capture of sequence of instructions from the Morse listing file.



6. Using the timing mode, measure the time which elapses from when the 74LS373 latches the address supplied by the 8051 to when the PSEN signal is activated during an instruction fetch. Before your demo to the TA, annotate a screen capture to show the measurement of tLLPL in timing mode and prove that your measured time meets the C501 data sheet specification for tLLPL.



Measured time = 90ns

C501 datasheet shows the tLLPL measurement as: tclcl - 25ns

= (1/11.0592MHz) - 25ns

= 65.42ns

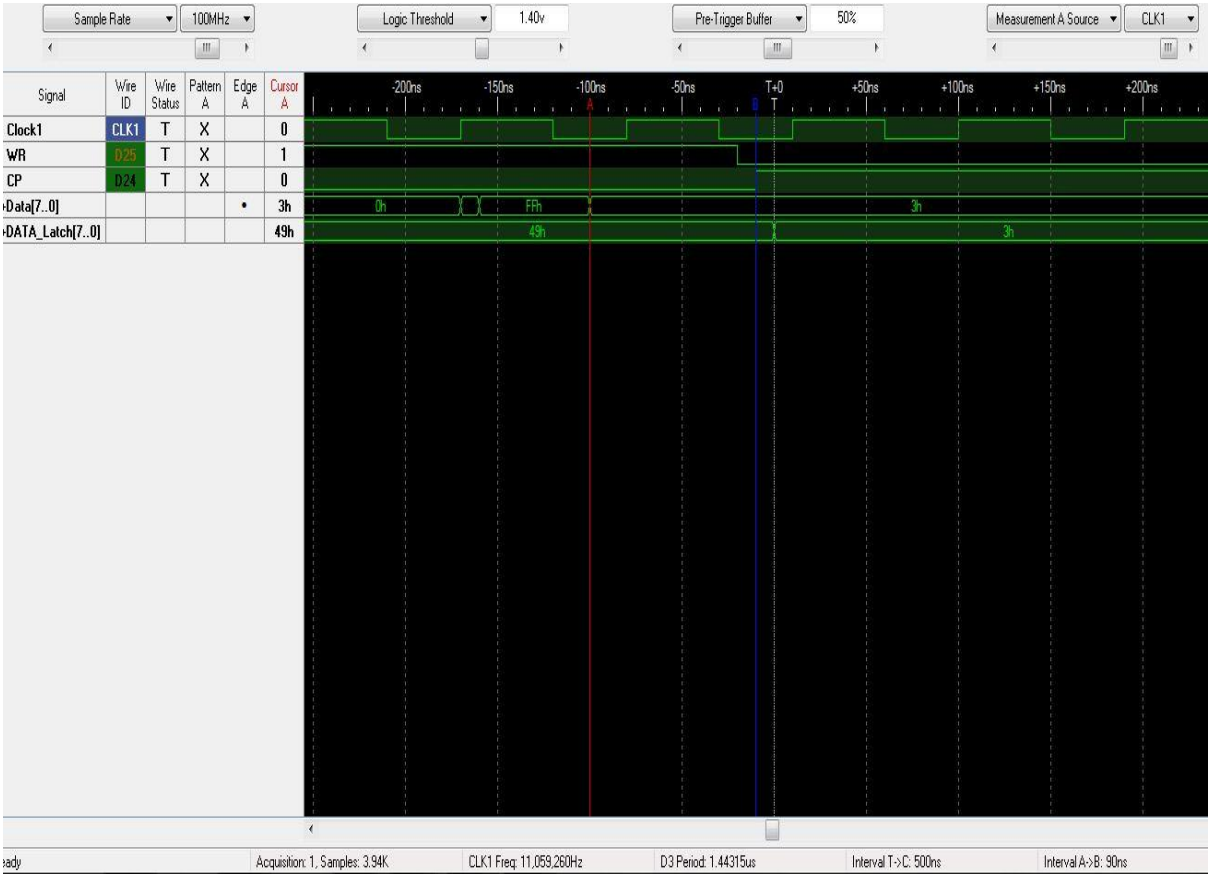
Thus, the measured tLLPL time satisfies the minimum requirement.

7. Perform a timing analysis to prove that your design satisfies the setup and hold requirements for the 74LS374. Your timing analysis should consist of two parts. First, calculate your circuit's minimum setup and hold time using the data sheets for the logic chips used in your design. Second, use a logic analyzer to measure the setup and hold time as seen at the '374 chip. Does your measured time satisfy the setup and hold time requirements of the '374?

   The circuit's minimum setup time: 20ns
   Hold time of circuit: 0ns

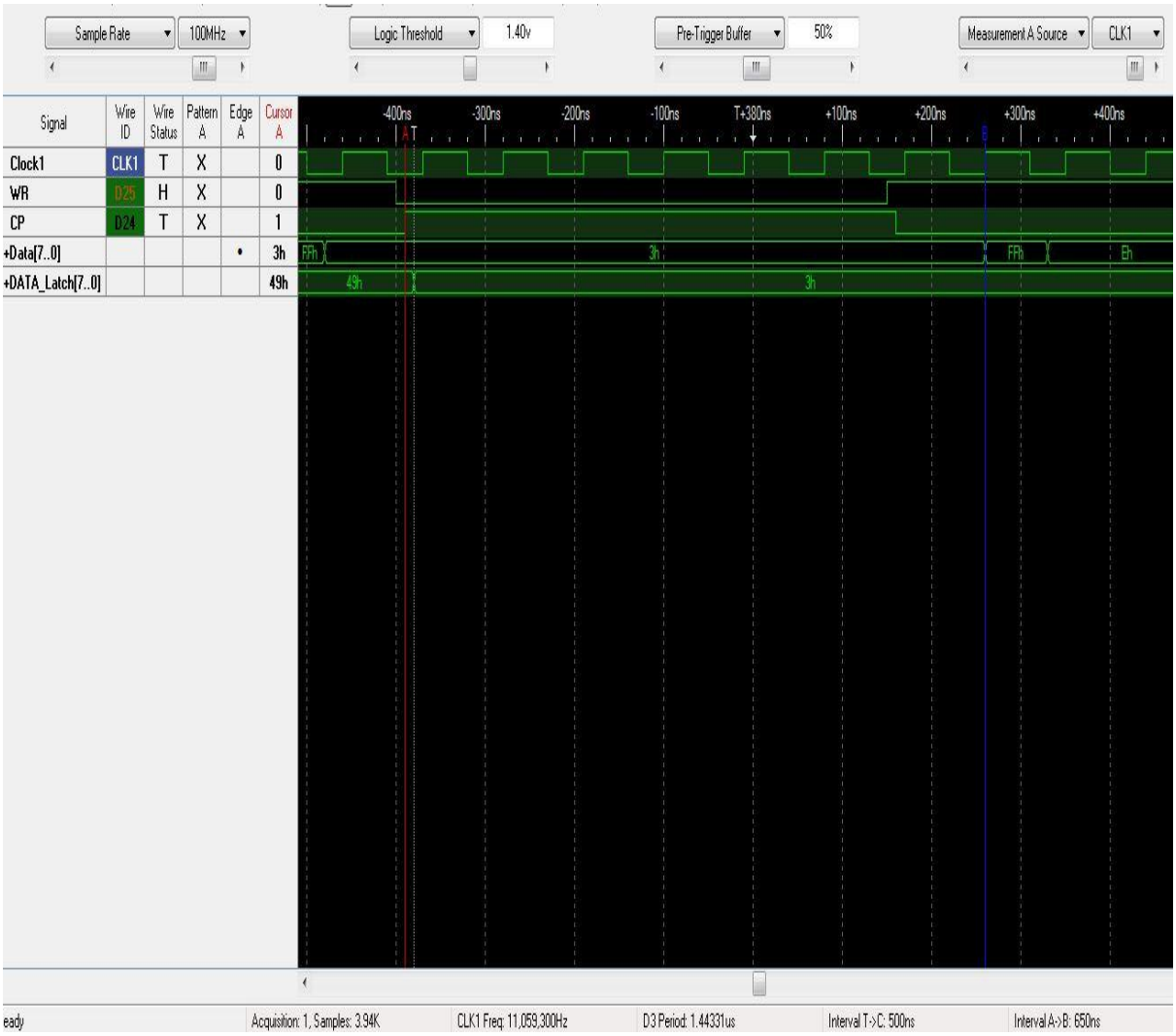
Below are the snapshots of measured setup and hold times:

Setup time:



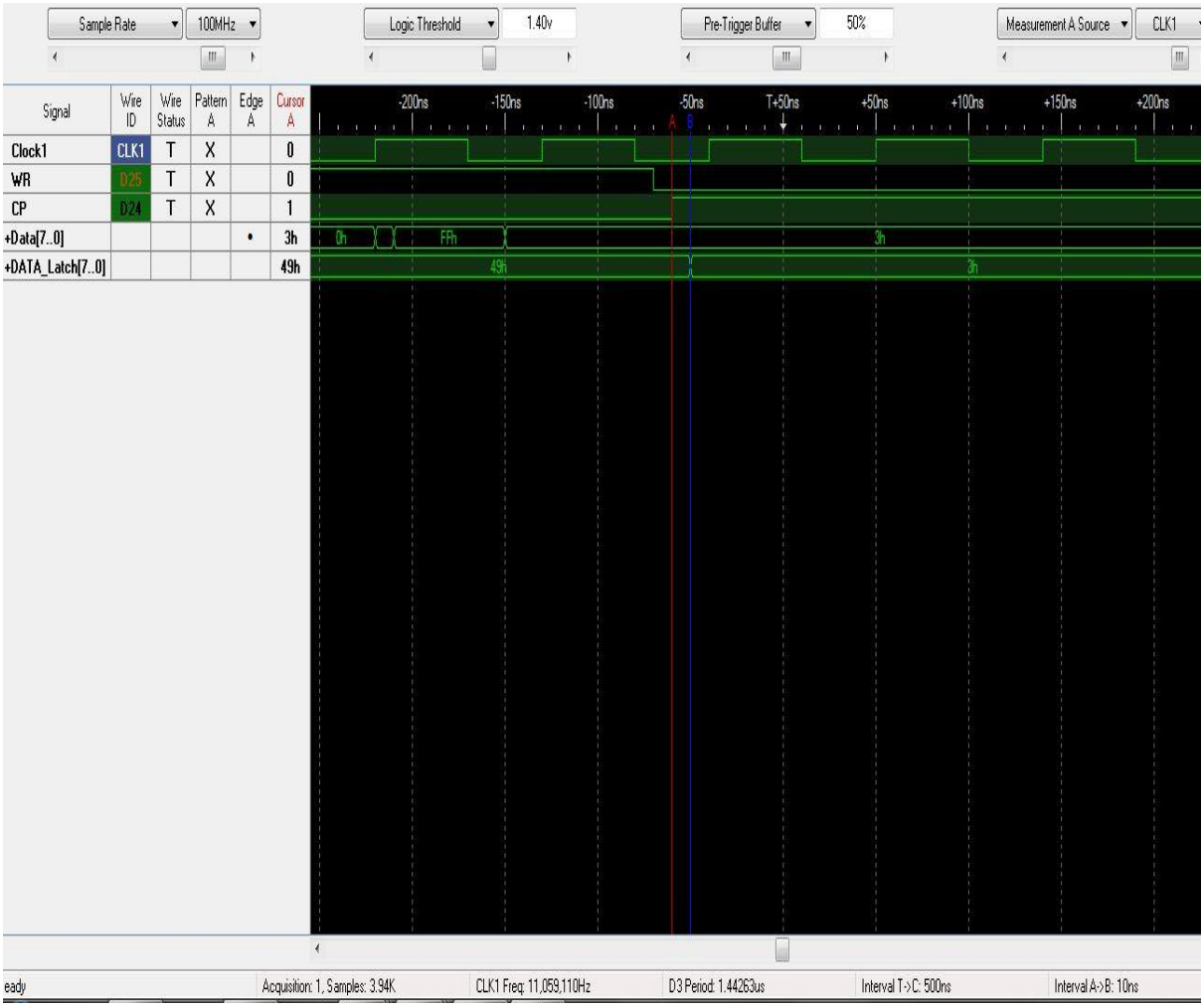
The setup time measured is 90ns. The minimum required setup time is 20ns. The measured setup time exceeds the minimum required time and hence satisfies the criteria.

Hold time:



The hold time measured is 650ns. The minimum required setup time is 0ns. The measured hold time exceeds the minimum required time and hence satisfies the criteria.

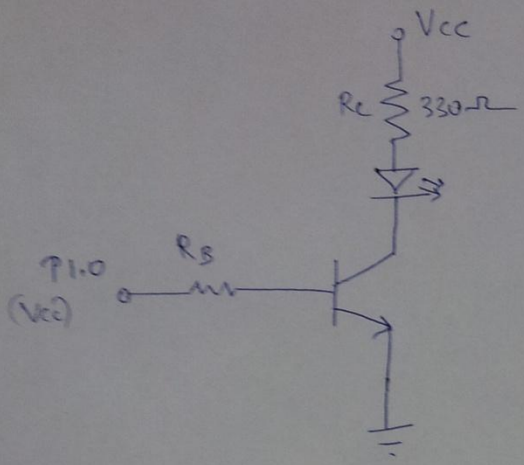
Propagation Delay:



The propagation delay is measured as 10ns.

LED Driver Circuit calculation:

LED DRIVER CIRCUIT



Calculation for R_B:

KVL to output loop:

$V_{cc} - I_C R_C - V_D - V_{CE\,sat} = 0$

$5 - \beta I_B 330 - 0.7 - 0.2 = 0$ (assume $\beta = 50$)

$I_B = 248.48\,\mu A$

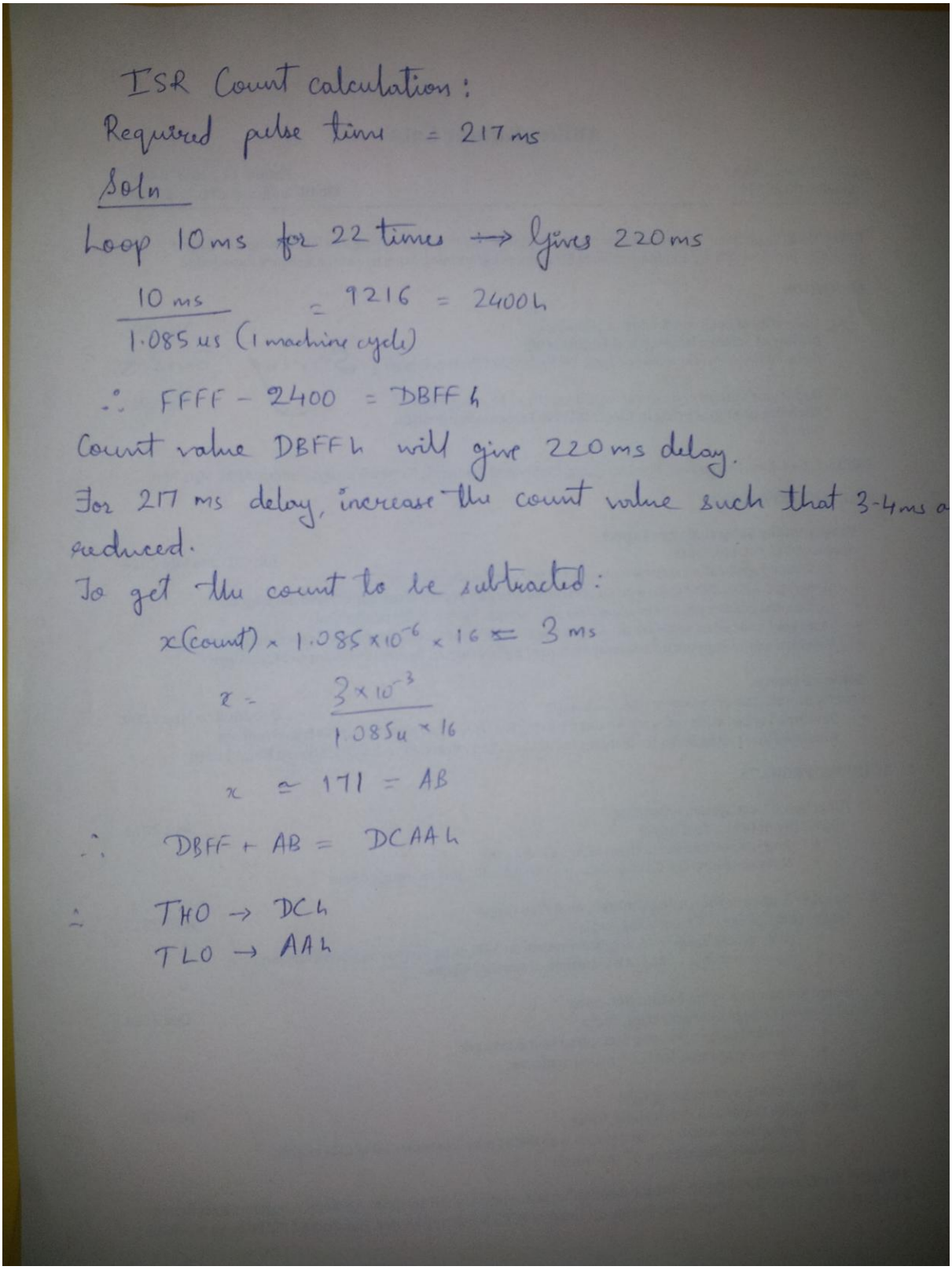
$V_{cc} - I_B R_B - V_{BE} = 0$

$5 - 248.48\mu R_B - 0.7 = 0$

$R_B = 17.3\,k\Omega$

$\therefore$ $\boxed{R_B = 18\,k\Omega}$ Standard Value.

ISR Count Calculation:



ISR Count calculation:

Required pulse time = 217 ms

Soln

Loop 10 ms for 22 times → gives 220 ms

$$\frac{10\text{ ms}}{1.085\text{ us (1 machine cycle)}} = 9216 = 2400_h$$

$\therefore$ FFFF − 2400 = DBFF h

Count value DBFFh will give 220 ms delay.

For 217 ms delay, increase the count value such that 3-4ms a reduced.

To get the count to be subtracted:

$$x(\text{count}) \times 1.085 \times 10^{-6} \times 16 = 3\text{ ms}$$

$$x = \frac{3 \times 10^{-3}}{1.085u \times 16}$$

$$x \simeq 171 = AB$$

$\therefore$ DBFF + AB = DCAA h

$\therefore$ TH0 → DCh

TL0 → AAh