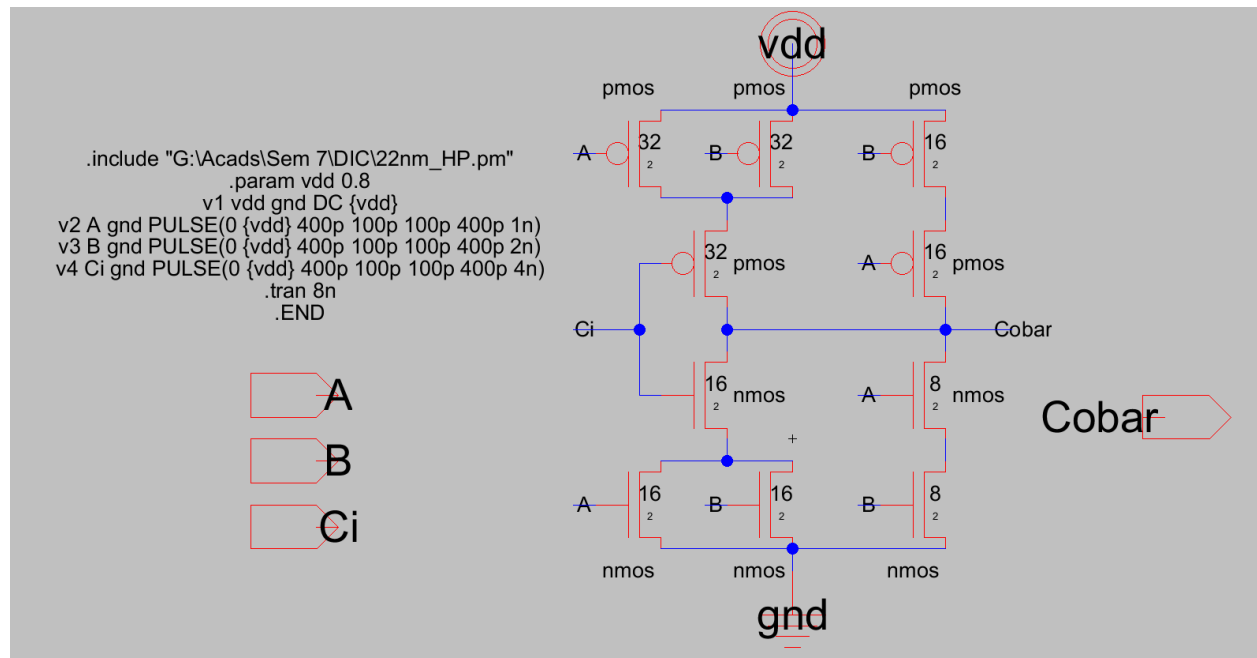
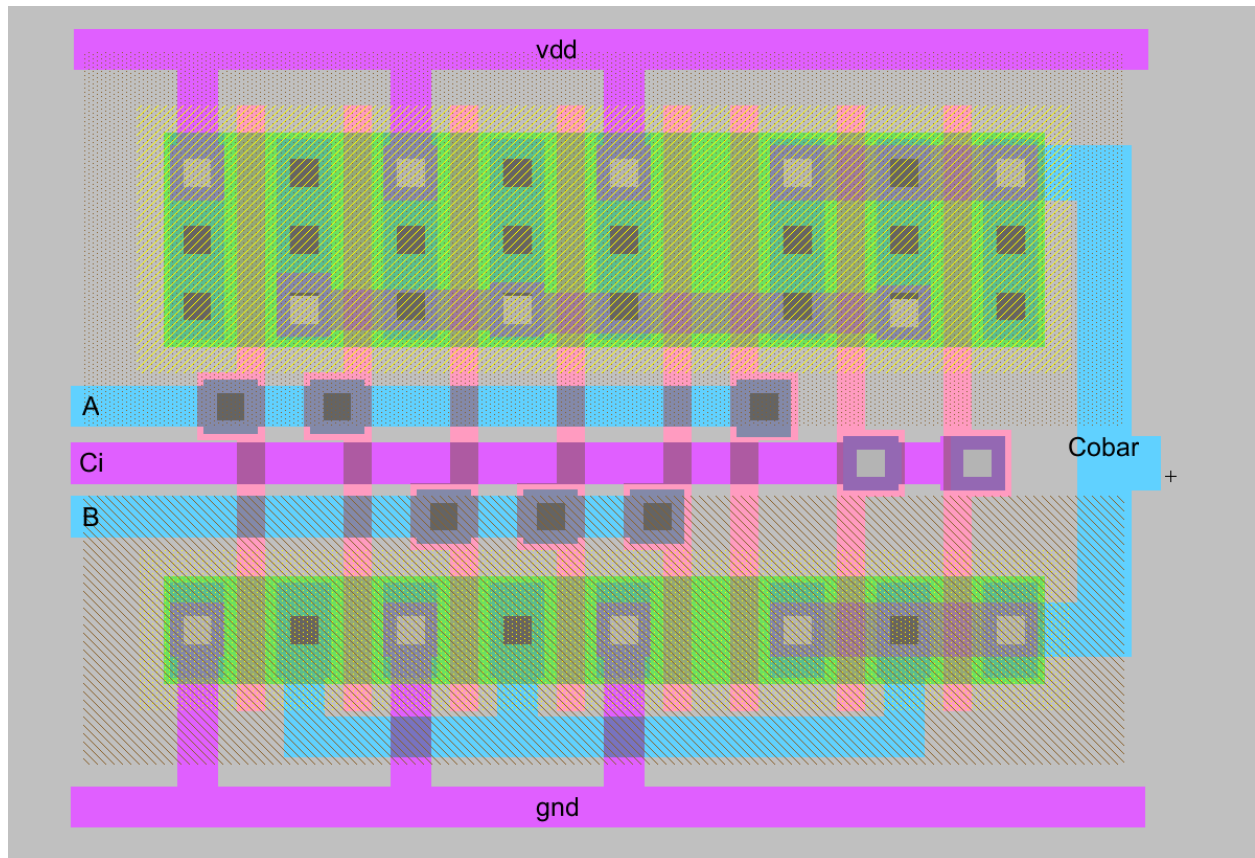


Schematic of 2X CARRY OUT circuit



Layout of 2X CARRY OUT circuit



DRC and LVS results

```
Electric Messages
=====20=====
Running DRC with area bit on, extension bit on, Mosis bit
Checking again hierarchy .... (0.0 secs)
Found 27 networks
0 errors and 0 warnings found (took 0.01 secs)
=====21=====
Hierarchical NCC every cell in the design: cell 'CarryOut:CarryOut{sch}' cell 'CarryOut:CarryOut{lay}'
Comparing: CarryOut:CarryOut{sch} with: CarryOut:CarryOut{lay}
  exports match, topologies match, sizes not checked in 0.01 seconds.
Summary for all cells: exports match, topologies match, sizes not checked
NCC command completed in: 0.01 seconds.
```

Simulation in SPICE to show correct functionality across all input combinations

