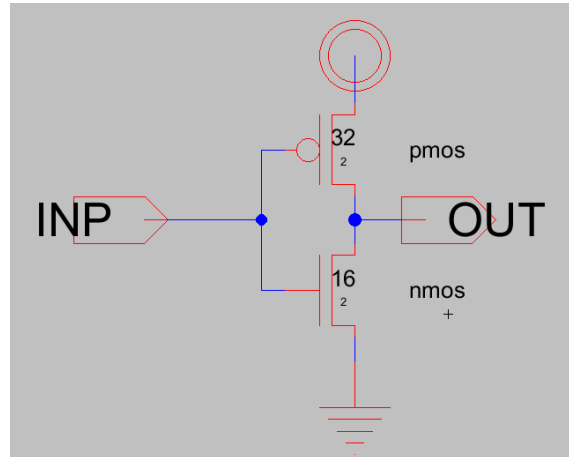
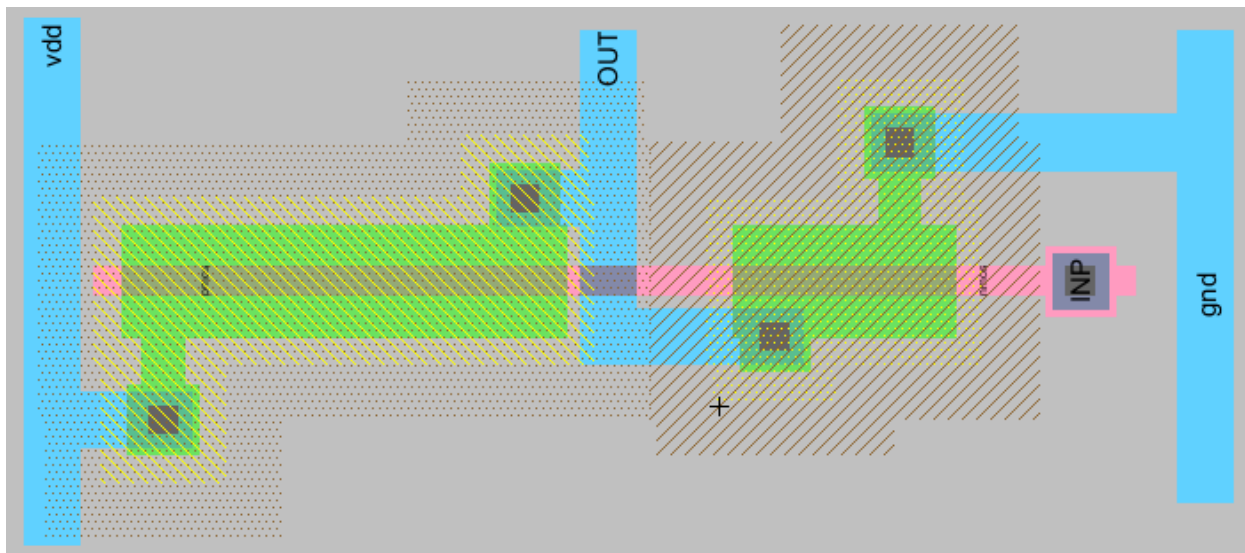


Inverter

Schematic



Layout

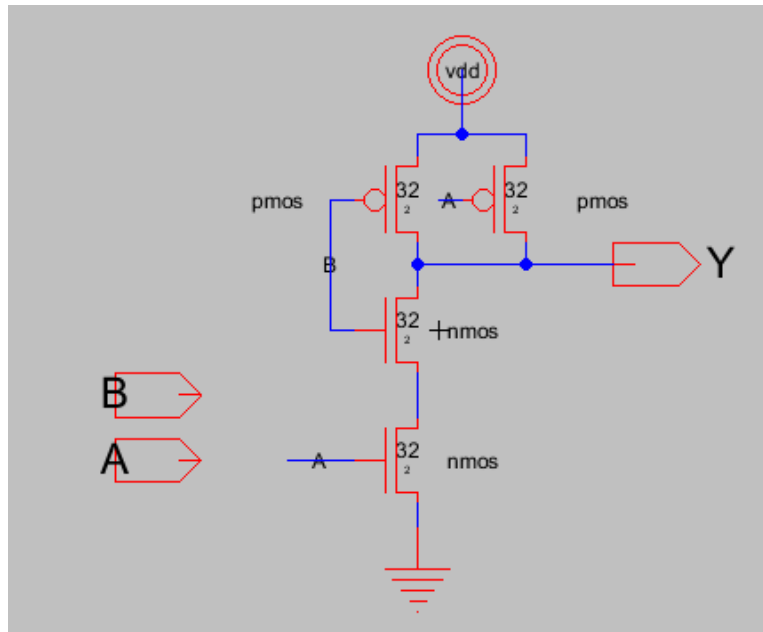


DRC and LVS

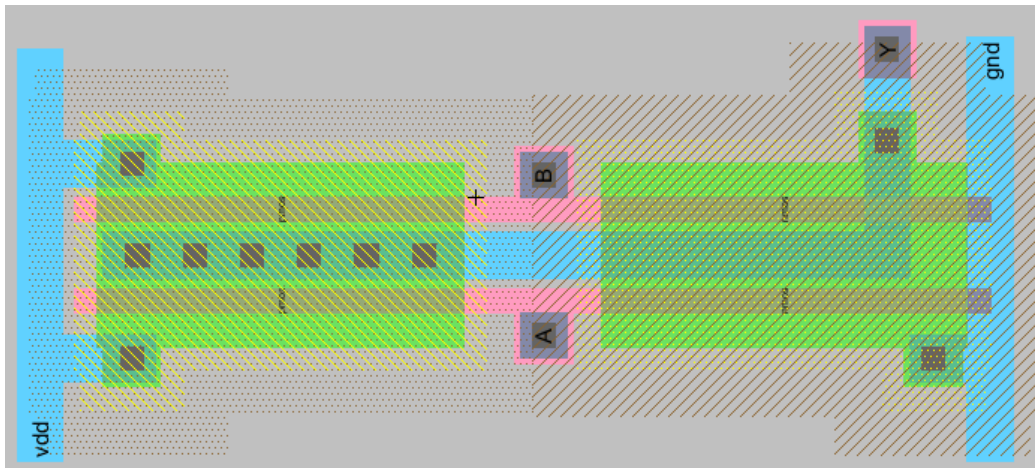
```
Electric Messages
=====2280=====
Running DRC with area bit on, extension bit on, Mosis bit
Checking again hierarchy .... (0.0 secs)
Found 7 networks
0 errors and 0 warnings found (took 0.0 secs)
=====2281=====
Hierarchical NCC every cell in the design: cell 'inverter-assignment:inverter{sch}' cell 'inverter-assignment:inverter{lay}'
Comparing: inverter-assignment:inverter{sch} with: inverter-assignment:inverter{lay}
  exports match, topologies match, sizes not checked in 0.0 seconds.
Summary for all cells: exports match, topologies match, sizes not checked
NCC command completed in: 0.0 seconds.
```

NAND2_4X

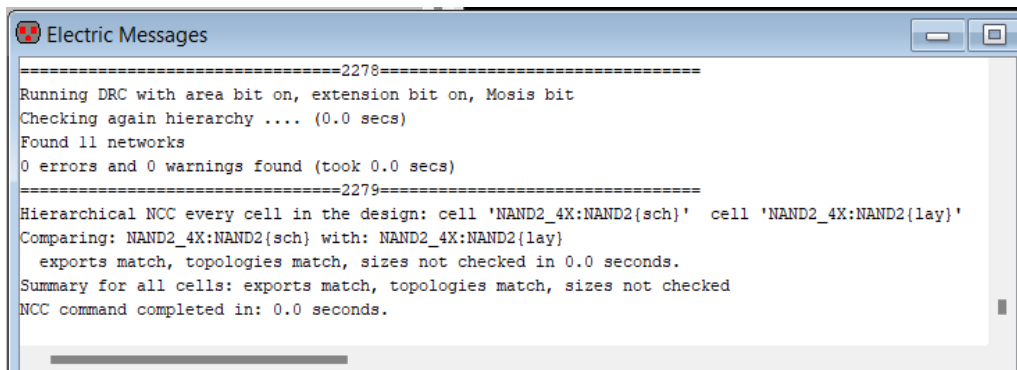
Schematic



Layout

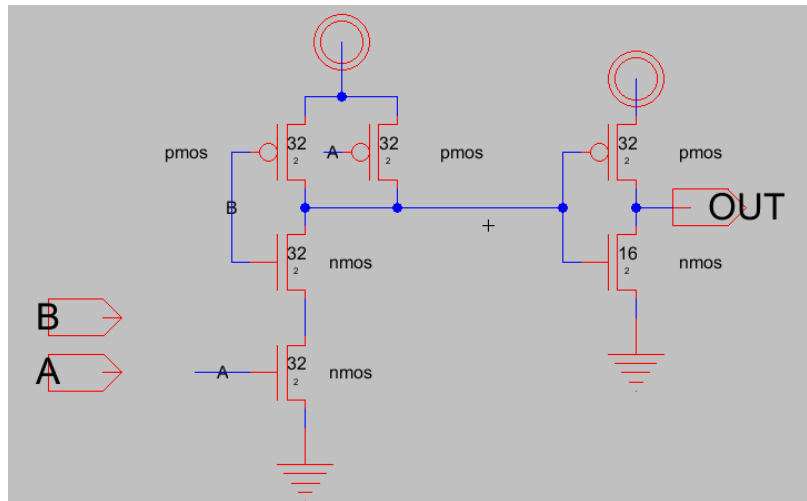


DRC and LVS

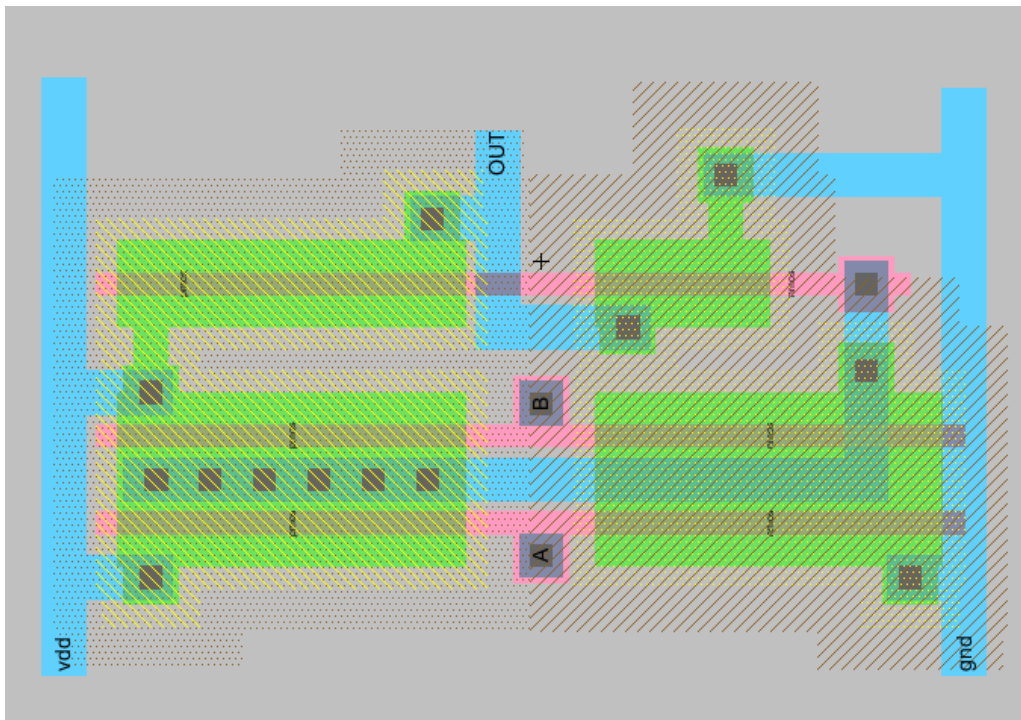


AND2

Schematic



Layout

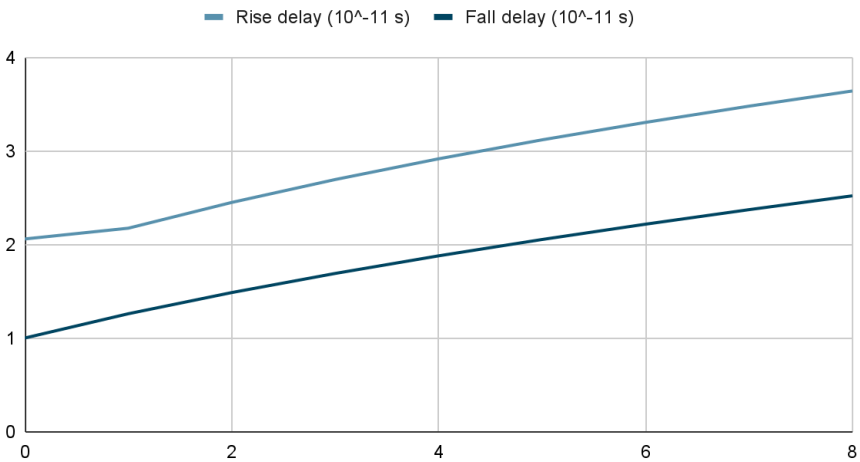


DRC and LVS

```
Electric Messages
=====2225=====
Running DRC with area bit on, extension bit on, Mosis bit
Checking again hierarchy .... (0.0 secs)
Found 14 networks
0 errors and 0 warnings found (took 0.0 secs)
=====2226=====
Hierarchical NCC every cell in the design: cell 'AND2{sch}' cell 'AND2{lay}'
Comparing: AND2:AND2{sch} with: AND2:AND2{lay}
exports match, topologies match, sizes not checked in 0.0 seconds.
Summary for all cells: exports match, topologies match, sizes not checked
NCC command completed in: 0.0 seconds.
```

Rise and fall delay of NAND2_4X gate

Fanout	Rise delay (10 ⁻¹¹ s)	Fall delay (10 ⁻¹¹ s)
0	2.06071	1.0025
1	2.17558	1.26178
2	2.45083	1.48809
3	2.69543	1.69239
4	2.9169	1.88045
5	3.11938	2.05494
6	3.30582	2.2185
7	3.47917	2.37359
8	3.64141	2.52164



Schematic

