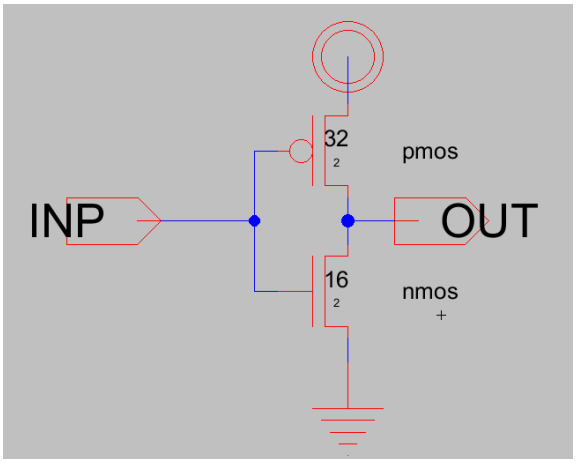
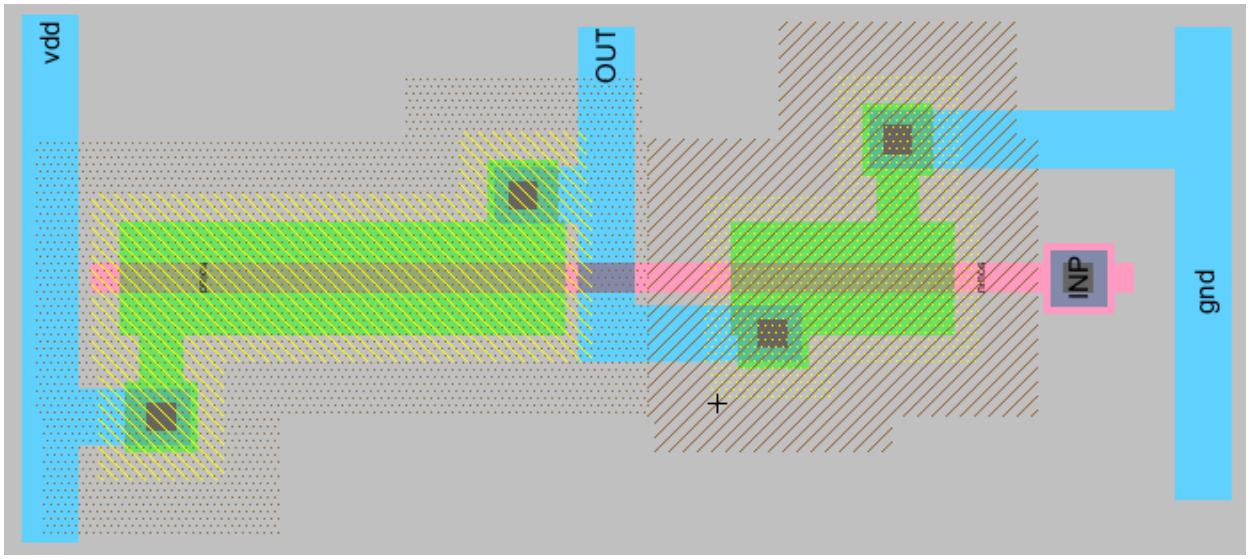
Inverter

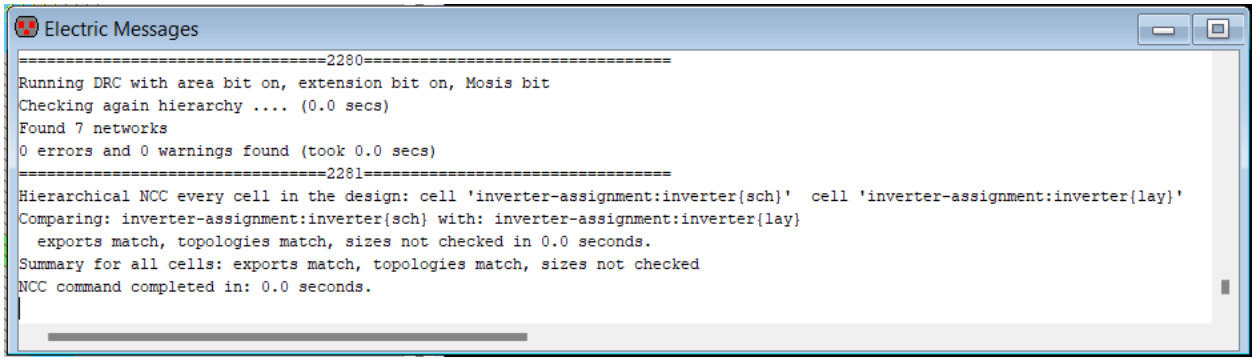
Schematic



Layout

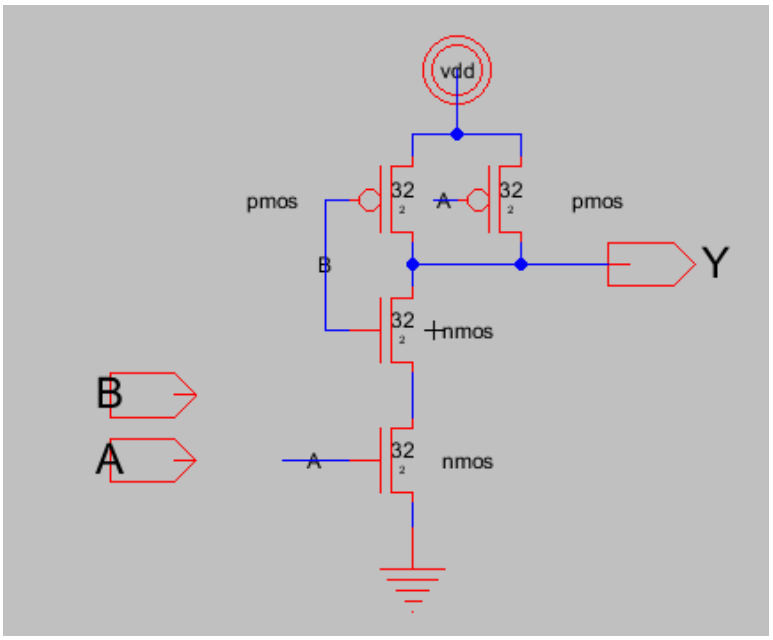


DRC and LVS

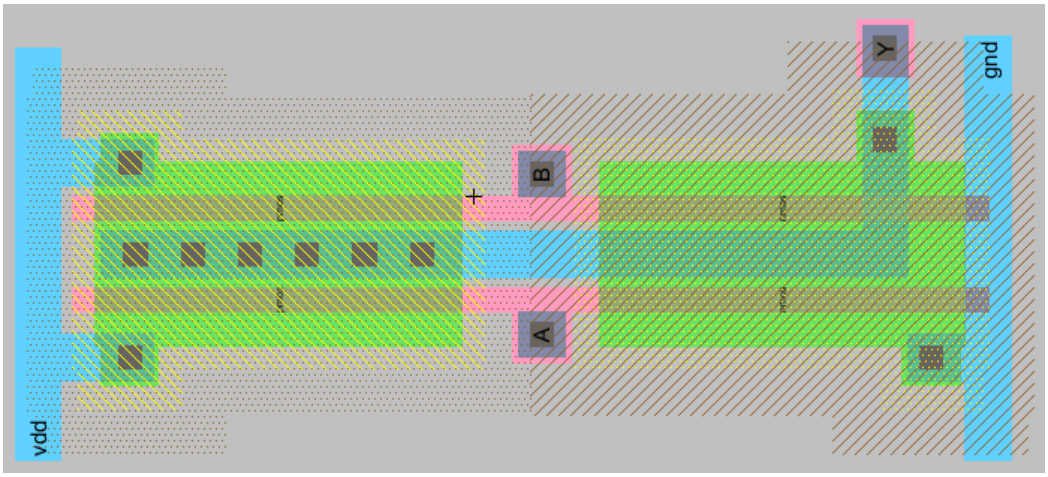


NAND2_4X

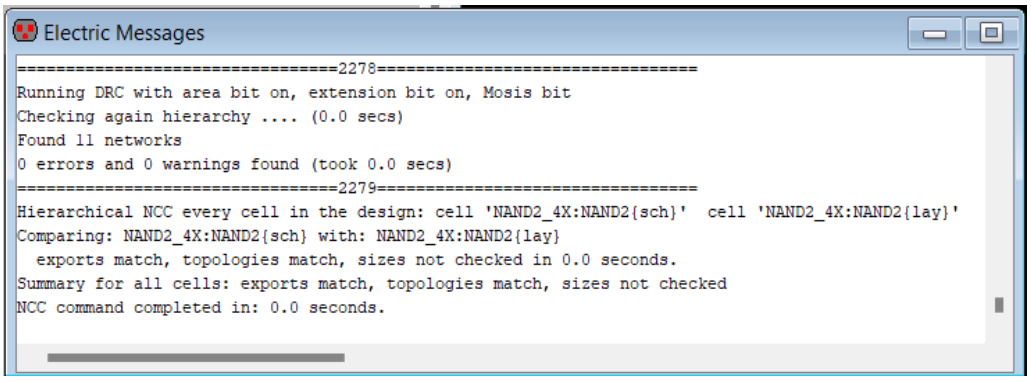
Schematic



Layout

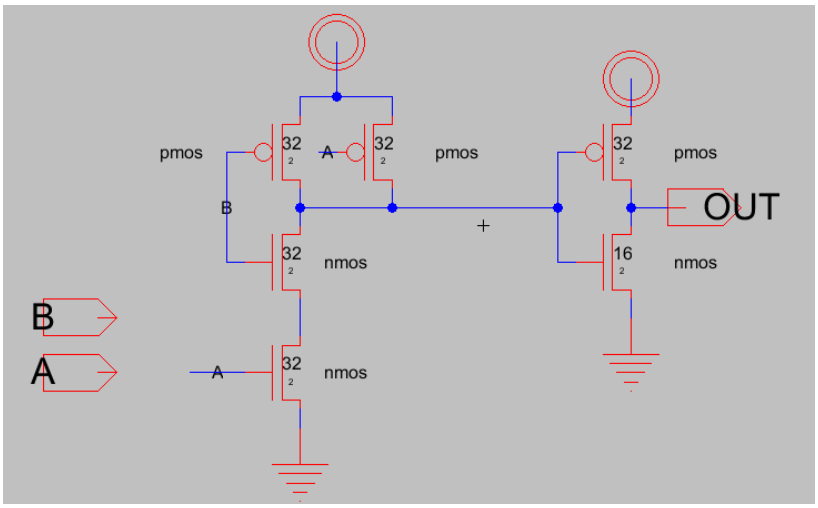


DRC and LVS

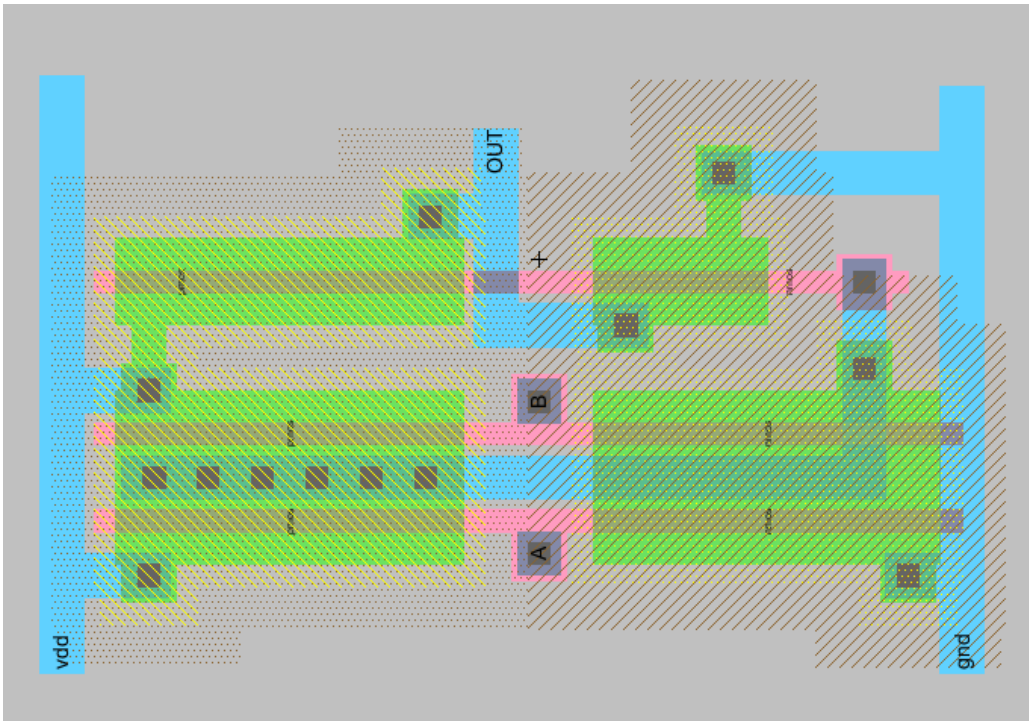


AND2

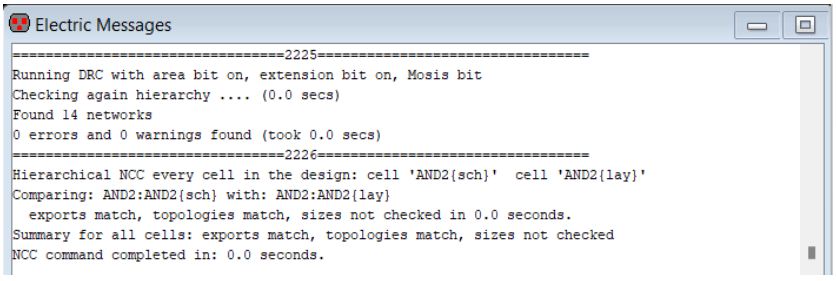
Schematic



Layout

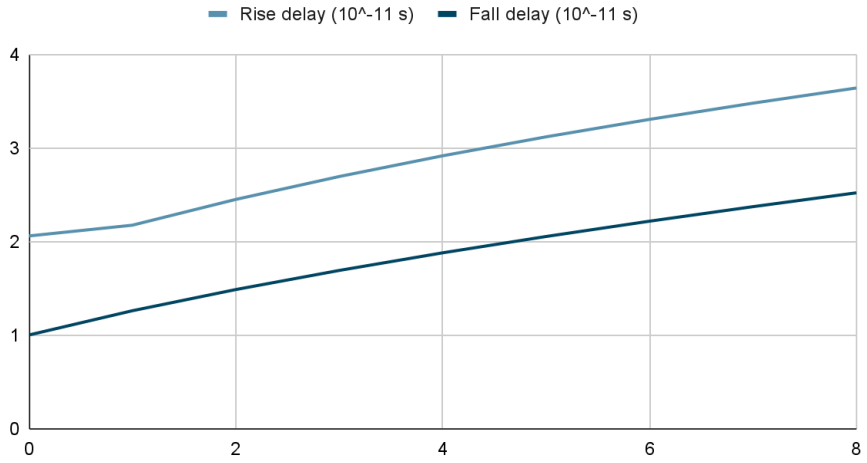


DRC and LVS



Rise and fall delay of NAND2_4X gate

Fanout	Rise delay (10^-11 s)	Fall delay (10^-11 s)
0	2.06071	1.0025
1	2.17558	1.26178
2	2.45083	1.48809
3	2.69543	1.69239
4	2.9169	1.88045
5	3.11938	2.05494
6	3.30582	2.2185
7	3.47917	2.37359
8	3.64141	2.52164



Schematic