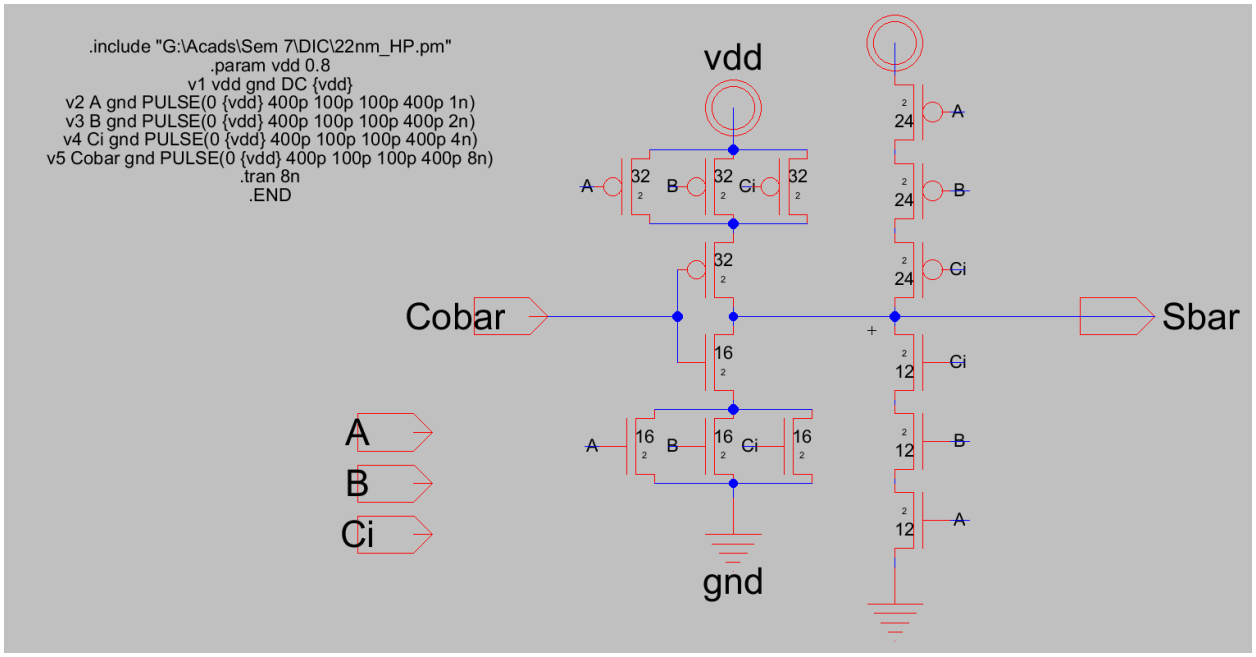
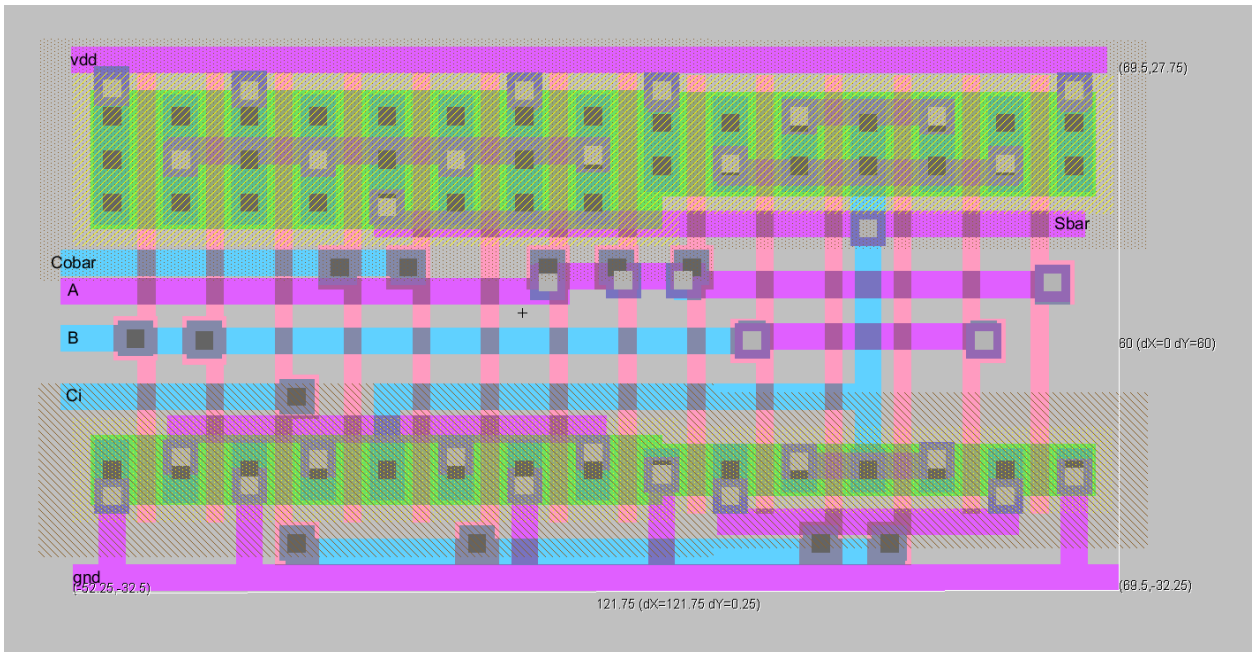
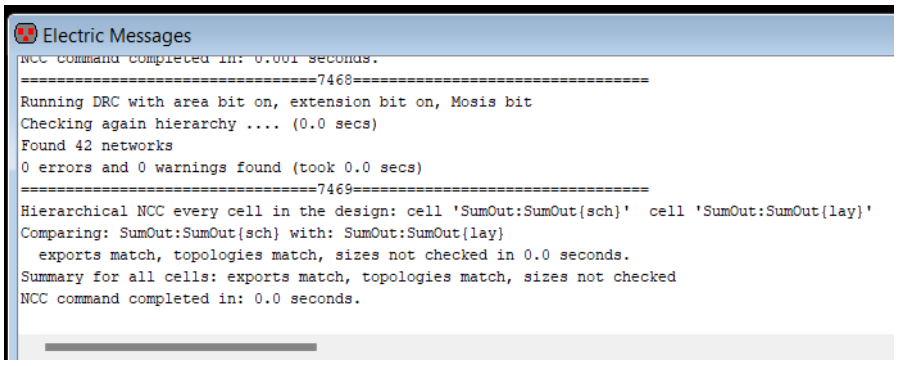
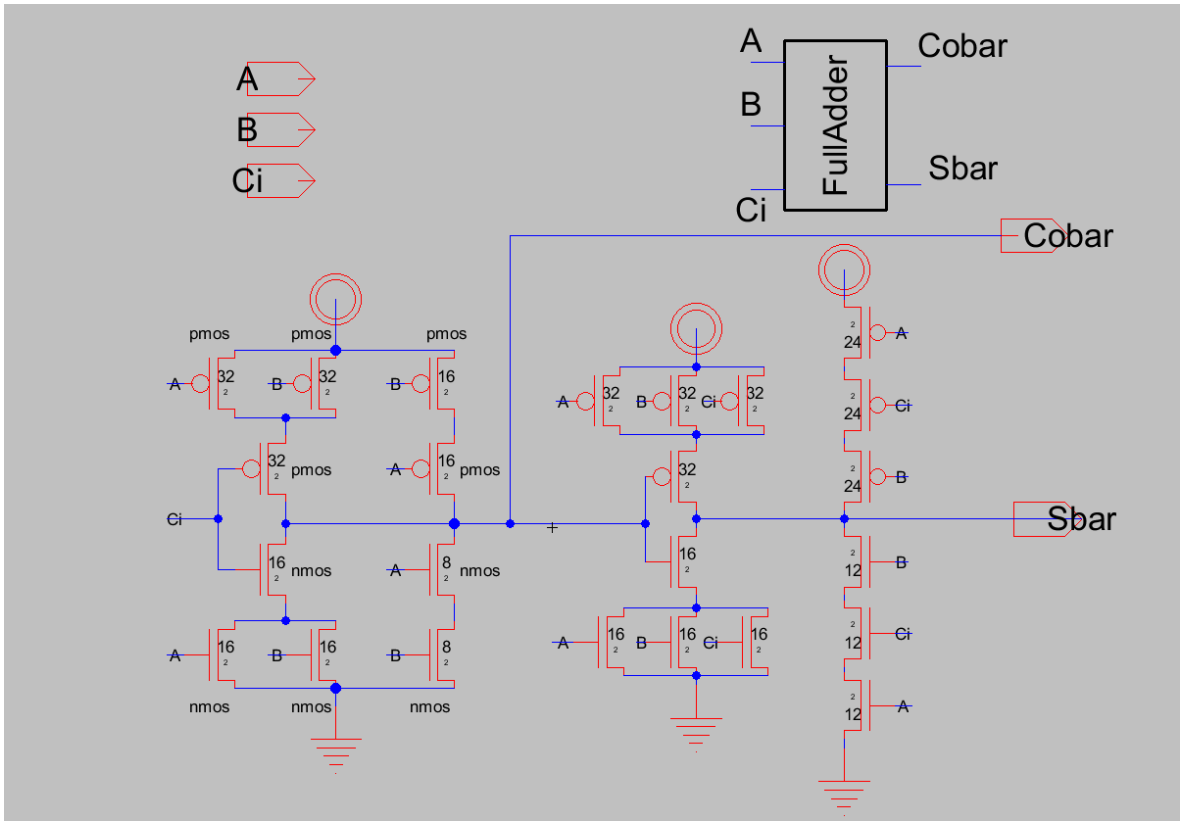
Schematic and Layout of 2X Sum part

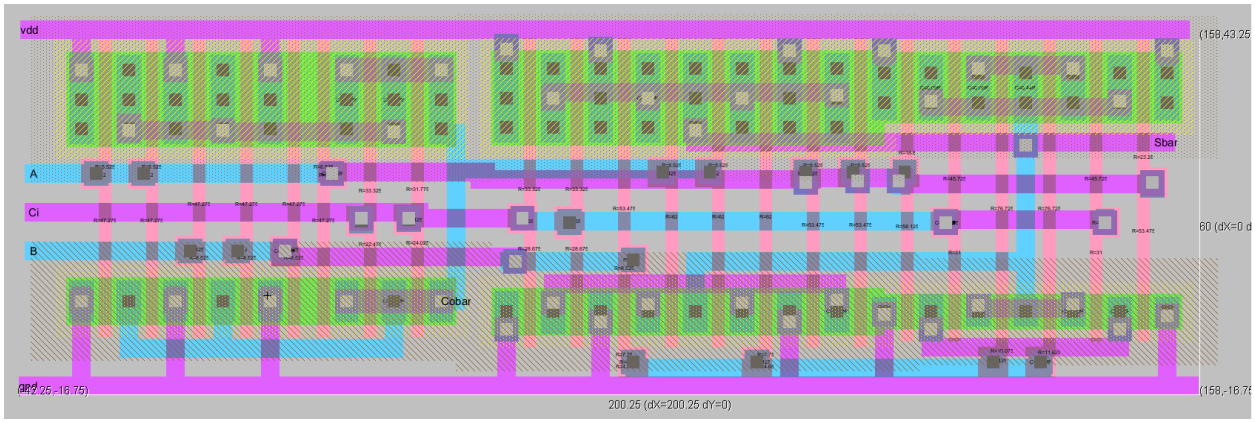






Schematic and Layout of Full Adder

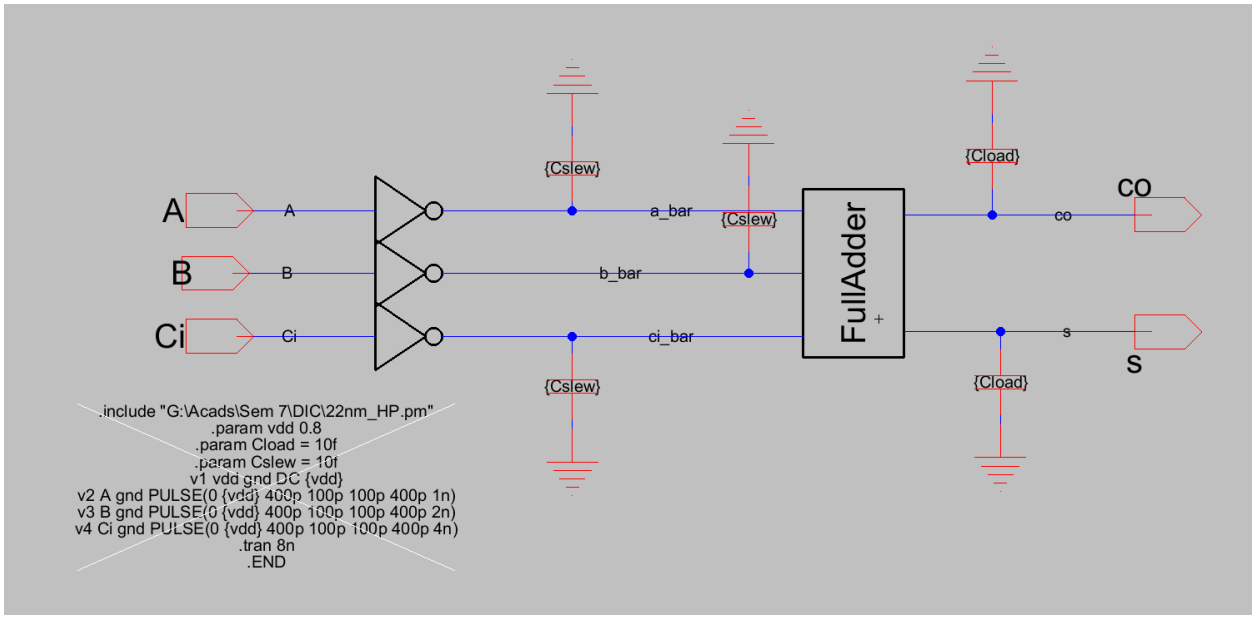




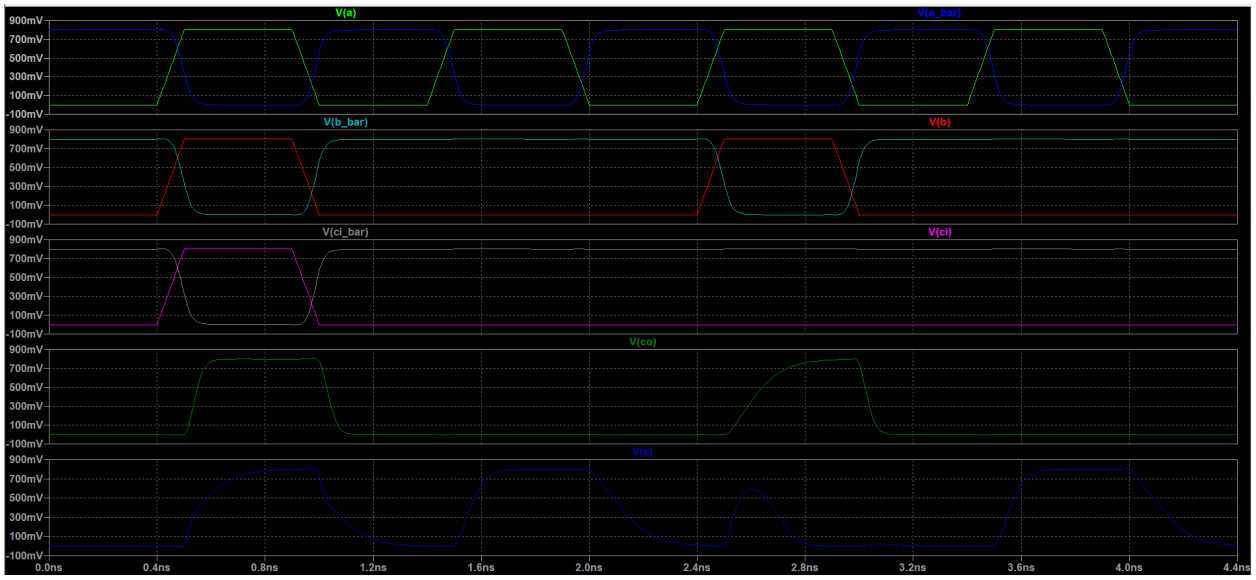

```
================================7479================================
Running DRC with area bit on, extension bit on, Mosis bit
Checking again hierarchy .... (0.0 secs)
Found 62 networks
Checking cell 'FullAdder:FullAdder{lay}'
================================7480================================
Hierarchical NCC every cell in the design: cell 'FullAdder:FullAdder{sch}'  cell 'FullAdder:FullAdder{lay}'
Comparing: FullAdder:FullAdder{sch} with: FullAdder:FullAdder{lay}
  exports match, topologies match, sizes not checked in 0.0 seconds.
Summary for all cells: exports match, topologies match, sizes not checked
NCC command completed in: 0.0 seconds.
        No errors/warnings found
0 errors and 0 warnings found (took 0.56 secs)
```

SPICE Simulation showing correct functionality of the adder for input and load capacitances as 10fF

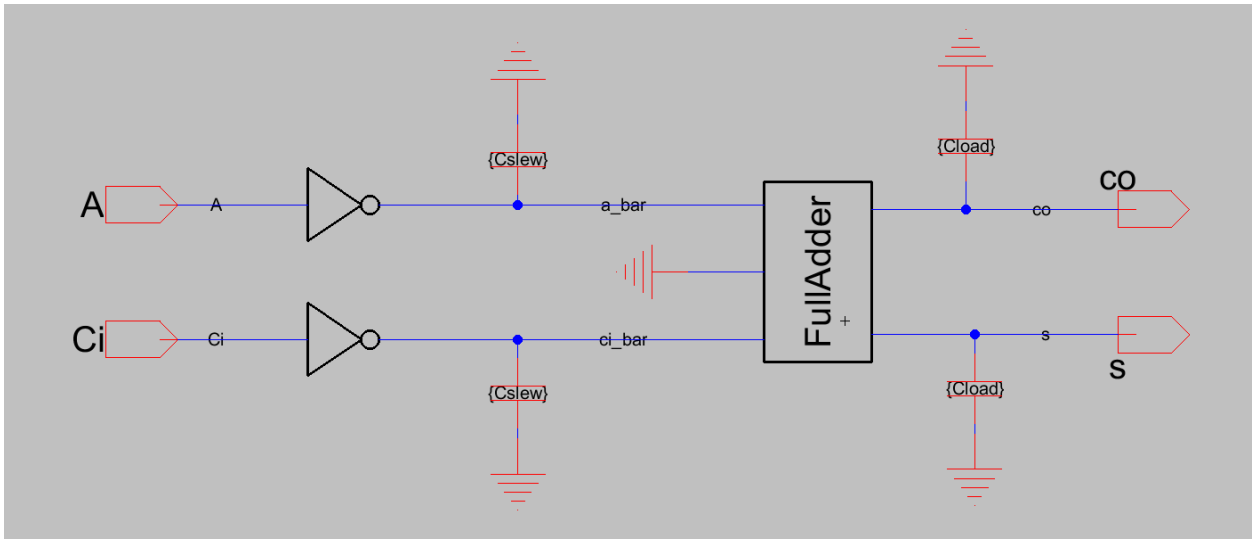
Schematic:



Output:



SPICE Simulation showing functionality of the adder for different input and output slews
Schematic:



Output:

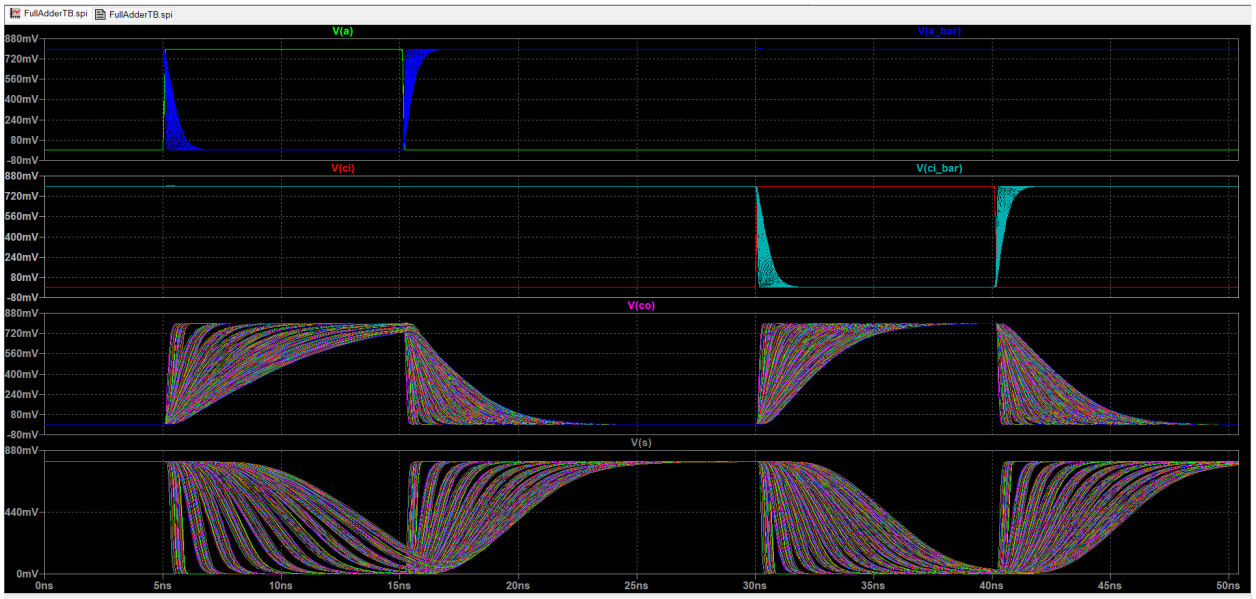


Table: Please find attached here:
https://docs.google.com/spreadsheets/d/1LuWbP5cpHO5kaWsmD9B9GLGgH1nXTOqOE8z0C96Hu4M/edit?usp=sharing