Aniketh Tarikonda

aniketh8@illinois.edu | aniketh ta.com | github.com/aniketh ta

Education

University of Illinois, Urbana-Champaign — Champaign, IL
Bachelor of Science in Computer Engineering, Minor in Physics — Expected Dec. 2027

- Honors: James Scholar, Dean's List (Fall 2024–Present), Member of IEEE-HKN Alpha Chapter
- Cumulative GPA: 3.97 / 4.00
- Relevant Coursework: Applied Parallel Programming (GPUs & CUDA), Digital Systems Laboratory (FPGAs), Digital Signal Processing, Analog Signal Processing, Data Structures
- Planned Coursework: Computer Organization and Design, Intro to VLSI System Design (Cadence Virtuoso/Innovus)

Experience

Eco Illini Supermileage — Champaign, IL
Electrical/Firmware Lead — Aug. 2024 – Present

- Leading an interdisciplinary team of 20+ engineers to design, verify, and integrate electrical systems for new generations of electric vehicles.
- Designed schematics and PCBs for 3+ custom boards, including a power distribution unit and battery management system, following automotive standards (e.g., SAE J1939).
- Programmed custom STM32 microcontroller-based boards with firmware supporting SPI, UART, and CAN communication protocols.
- Validated hardware on 2+ boards, achieving reliable data transmission rates exceeding 99%.
- Mentoring new members in automotive systems, embedded systems, and concepts in electrical engineering.

ResearchBase Inc. — Pleasanton, CA
Software Engineering Intern — July 2025 – Aug. 2025

- Built a ResearchCopilot prototype with a real-time conversational pipeline integrating automatic speech recognition (ASR) and analytics to surface insights dynamically.
- Improved document parsing accuracy by integrating LandingAI Agentic Document Extraction (ADE) APIs for structured data extraction.
- Developed a text-to-image generation feature using ChatGPT image APIs, converting natural language prompts into visuals.

Projects

FPGA Flight Simulator with 3D Rendering (Ongoing)

- Designed and implemented a hardware-accelerated flight simulator on the RealDigital Urbana board using SystemVerilog, featuring a custom GPU pipeline, DDR3 memory interfaces, and real-time 3D graphics rendering to a HDMI display.
- Developed a MicroBlaze-driven control subsystem to process keyboard inputs and transmit graphics data to the hardware GPU pipeline over AXI interface(s).

GPT-2 Transformer Model Implementation (Ongoing)

- Implementing core components of the GPT-2 transformer model in CUDA—including the attention mechanism, encoder layers, and layer normalization—optimized for GPU parallelism.
- Implemented optimizations to improve inferencing performance, including but not limited to KV-caching, reduction trees, and leveraging tensor-core-accelerated matrix operations.
- Deploying a custom GPT-2 inference pipeline on NCSA's Delta HPC cluster, leveraging high-throughput compute nodes and NVIDIA Nsight Compute for performance profiling.

Technical Skills

Languages: SystemVerilog, Verilog, C/C++, Python, Java, CUDA, JavaScript, bash
Tools: Vivado, Vitis, Verilator, STM32CubeIDE, Postman, Linux, Altium Designer, KiCAD, Jira, oscilloscopes, function generators, gdb, git
Libraries/Frameworks: NumPy, Node.js, React, Spring, PostgreSQL