

ANIKETH TARIKONDA

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EDUCATION

University of Illinois, Urbana-Champaign

Bachelor of Science in Computer Engineering, Minor in Physics

Champaign, IL

Expected Dec. 2027

- Honors: James Scholar, Dean's List (Fall 2024–Present), Member of IEEE-HKN Alpha Chapter
- Cumulative GPA: 3.96 / 4.00
- Relevant Coursework: Computer Organization and Design (**Computer Architecture**, **Synopsys Verdi/VCS**), Intro to VLSI System Design (**Cadence Virtuoso/Innovus**), Applied Parallel Programming (**GPU Architecture & CUDA**), Digital Systems Laboratory (**FPGAs**), Digital Signal Processing, Analog Signal Processing, Data Structures

EXPERIENCE

Eco Illini Supermileage

Electrical/Firmware Lead

Champaign, IL

Aug. 2024 – Present

- Leading an interdisciplinary team of 20+ engineers to design, verify, and integrate electrical systems for new generations of electric vehicles.
- Designed schematics and PCBs for 3+ custom boards, including a power distribution unit and battery management system, following automotive standards (e.g., SAE J1939).
- Programmed custom STM32 microcontroller-based boards with firmware supporting SPI, UART, and CAN communication protocols.
- Validated hardware on 2+ boards, achieving reliable data transmission rates exceeding 99%.
- Mentoring new members in automotive systems, embedded systems, and concepts in electrical engineering.

ResearchBase Inc.

Software Engineering Intern

Pleasanton, CA

July 2025 – Aug. 2025

- Built a ResearchCopilot prototype with a real-time conversational pipeline integrating automatic speech recognition (ASR) and analytics to surface insights dynamically.
- Improved document parsing accuracy by integrating LandingAI Agentic Document Extraction (ADE) APIs for structured data extraction.
- Developed a text-to-image generation feature using ChatGPT image APIs, converting natural language prompts into visuals.

PROJECTS

FPGA Flight Simulator with 3D Rendering

- Designed and implemented a hardware-accelerated flight simulator on the RealDigital Urbana board using SystemVerilog, featuring a custom graphics pipeline, DDR3 SDRAM interfaces, and real-time 3D graphics rendering to a HDMI display.
- Developed a MicroBlaze-driven control subsystem to process keyboard inputs and transmit object data to the hardware GPU pipeline over GPIO interface(s).

GPT-2 Transformer Model Implementation

- Implemented core components of the GPT-2 transformer model in CUDA—including the attention mechanism, encoder layers, and layer normalization—optimized for GPU parallelism.
- Implemented optimizations to improve inferencing performance, including but not limited to KV-caching, reduction trees, and leveraging tensor-core-accelerated matrix operations.
- Deployed a custom GPT-2 inference pipeline on NCSA’s Delta HPC cluster, leveraging NVIDIA Nsight Compute and Nsight Systems for kernel and system-level profiling, respectively.

TECHNICAL SKILLS

Languages: SystemVerilog, Verilog, C/C++, Python, CUDA, RISC-V, bash, Java, Javascript

Tools: Synopsys VCS, Verdi, Design Compiler, Cadence Virtuoso, Innovus, Calibre, Vivado, Vitis, Verilator, STM32CubeIDE, Linux, Altium Designer, KiCAD, Jira, oscilloscopes, function generators, gdb, git

Libraries/Frameworks: NumPy, Node.js, React, Spring, PostgreSQL