Aniketh Tarikonda

aniketh8@illinois.edu | aniketh ta.com | github.com/aniketh ta

Education

University of Illinois, Urbana-Champaign — Champaign, IL
Bachelor of Science in Computer Engineering, Minor in Physics — Expected Dec. 2027

- Honors: James Scholar, Dean's List (Fall 2024–Present), IEEE-HKN Honor Society
- Cumulative GPA: 3.97 / 4.00
- Relevant Coursework: Applied Parallel Programming (GPUs & CUDA), Digital Systems Laboratory (FPGAs), Digital Signal Processing, Analog Signal Processing, Data Structures
- Planned Coursework: Computer Organization and Design, Intro to VLSI System Design

Experience

Eco Illini Supermileage — Champaign, IL
Electrical Lead — May 2025 – Present

- Lead an interdisciplinary team of 20+ engineers to design and integrate electrical systems for new generations of electric vehicles.
- Mentor new members in automotive systems, embedded systems, and electrical design best practices.

Electrical/Firmware Engineer — Aug. 2024 – May 2025

- Designed schematics and PCBs for 3+ custom boards, including a power distribution unit and battery management system, following automotive standards (e.g., J1939-17).
- Programmed STM32-based microcontrollers with firmware supporting SPI, UART, and CAN communication protocols.
- Validated hardware on 2+ boards, achieving reliable data transmission rates exceeding 99%.

ResearchBase Inc. — Pleasanton, CA
Software Engineering Intern — July 2025 – Aug. 2025

- Built a ResearchCopilot prototype with a real-time conversational pipeline integrating automatic speech recognition (ASR) and analytics to surface insights dynamically.
- Improved document parsing accuracy by integrating LandingAI Agentic Document Extraction (ADE) APIs for structured data extraction.
- Developed a text-to-image generation feature using ChatGPT image APIs, converting natural language prompts into visuals.

Alameda County IT Department — Oakland, CA
IT Intern — June 2022 – Aug. 2022

- Migrated 2000+ support requests between Axosoft and Atlassian Jira using RESTful APIs.
- Collaborated with multiple teams to ensure functionality parity and workflow continuity post-migration.

Projects

GPT-2 Transformer Implementation

- Implemented core components of the GPT-2 transformer model in CUDA, including encoder layers, GELU activation, and layer normalization, optimized for GPU parallelism.
- Deployed a custom GPT-2 inference pipeline on NCSA's Delta HPC cluster, leveraging high-throughput compute nodes for performance evaluation.

Technical Skills

Languages: SystemVerilog, Verilog, C/C++, Python, Java, CUDA, JavaScript
Tools/Frameworks: Vivado, Vitis, Verilator, STM32CubeIDE, Postman, Jira, git, REST APIs, Node.js