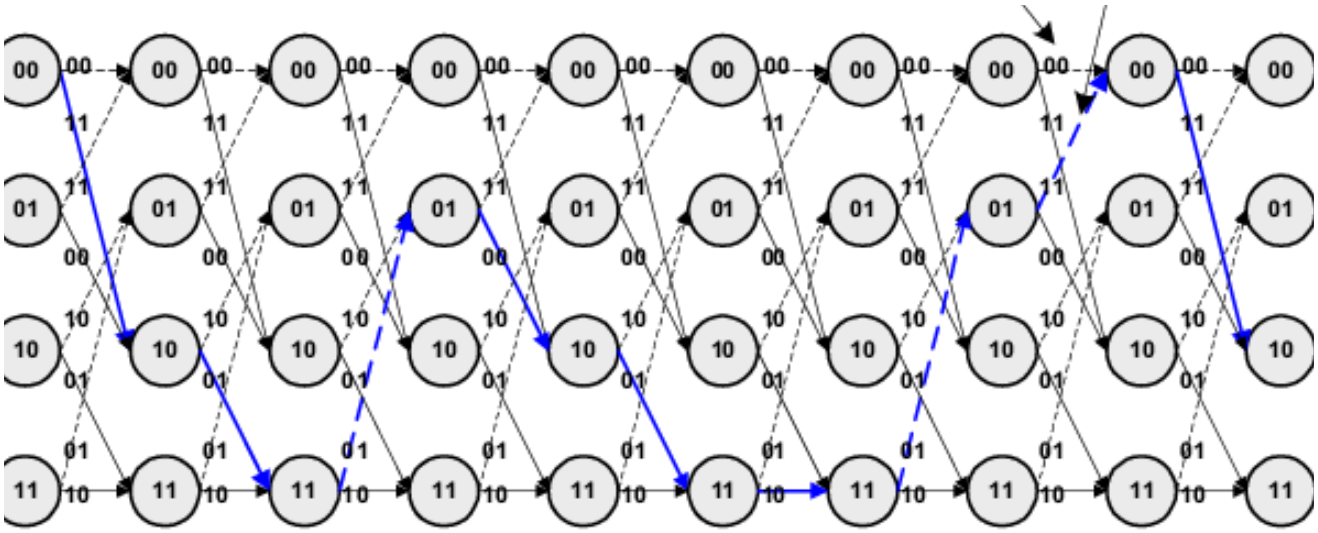
TRINIT HACKATHON – 2023

DE02 : Convolutional Code Communication System



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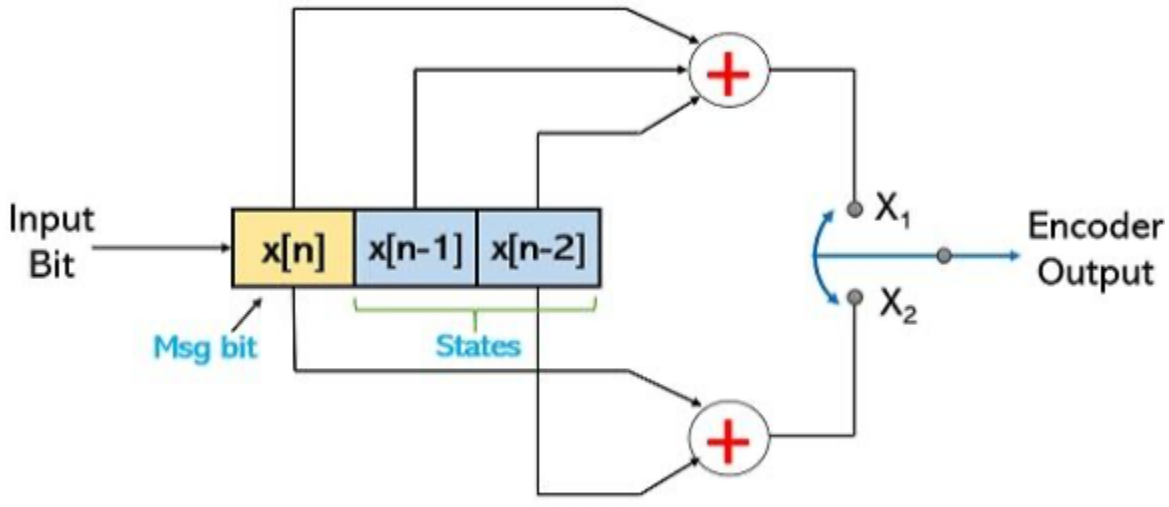
Problem Statement

Our problem statement is to design a digital communication system based on convolutional codes. The problem statement is divided into 3 parts:

1. Design a convolutional code encoder circuit.
2. Design a circuit that simulates channel noise to the transmitter.
3. Design a convolutional code decoder circuit using Viterbi's algorithm.

INTRODUCTION

Convolutional code is another type of error-correcting code called convolutional code, and it produces its output bits by executing a specified logical operation on a current bitstream while also taking certain bits from a preceding stream into account. Instead of relying on a block of bits, this coding style demonstrates a reliance on the bitstream.



Block Diagram for Convolutional Encoder

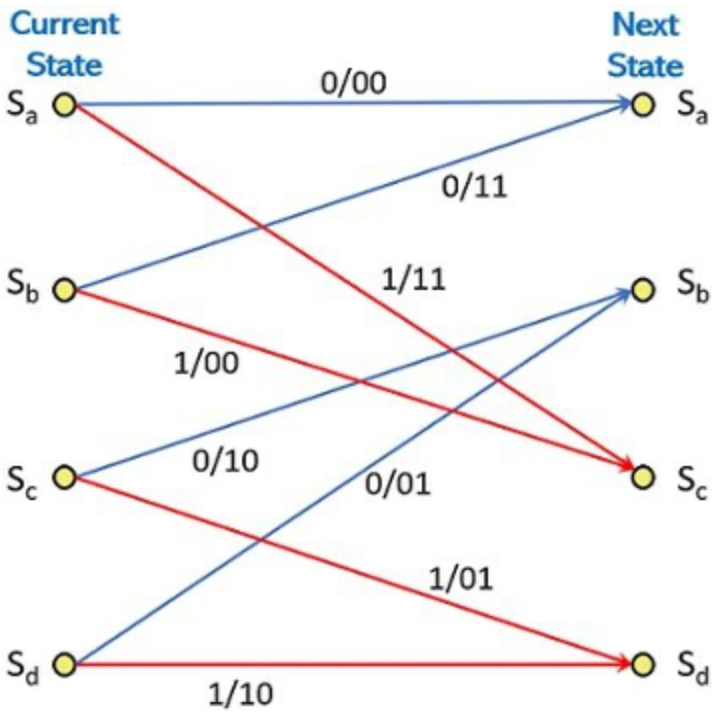
Trellis Diagram for Decoder

The trellis diagram is obtained by the state diagram

representation which is shown above. By using a trellis diagram one can efficiently decode the obtained code sequence.

Here we have marked the four current states and the next states, in the two columns. Each state of the current state column forms connections with 2 other states of the next state column according to the path in the state diagram representation. For input 0 the CS and NS, both are S_a resulting in output 00. Likewise, when input is 1, then CS and NS are S_a and S_c respectively. This combination provides output 11. In a similar way, when the input is 0, CS and NS will be S_b and S_a respectively, with the current state combinational output as 11.

Basically, for decoding operation, the decoder needs to determine the sequence of stream which actually generates the parity bit sequence which is received at the receiver. This is achieved by observing the best path through the trellis that provides the sequence of parity bits received.



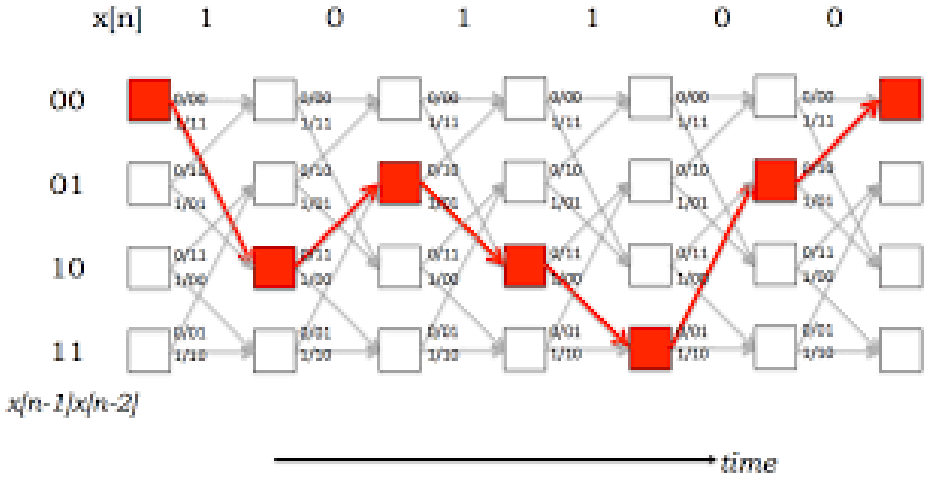
The above figure displays the state diagram which helps to determine the next state based on the current state and the input.

Viterbi Decoding Algorithm

The basic units of the Viterbi decoder are branch metrics, Add compare select and Survivor management unit. Viterbi decoder consist of three blocks: the branch metric unit (BMU), which computes metrics, the add–compare–select unit (ACSU), which selects the survivor paths for each trellis state, also finds the minimum path metric of the survivor paths and the survivor management unit (SMU), that is responsible for selecting the output based on the minimum path metric.

The Viterbi algorithm can be explained briefly with the following three steps.

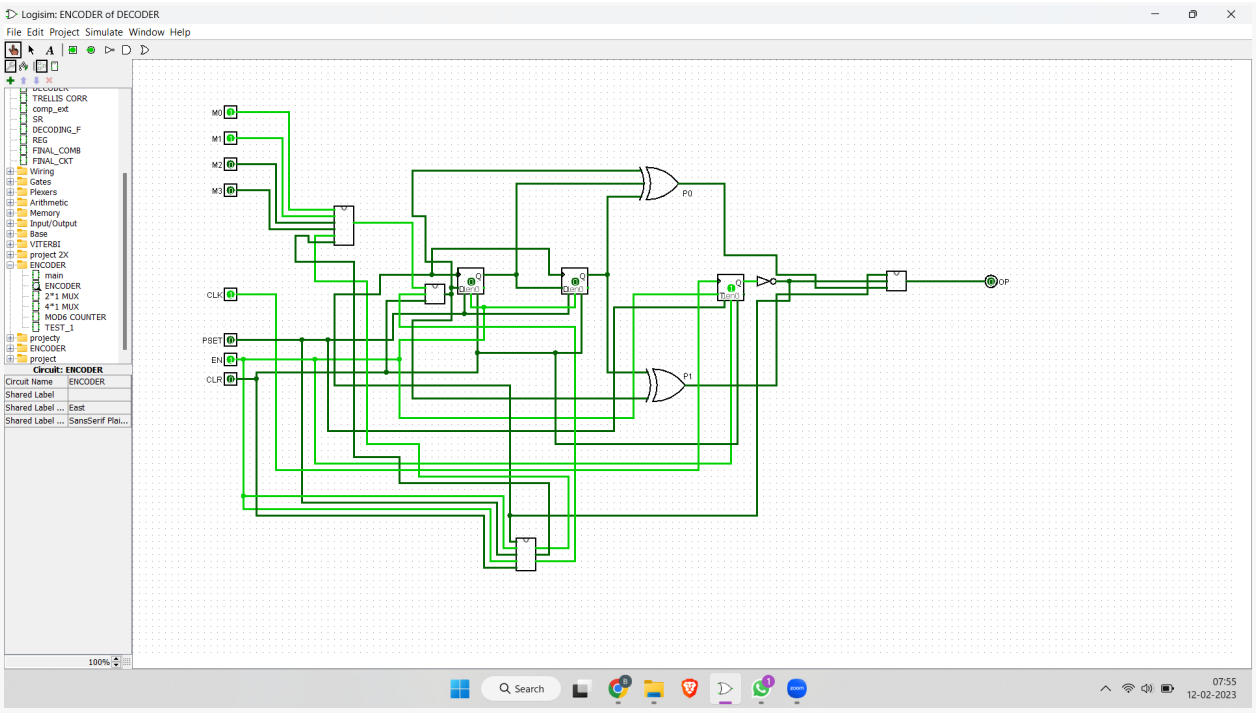
1. Weigh the trellis; that is, calculate the branch metrics.
2. Recursively computes the shortest paths to time n, in terms of the shortest paths to time n-1. In this step, decisions are used to recursively update the survivor path of the signal. This is known as add-compare-select (ACS) recursion.
3. Recursively finds the shortest path leading to each trellis state using the decisions from Step 2. The shortest path is called the survivor path for that state and the process is referred to as survivor path decode. Finally, if all survivor paths are traced back in time, they merge into a unique path, which is the most likely signal path.



Design

Channel Encoder Design:

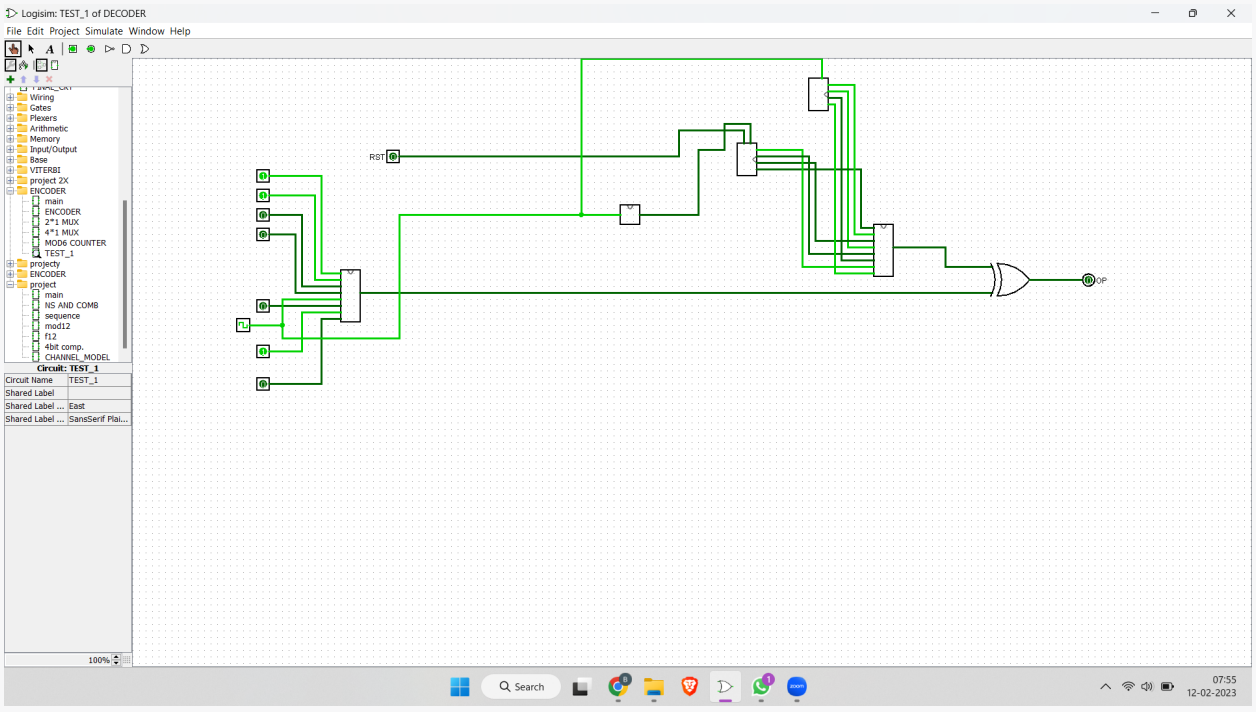
The design of a convolutional code encoder consists of multiplexors,shift registers (for generation of x[n-1] and x[n-2]) and a set of modulo-2 adders. The 4 bit input data is transformed to serial data using a multiplexor and we have appended two 0's at the end . The generated serial data is shifted through the shift register one bit at a time, and the contents of the record are used to generate multiple output streams, called code words(12 bits).



Noisy Channel Design:

The noisy channel has been designed to introduce an error in the code word received by the encoder. The noise channel consists of a Pseudo-noise encoder which introduces an error in the codeword received at the bit position which the

counter holds.The idea behind how we achieved this is that ,since we have serial data coming in. When first bit is received , we initialize an up counter which increments on the arrival of the next bit of the codeword, When the counter value matches with the value of current pn sequence counter, it flips that particular bit of the codeword. By this way, we are able to introduce a 1-bit error in the position specified by the sequence counter.

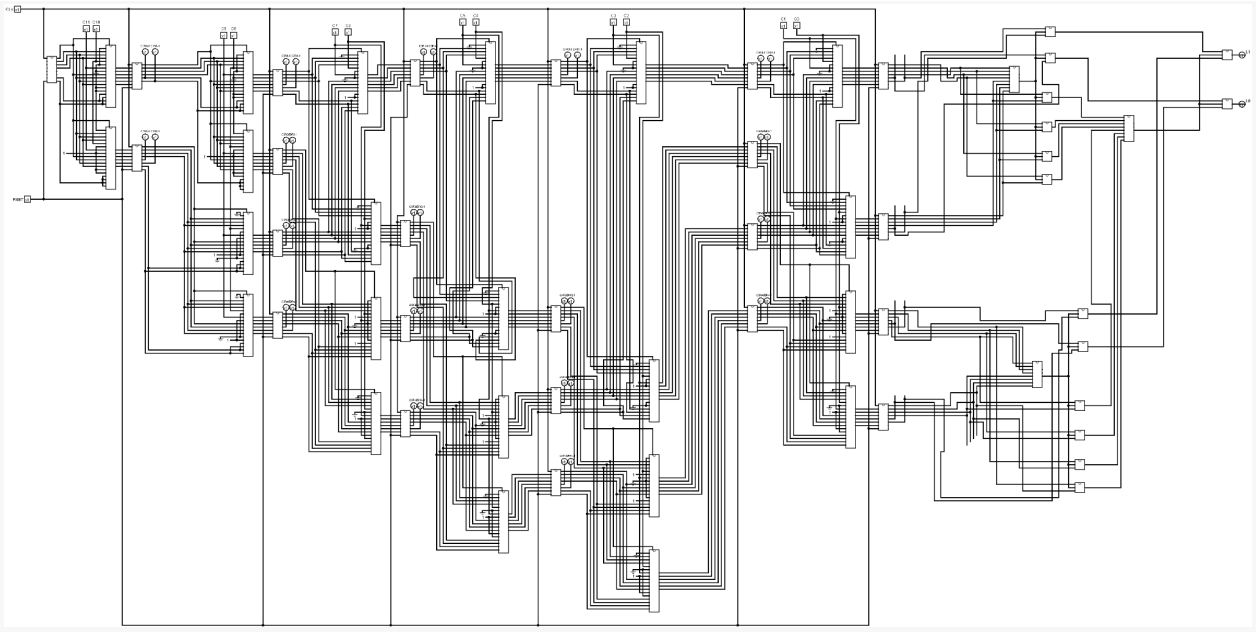


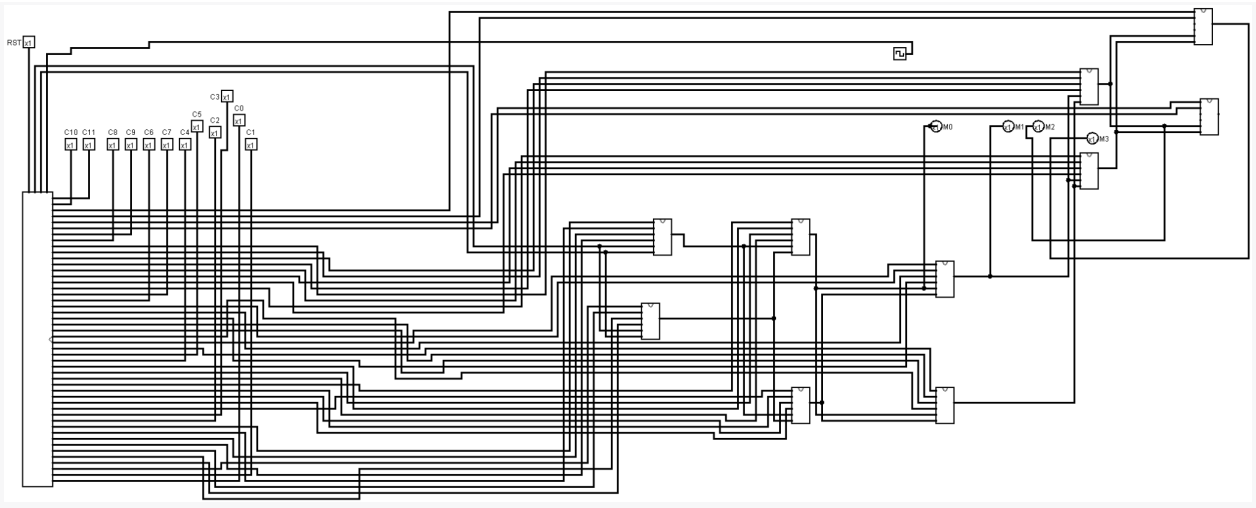
Design of the decoder:

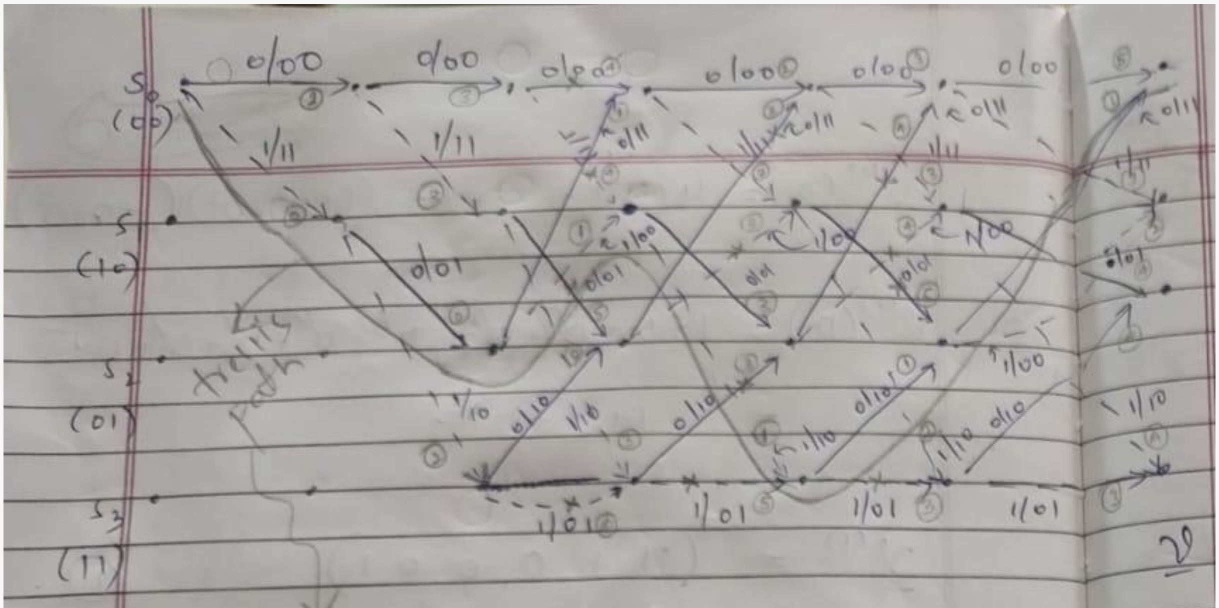
Basically we have tried to implement the Trellis path Viterbi's algorithm. From the transmitter, we receive the encoded word serially. So firstly we have tried to get all the 12 bits of codeword through a designed serial to the parallel shift register. The obtained parallel data is now used in the calculation of the least cumulative discrepancy.

Through forward propagation in the trellis tree structure, we will calculate the discrepancy involved in received 2bit from noisy channel and the output combination and in case of two paths to same node in Trellis tree we choose the path with the minimum cumulative discrepancy.Every state of each and every stages in the diagram is designed as a register that will hold the minimum cumulative discrepancy of all the discrepancies occurring from various paths

from previous stages, and also the state which produces this minimum discrepancy. We are storing the previous state so that backtracking to calculate the input code word at transmitter can be found very easily. Once we reach the end of all stages, we backtrace this path to find out the input pattern.







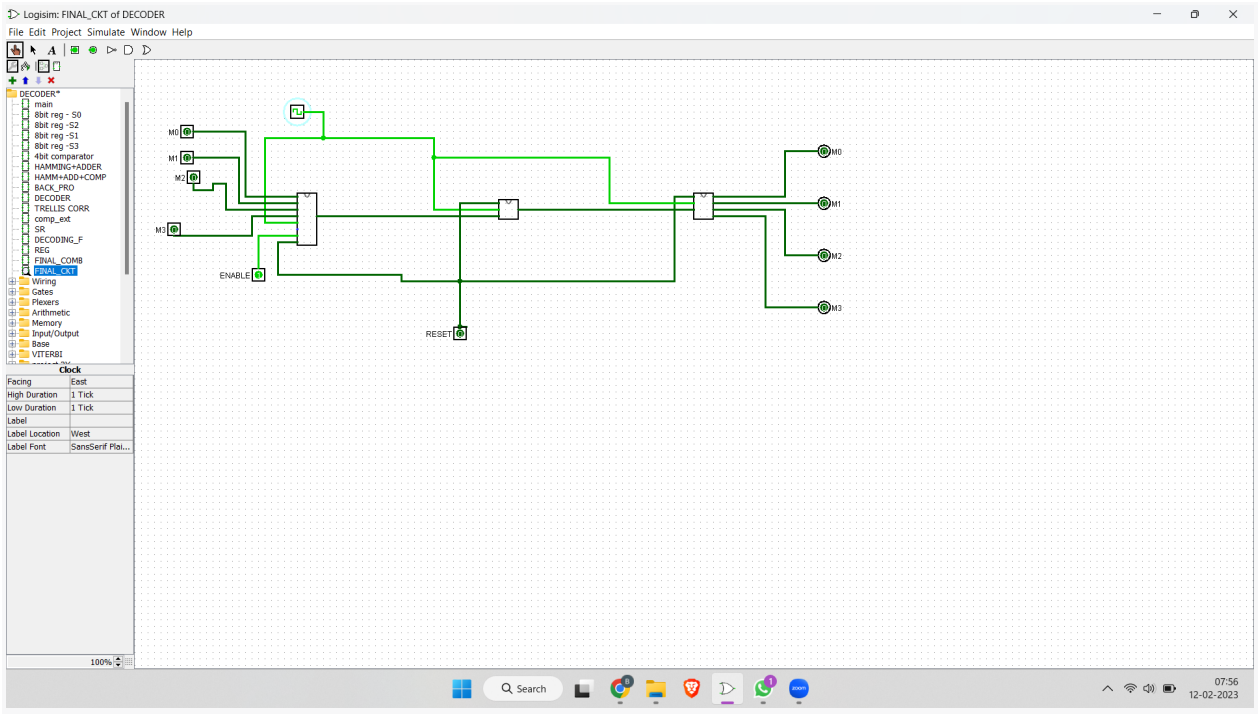
$\underline{u} = (1\ 0\ 1\ 1\ 0\ 0)$

$\underline{v} = (11 \mid 01 \mid 00 \mid 10 \mid 10 \mid 00 \mid)$ (11 written above the last 00)

Starting with S_0

"Every codeword of a convolutional code can be represented by a path through the trellis".

for starting encoding machine start at ... stage.


Logisim: FINAL_CKT of DECODER
File Edit Project Simulate Window Help
DECODER*
main
8bit reg - S0
8bit reg -S2
8bit reg -S1
8bit reg -S3
4bit comparator
HAMMING+ADDER
HAMM+ADD+COMP
BACK_PRO
DECODER
TRELLIS CORR
comp_ext
SR
DECODING_F
REG
FINAL_COMB
FINAL_CKT
Wiring
Gates
Plexers
Arithmetic
Memory
Input/Output
Base
VITERBI
Clock
Facing East
High Duration 1 Tick
Low Duration 1 Tick
Label
Label Location West
Label Font SansSerif Plai...
100%
M0
M1
M2
M3
ENABLE
RESET
M0
M1
M2
M3
Search
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