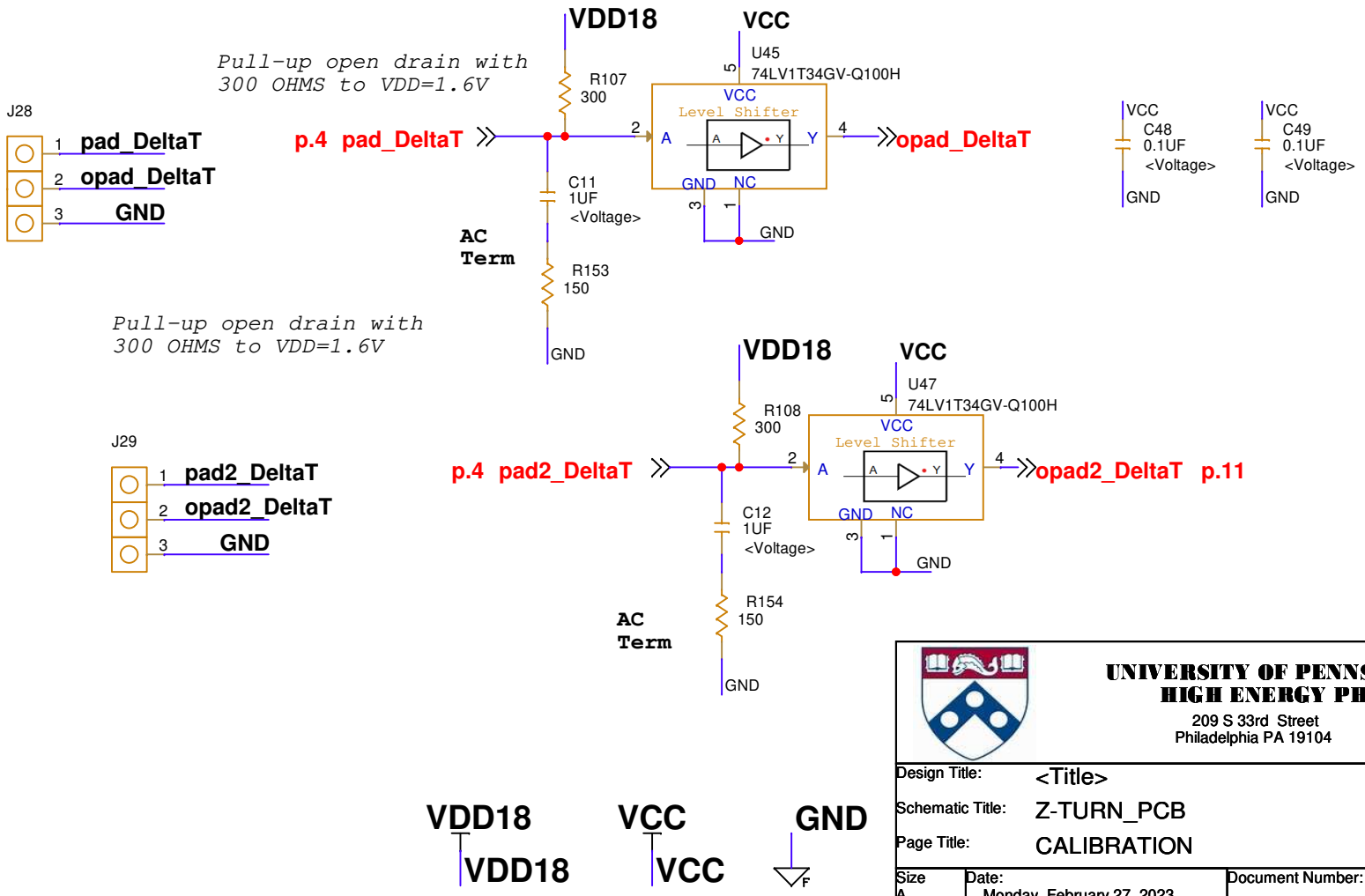
QPIX output: Calibration (deltaT)



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QPIX input: clocks, resets

CLOCKS IN

p.4,15! pad2_CLK_P
p.4,15! pad2_CLK_N
p.4,16! pad_CLK_P
p.4,16! pad_CLK_N

RESETS IN

p.4,17! pad2_RST_EXT_P
p.4,17! pad2_RST_EXT_N
p.4,18! pad_RST_EXT_P
p.4,18! pad_RST_EXT_N

GNET1, GNET2, GNET3, GNET4 — G-NETWORK (GND, VDD, out1, out2, IN1, IN2)

xpad2_CLK_P
xpad2_CLK_N
xpad_CLK_P
xpad_CLK_N
xpad2_RST_EXT_P
xpad2_RST_EXT_N
xpad_RST_EXT_P
xpad_RST_EXT_N

U58 — SN65LVDS31DR

opad2_CLK
opad_CLK
opad2_RST_EXT
opad_RST_EXT

C33 0.1UF <Voltage>

QPIX outputs: Ring Oscillators

C24 0.1UF <Voltage>

p.4 pad2_CLKOUTP
p.4 pad2_CLKOUTN
p.4 pad_CLKOUTP
p.4 pad_CLKOUTN

R193 100
R194 100

U36 MAX40027

scope_pad2_CLKOUTP
scope_pad2_CLKOUTN
scope_pad_CLKOUTP
scope_pad_CLKOUTN

J22
J23

TO SCOPE

Termination

VCC
GND
VDD

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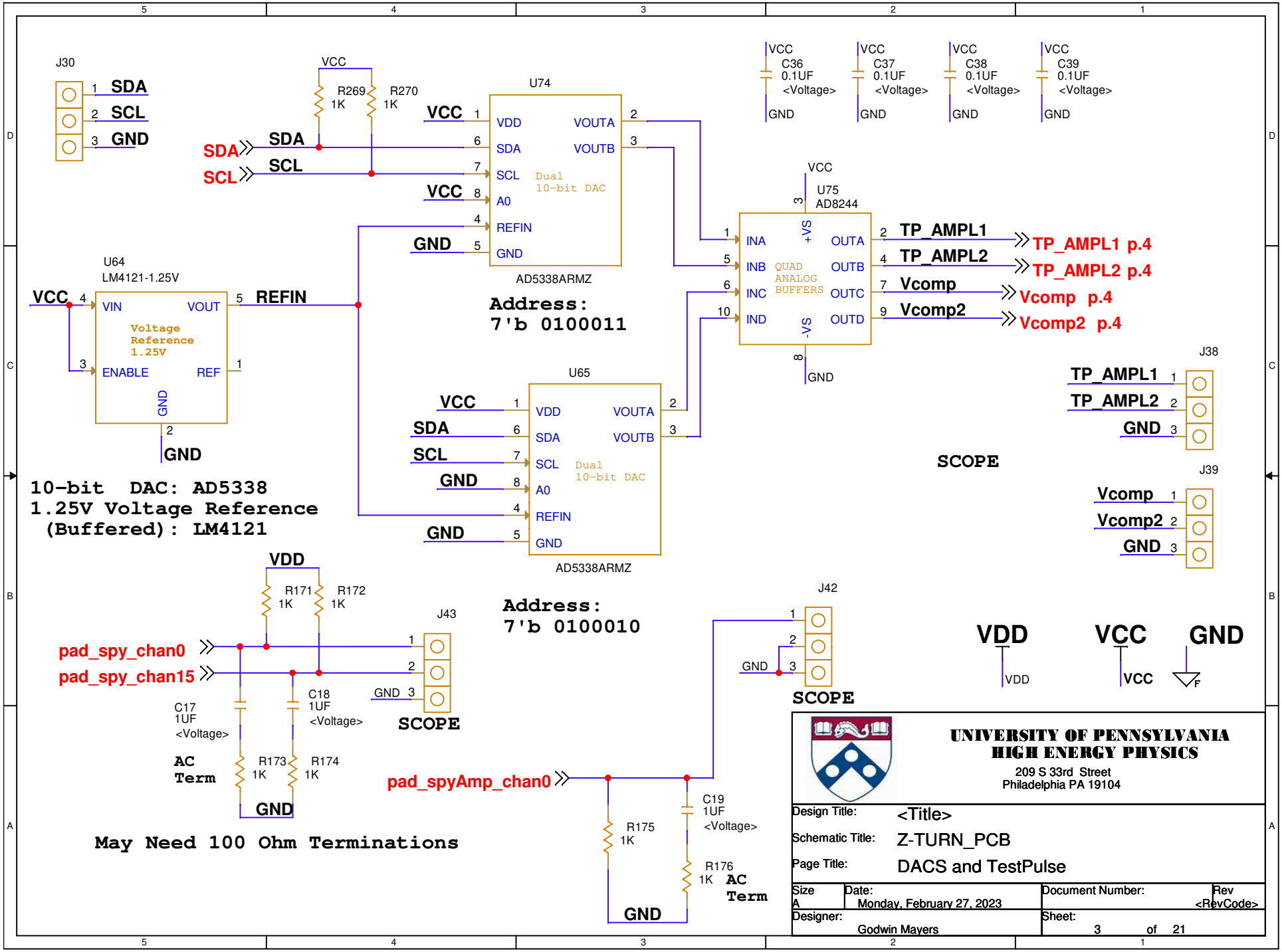
J30
SDA
SCL
GND
VCC
R269 1K
R270 1K
SDA
SCL
U74
VDD
VOUTA
SDA
VOUTB
SCL
Dual 10-bit DAC
A0
REFIN
GND
AD5338ARMZ
Address: 7'b 0100011
VCC C36 0.1UF <Voltage> GND
VCC C37 0.1UF <Voltage> GND
VCC C38 0.1UF <Voltage> GND
VCC C39 0.1UF <Voltage> GND
U75 AD8244
+VS
-VS
INA
INB
INC
IND
OUTA
OUTB
OUTC
OUTD
QUAD ANALOG BUFFERS
TP_AMPL1
TP_AMPL2
Vcomp
Vcomp2
TP_AMPL1 p.4
TP_AMPL2 p.4
Vcomp p.4
Vcomp2 p.4
U64
LM4121-1.25V
VIN
VOUT
Voltage Reference 1.25V
ENABLE
REF
REFIN
U65
J38
J39
SCOPE
10-bit DAC: AD5338
1.25V Voltage Reference (Buffered): LM4121
Address: 7'b 0100010
VDD
R171 1K
R172 1K
J43
pad_spy_chan0
pad_spy_chan15
C17 1UF <Voltage>
C18 1UF <Voltage>
AC Term
R173 1K
R174 1K
J42
pad_spyAmp_chan0
R175 1K
C19 1UF <Voltage>
R176 1K
May Need 100 Ohm Terminations
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Schematic Title: Z-TURN_PCB
Page Title: DACS and TestPulse
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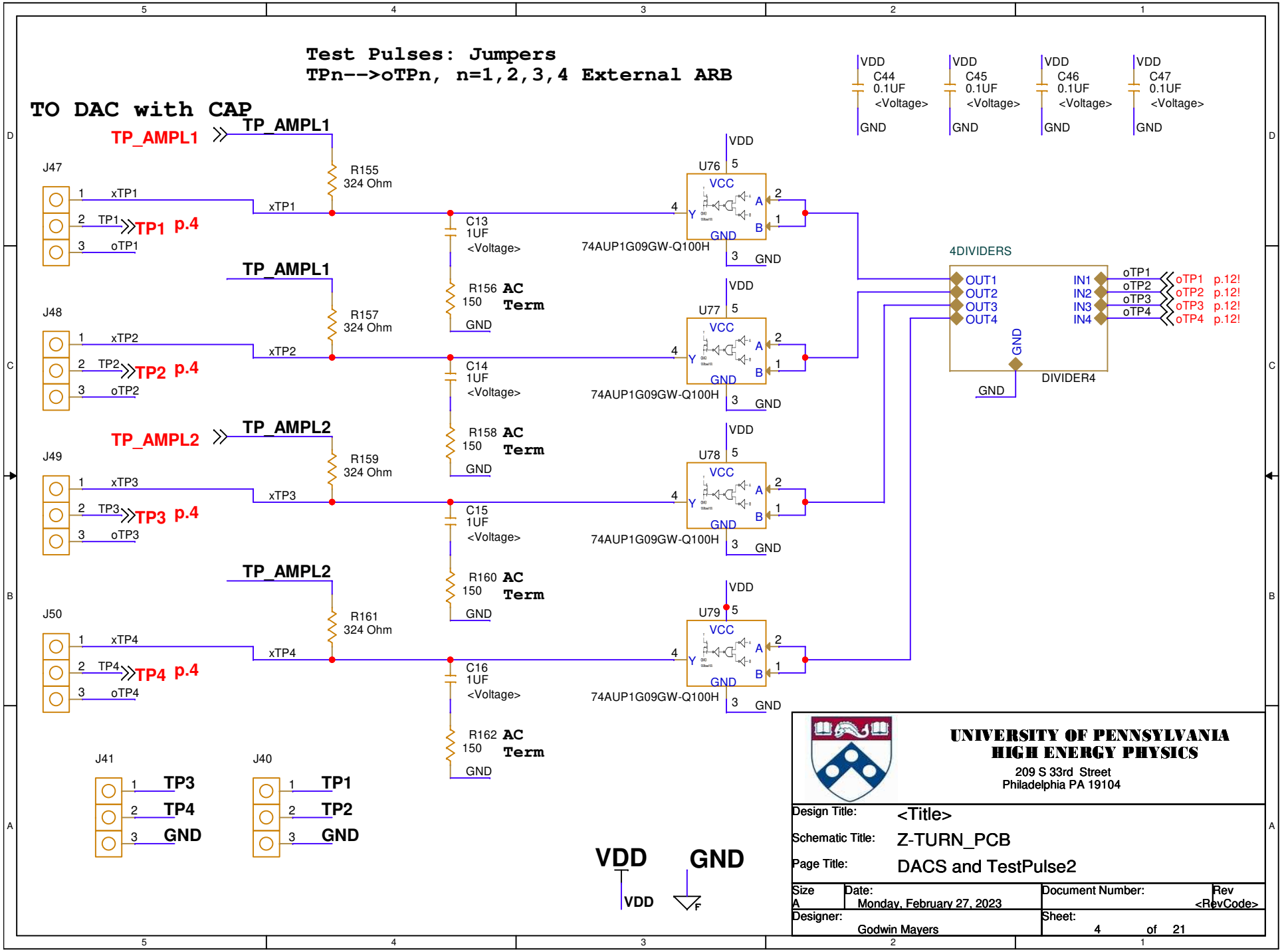
Test Pulses: Jumpers
TPn-->oTPn, n=1,2,3,4 External ARB
TO DAC with CAP
TP_AMPL1
TP_AMPL2
J47
J48
J49
J50
xTP1
xTP2
xTP3
xTP4
oTP1
oTP2
oTP3
oTP4
TP1 p.4
TP2 p.4
TP3 p.4
TP4 p.4
R155 324 Ohm
R157 324 Ohm
R159 324 Ohm
R161 324 Ohm
C13 1UF <Voltage>
C14 1UF <Voltage>
C15 1UF <Voltage>
C16 1UF <Voltage>
R156 150 AC Term
R158 150 AC Term
R160 150 AC Term
R162 150 AC Term
U76
U77
U78
U79
74AUP1G09GW-Q100H
VDD
GND
4DIVIDERS
DIVIDER4
OUT1
OUT2
OUT3
OUT4
IN1
IN2
IN3
IN4
oTP1 p.12!
oTP2 p.12!
oTP3 p.12!
oTP4 p.12!
C44 0.1UF <Voltage>
C45 0.1UF <Voltage>
C46 0.1UF <Voltage>
C47 0.1UF <Voltage>
J41
J40
TP3
TP4
TP1
TP2
GND
VDD
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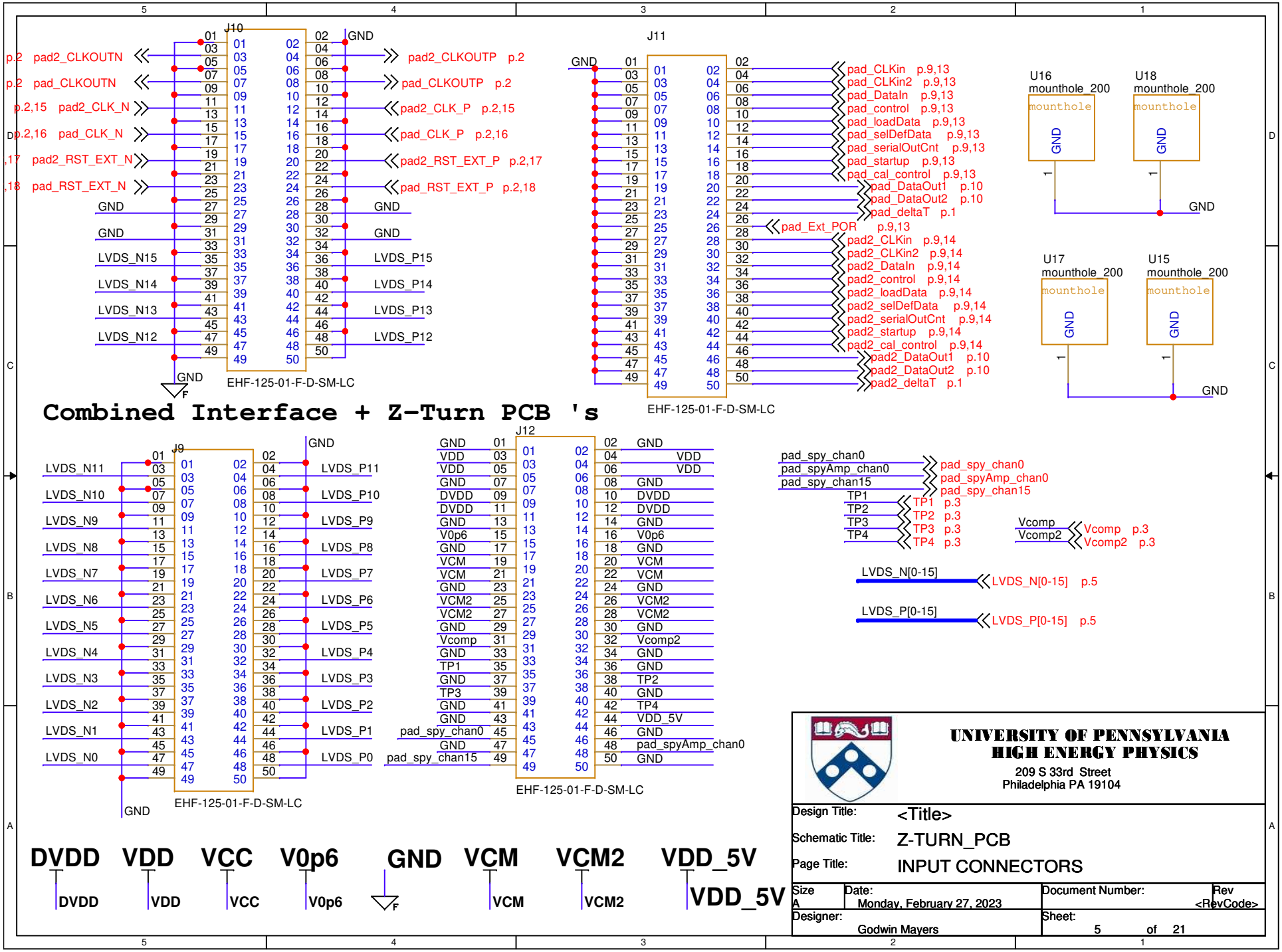
J10
EHF-125-01-F-D-SM-LC
p.2 pad2_CLKOUTN
p.2 pad_CLKOUTN
p.2,15 pad2_CLK_N
p.2,16 pad_CLK_N
,17 pad2_RST_EXT_N
,18 pad_RST_EXT_N
pad2_CLKOUTP p.2
pad_CLKOUTP p.2
pad2_CLK_P p.2,15
pad_CLK_P p.2,16
pad2_RST_EXT_P p.2,17
pad_RST_EXT_P p.2,18
GND
LVDS_N15
LVDS_N14
LVDS_N13
LVDS_N12
LVDS_P15
LVDS_P14
LVDS_P13
LVDS_P12
J11
EHF-125-01-F-D-SM-LC
pad_CLKin p.9,13
pad_CLKin2 p.9,13
pad_DataIn p.9,13
pad_control p.9,13
pad_loadData p.9,13
pad_selDefData p.9,13
pad_serialOutCnt p.9,13
pad_startup p.9,13
pad_cal_control p.9,13
pad_DataOut1 p.10
pad_DataOut2 p.10
pad_deltaT p.1
pad_Ext_POR p.9,13
pad2_CLKin p.9,14
pad2_CLKin2 p.9,14
pad2_DataIn p.9,14
pad2_control p.9,14
pad2_loadData p.9,14
pad2_selDefData p.9,14
pad2_serialOutCnt p.9,14
pad2_startup p.9,14
pad2_cal_control p.9,14
pad2_DataOut1 p.10
pad2_DataOut2 p.10
pad2_deltaT p.1
U16 mounthole_200
U18 mounthole_200
U17 mounthole_200
U15 mounthole_200
mounthole
GND
Combined Interface + Z-Turn PCB 's
J9
EHF-125-01-F-D-SM-LC
LVDS_N11
LVDS_N10
LVDS_N9
LVDS_N8
LVDS_N7
LVDS_N6
LVDS_N5
LVDS_N4
LVDS_N3
LVDS_N2
LVDS_N1
LVDS_N0
LVDS_P11
LVDS_P10
LVDS_P9
LVDS_P8
LVDS_P7
LVDS_P6
LVDS_P5
LVDS_P4
LVDS_P3
LVDS_P2
LVDS_P1
LVDS_P0
J12
EHF-125-01-F-D-SM-LC
VDD
DVDD
GND
V0p6
VCM
VCM2
Vcomp
Vcomp2
TP1
TP2
TP3
TP4
VDD_5V
pad_spy_chan0
pad_spyAmp_chan0
pad_spy_chan15
LVDS_N[0-15]
LVDS_P[0-15]
p.3
p.5
DVDD
VDD
VCC
V0p6
GND
VCM
VCM2
VDD_5V
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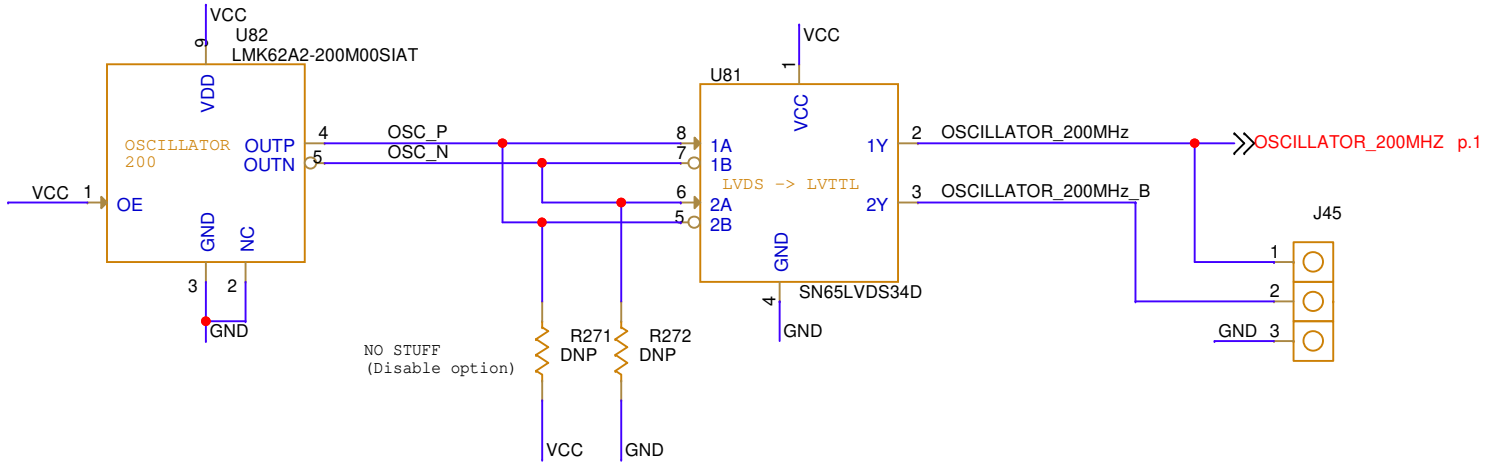
Still Need 200MHz Oscillator:
LMK62A2-200M00SIAT Oscillator LVDS



VCC

VCC

GND

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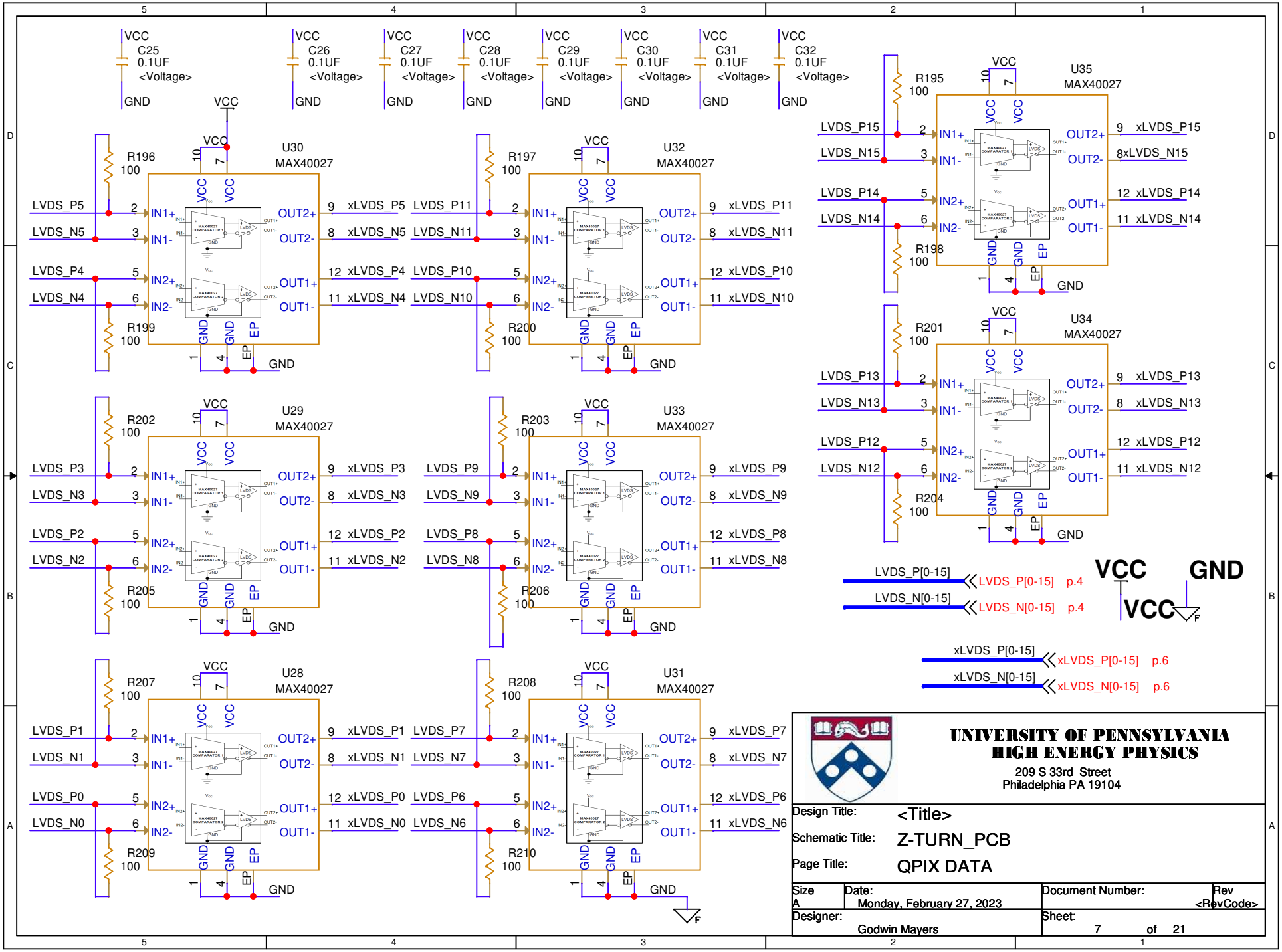
C25 0.1UF <Voltage>
C26 0.1UF <Voltage>
C27 0.1UF <Voltage>
C28 0.1UF <Voltage>
C29 0.1UF <Voltage>
C30 0.1UF <Voltage>
C31 0.1UF <Voltage>
C32 0.1UF <Voltage>
VCC
GND
U30 MAX40027
U32 MAX40027
U35 MAX40027
U29 MAX40027
U33 MAX40027
U34 MAX40027
U28 MAX40027
U31 MAX40027
R196 100
R197 100
R195 100
R199 100
R200 100
R198 100
R202 100
R203 100
R201 100
R205 100
R206 100
R204 100
R207 100
R208 100
R209 100
R210 100
LVDS_P5
LVDS_N5
LVDS_P4
LVDS_N4
LVDS_P11
LVDS_N11
LVDS_P10
LVDS_N10
LVDS_P15
LVDS_N15
LVDS_P14
LVDS_N14
LVDS_P3
LVDS_N3
LVDS_P2
LVDS_N2
LVDS_P9
LVDS_N9
LVDS_P8
LVDS_N8
LVDS_P13
LVDS_N13
LVDS_P12
LVDS_N12
LVDS_P1
LVDS_N1
LVDS_P0
LVDS_N0
LVDS_P7
LVDS_N7
LVDS_P6
LVDS_N6
IN1+
IN1-
IN2+
IN2-
OUT2+
OUT2-
OUT1+
OUT1-
xLVDS_P5
xLVDS_N5
xLVDS_P4
xLVDS_N4
xLVDS_P11
xLVDS_N11
xLVDS_P10
xLVDS_N10
xLVDS_P15
xLVDS_N15
xLVDS_P14
xLVDS_N14
xLVDS_P3
xLVDS_N3
xLVDS_P2
xLVDS_N2
xLVDS_P9
xLVDS_N9
xLVDS_P8
xLVDS_N8
xLVDS_P13
xLVDS_N13
xLVDS_P12
xLVDS_N12
xLVDS_P1
xLVDS_N1
xLVDS_P0
xLVDS_N0
xLVDS_P7
xLVDS_N7
xLVDS_P6
xLVDS_N6
LVDS_P[0-15]
LVDS_N[0-15]
LVDS_P[0-15] p.4
LVDS_N[0-15] p.4
xLVDS_P[0-15]
xLVDS_N[0-15]
xLVDS_P[0-15] p.6
xLVDS_N[0-15] p.6
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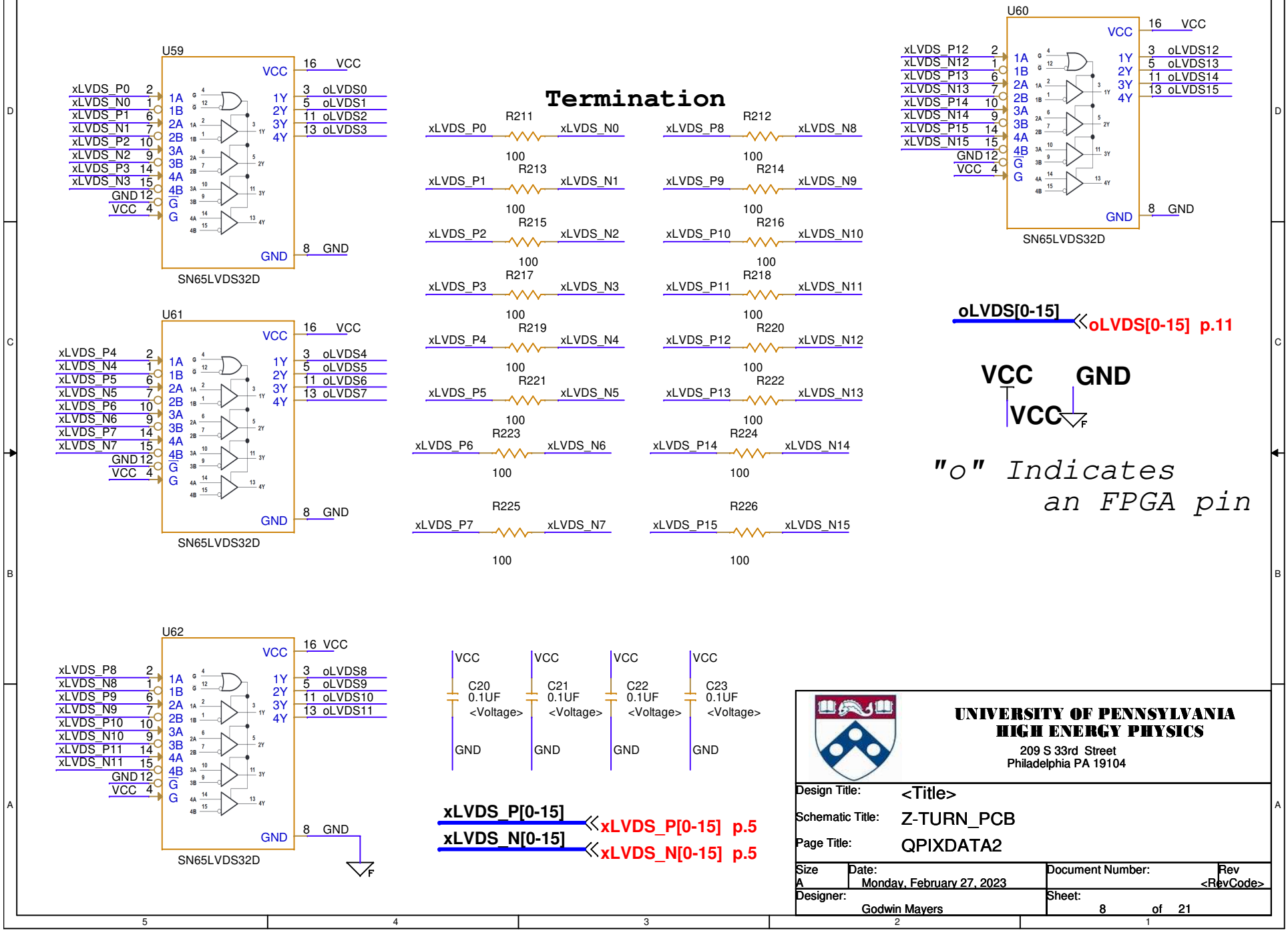
U59
xLVDS_P0 2
xLVDS_N0 1
xLVDS_P1 6
xLVDS_N1 7
xLVDS_P2 10
xLVDS_N2 9
xLVDS_P3 14
xLVDS_N3 15
GND 12
VCC 4
1A 1B 2A 2B 3A 3B 4A 4B G G
VCC
GND
16 VCC
3 oLVDS0
5 oLVDS1
11 oLVDS2
13 oLVDS3
8 GND
SN65LVDS32D
U61
xLVDS_P4 2
xLVDS_N4 1
xLVDS_P5 6
xLVDS_N5 7
xLVDS_P6 10
xLVDS_N6 9
xLVDS_P7 14
xLVDS_N7 15
GND 12
VCC 4
1Y 2Y 3Y 4Y
VCC
GND
16 VCC
3 oLVDS4
5 oLVDS5
11 oLVDS6
13 oLVDS7
8 GND
SN65LVDS32D
U62
xLVDS_P8 2
xLVDS_N8 1
xLVDS_P9 6
xLVDS_N9 7
xLVDS_P10 10
xLVDS_N10 9
xLVDS_P11 14
xLVDS_N11 15
GND 12
VCC 4
1Y 2Y 3Y 4Y
VCC
GND
16 VCC
3 oLVDS8
5 oLVDS9
11 oLVDS10
13 oLVDS11
8 GND
SN65LVDS32D
Termination
R211
xLVDS_P0 xLVDS_N0
100
R213
xLVDS_P1 xLVDS_N1
100
R215
xLVDS_P2 xLVDS_N2
100
R217
xLVDS_P3 xLVDS_N3
100
R219
xLVDS_P4 xLVDS_N4
100
R221
xLVDS_P5 xLVDS_N5
100
R223
xLVDS_P6 xLVDS_N6
100
R225
xLVDS_P7 xLVDS_N7
100
R212
xLVDS_P8 xLVDS_N8
100
R214
xLVDS_P9 xLVDS_N9
100
R216
xLVDS_P10 xLVDS_N10
100
R218
xLVDS_P11 xLVDS_N11
100
R220
xLVDS_P12 xLVDS_N12
100
R222
xLVDS_P13 xLVDS_N13
100
R224
xLVDS_P14 xLVDS_N14
100
R226
xLVDS_P15 xLVDS_N15
100
U60
xLVDS_P12 2
xLVDS_N12 1
xLVDS_P13 6
xLVDS_N13 7
xLVDS_P14 10
xLVDS_N14 9
xLVDS_P15 14
xLVDS_N15 15
GND 12
VCC 4
1A 1B 2A 2B 3A 3B 4A 4B G G
VCC
GND
16 VCC
3 oLVDS12
5 oLVDS13
11 oLVDS14
13 oLVDS15
8 GND
SN65LVDS32D
oLVDS[0-15]
oLVDS[0-15] p.11
VCC GND
VCC
"o" Indicates an FPGA pin
VCC
C20 0.1UF <Voltage>
GND
VCC
C21 0.1UF <Voltage>
GND
VCC
C22 0.1UF <Voltage>
GND
VCC
C23 0.1UF <Voltage>
GND
xLVDS_P[0-15]
xLVDS_P[0-15] p.5
xLVDS_N[0-15]
xLVDS_N[0-15] p.5
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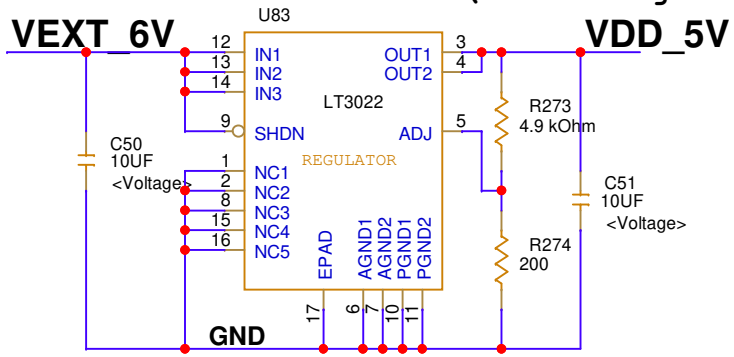
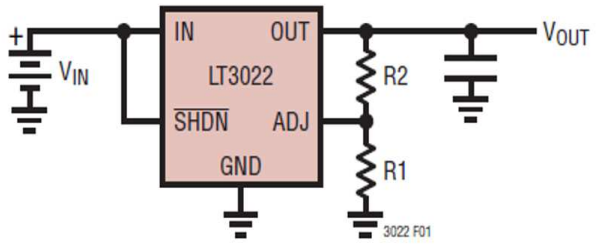
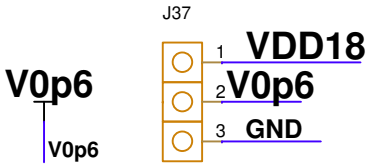
(For Analog switch DG412)

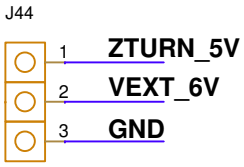




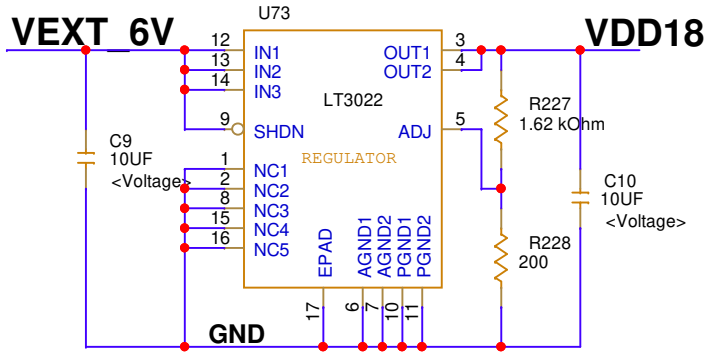
V_{OUT}: 200mV • (1 + R2/R1) – (I_{ADJ} • R2)
V_{ADJ}: 200mV
I_{ADJ}: 30nA AT 25°C
OUTPUT RANGE: 0.2V TO 9.5V

Figure 1. Adjustable Operation

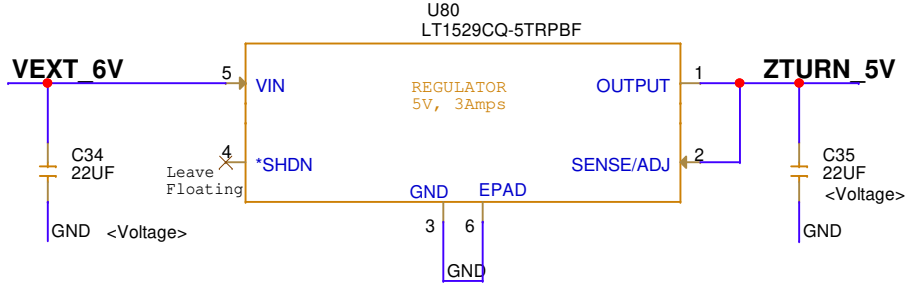


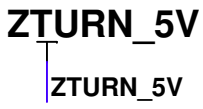


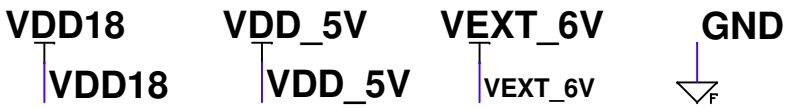
VDD18: 1.8v
QPIX output: Calibration (deltaT)

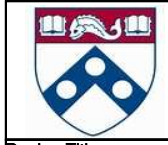


NEED 5v regulator for zTURN
***** to be safe *****









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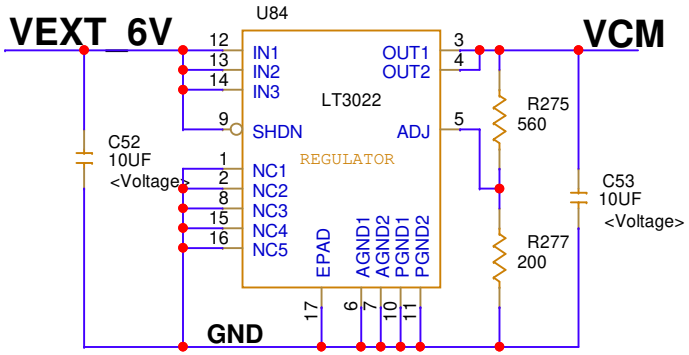
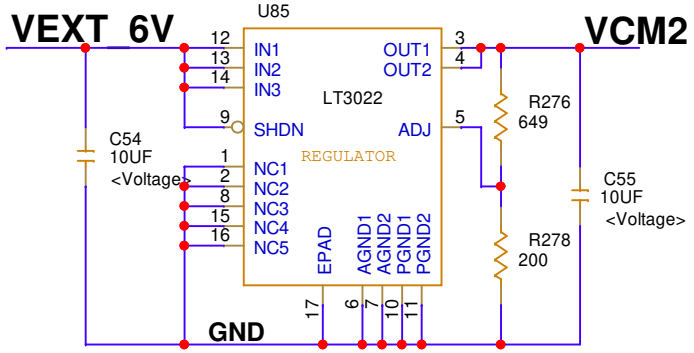
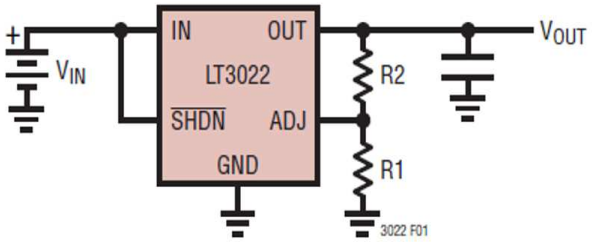
VCM: 750mV



VCM2: 850mV





V_{OUT}: 200mV • (1 + R2/R1) – (I_{ADJ} • R2)
V_{ADJ}: 200mV
I_{ADJ}: 30nA AT 25°C
OUTPUT RANGE: 0.2V TO 9.5V

Figure 1. Adjustable Operation

VCM
VCM

VCM2
VCM2

VEXT_6V
VEXT_6V

GND

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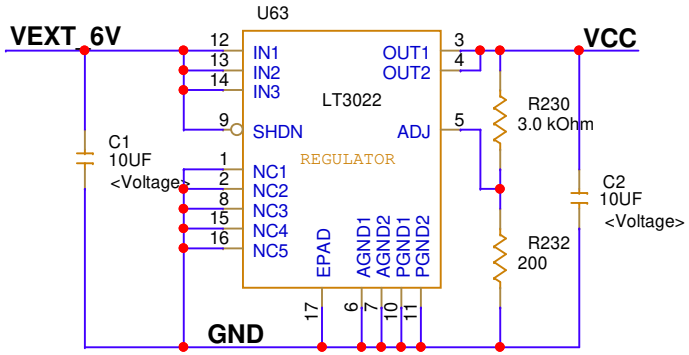
REGULATOR OPTIONS
LT3081: 1.5A, adjustable 0 - 3v0

LT3022: 1.0A adjustable 200mV -->

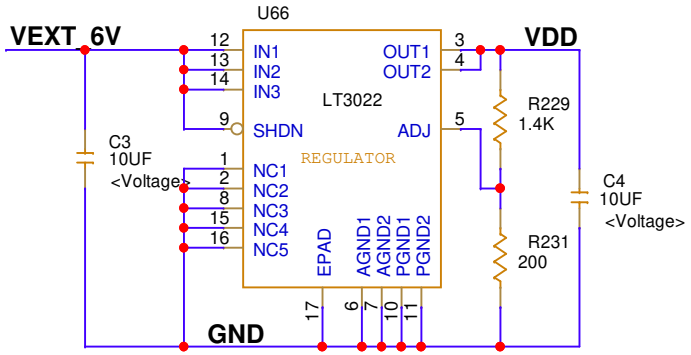
DVDD VDD VCC V0p6 GND

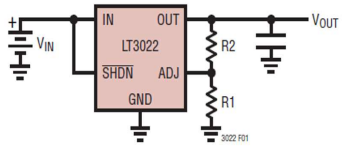
DVDD VDD VCC V0p6

VCC: 3.3v



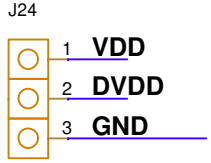
VDD: 1.6v



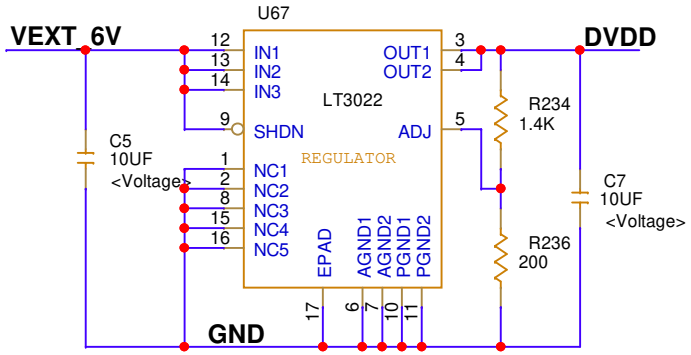


V_{OUT}: 200mV • (1 + R2/R1) – (I_{ADJ} • R2)
V_{ADJ}: 200mV
I_{ADJ}: 30nA AT 25°C
OUTPUT RANGE: 0.2V TO 9.5V

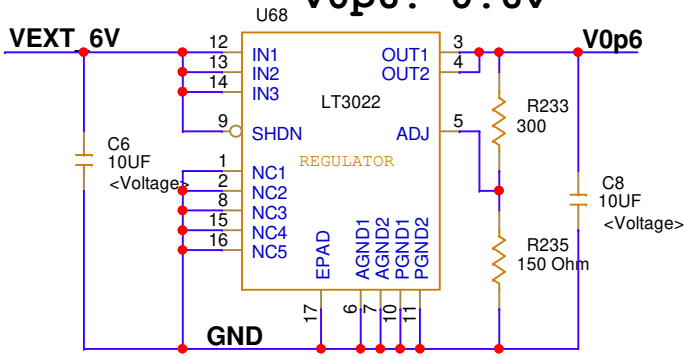
Figure 1. Adjustable Operation

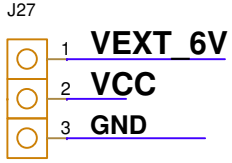


DVDD: 1.6v

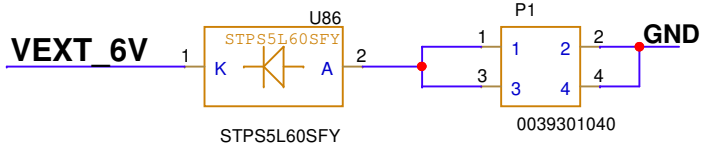


V0p6: 0.6v





POWER PLUG:7v



VEXT_6V

VEXT_6V

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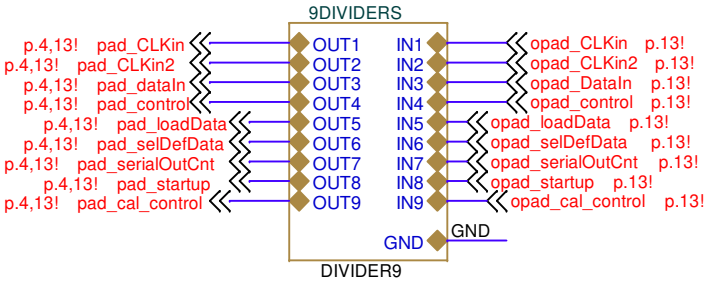
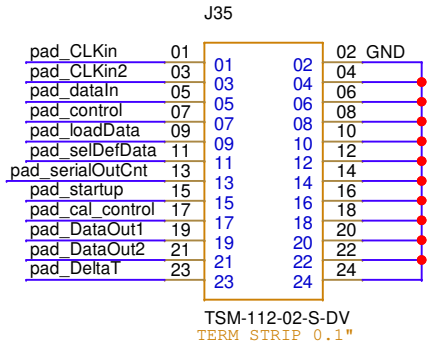
Map these to "F"

QPIX inputs: Serial Interface

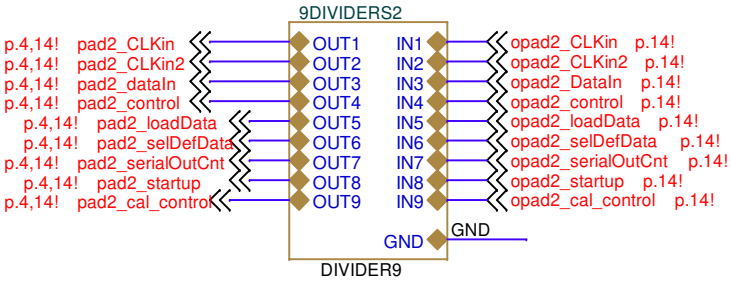


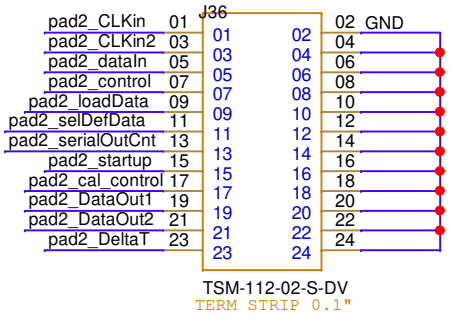


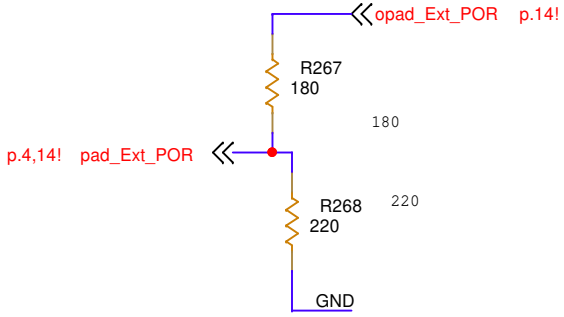
"o" Indicates an FPGA pin

p.4 pad_DataOut1 >> pad_DataOut1
p.4 pad_DataOut2 >> pad_DataOut2
p.4 pad_DeltaT >> pad_DeltaT

p.4 pad2_DataOut1 >> pad2_DataOut1
p.4 pad2_DataOut2 >> pad2_DataOut2
p.4 pad2_DeltaT >> pad2_DeltaT







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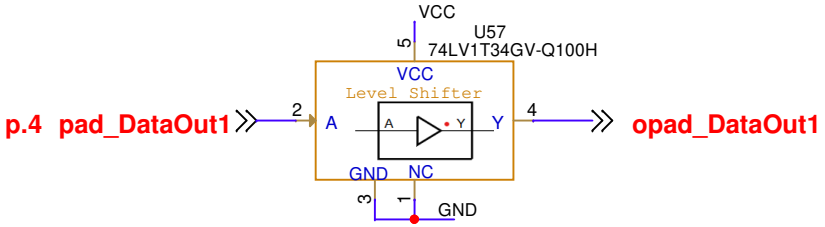
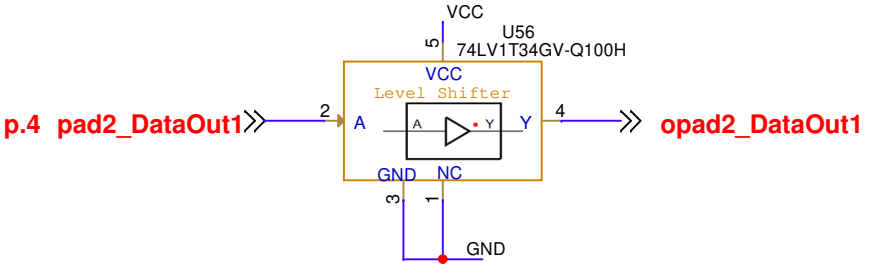
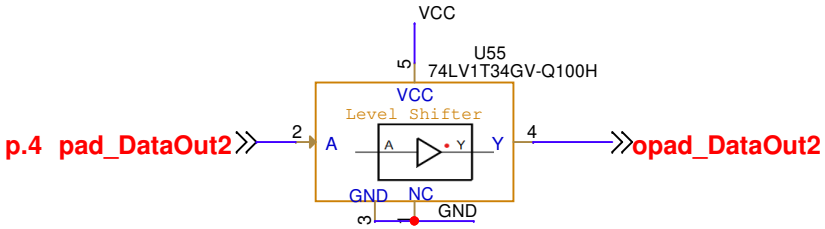
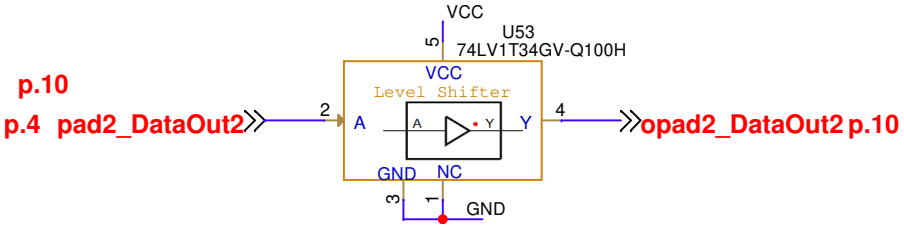
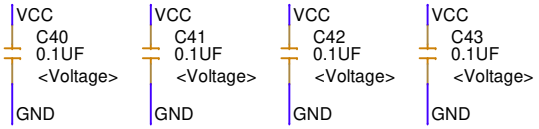
"o" Indicates an FPGA pin

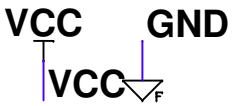












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Z-TURN CONNECTORS

"o" Indicates an FPGA pin

opad_CLKin
opad_CLKin2
opad_DataIn
opad_control
opad_loadData
opad_selDefData
opad_serialOutCnt
opad_startup
opad_cal_control
opad_DataOut1
opad_DataOut2
opad_deltaT

opad_CLKin p.9,13
opad_CLKin2 p.9,13
opad_DataIn p.9,13
opad_control p.9,13
opad_loadData p.9,13
opad_selDefData p.9,13
opad_serialOutCnt p.9,13
opad_startup p.9,13
opad_cal_control p.9,13
opad_DataOut1 p.10
opad_DataOut2 p.10
opad_deltaT p.1

opad2_CLKin
opad2_CLKin2
opad2_DataIn
opad2_control
opad2_loadData
opad2_selDefData
opad2_serialOutCnt
opad2_startup
opad2_cal_control
opad2_DataOut1
opad2_DataOut2
opad2_deltaT

opad2_CLKin p.9,14
opad2_CLKin2 p.9,14
opad2_DataIn p.9,14
opad2_control p.9,14
opad2_loadData p.9,14
opad2_selDefData p.9,14
opad2_serialOutCnt p.9,14
opad2_startup p.9,14
opad2_cal_control p.9,14
opad2_DataOut1 p.10
opad2_DataOut2
opad2_deltaT p.1

opad_Ext_POR
opad_Ext_POR p.14!

SDA
SDA p.9,14

SCL
SCL p.9,14

opad2_CLK
opad2_CLK

opad_CLK
opad_CLK

opad2_RST_EXT
opad2_RST_EXT

opad_RST_EXT
opad_RST_EXT

oTP1
oTP2
oTP3
oTP4

oTP1 p.12!
oTP2 p.12!
oTP3 p.12!
oTP4 p.12!

MYiR schematic J11 --> CN1

J20

ZTURN_5V	1	2	GND
	3	4	GND
	5	6	
	7	8	
	9	10	
	11	12	
	13	14	
	15	16	
	17	18	
	19	20	
	21	22	
GND	23	24	GND
GND	25	26	opad_Ext_POR
	27	28	SDA
	29	30	SCL
	31	32	TRIGGER
	33	34	GND
GND	35	36	opad2_RST_EXT
	37	38	opad_RST_EXT
	39	40	
	41	42	
	43	44	GND
	45	46	
	47	48	
	49	50	
	51	52	
	53	54	GND
	55	56	
	57	58	
	59	60	
	61	62	
	63	64	
	65	66	
GND	67	68	GND
	69	70	
	71	72	
	73	74	
	75	76	
	77	78	
	79	80	

TFM-140-02-X-D-A

MYiR schematic J12 --> CN2

J21

ZTURN_5V	1	2	GND
	3	4	GND
	5	6	
	7	8	
	9	10	GND
	11	12	
	13	14	
	15	16	
	17	18	
	19	20	GND
GND	21	22	opad2_loadData
opad_CLKin	23	24	opad2_selDefData
opad_CLKin2	25	26	opad2_serialOutCnt
opad_DataIn	27	28	opad2_startup
opad_control	29	30	GND
GND	31	32	opad2_CLKin
opad_loadData	33	34	opad2_CLKin2
opad_selDefData	35	36	opad2_DataIn
opad_serialOutCnt	37	38	opad2_control
opad_startup	39	40	GND
GND	41	42	opad2_DataOut1
opad_cal_control	43	44	opad2_DataOut2
opad_DataOut1	45	46	opad_CLK
opad_DataOut2	47	48	opad2_CLK
opad2_cal_control	49	50	GND
	51	52	oTP1
OSCILLATOR_200MHz	53	54	oTP2
	55	56	oTP3
opad_deltaT	57	58	oTP4
opad2_deltaT	59	60	GND
GND	61	62	oLVDS15
oLVDS0	63	64	oLVDS14
oLVDS1	65	66	oLVDS13
oLVDS2	67	68	oLVDS12
oLVDS3	69	70	GND
GND	71	72	oLVDS11
oLVDS4	73	74	oLVDS10
oLVDS5	75	76	oLVDS9
oLVDS6	77	78	oLVDS8
oLVDS7	79	80	GND

TFM-140-02-X-D-A

Z1

GND
GND
3 GND
4 GND

Zturn Holes

J46

SMB_RA

5 TRIGGER

0734042270

GND

VCC
VCC

GND

ZTURN_5V
ZTURN_5V

oLVDS[0-15]
oLVDS[0-15] p.6

OSCILLATOR_200MHz
OSCILLATOR_200MHZ

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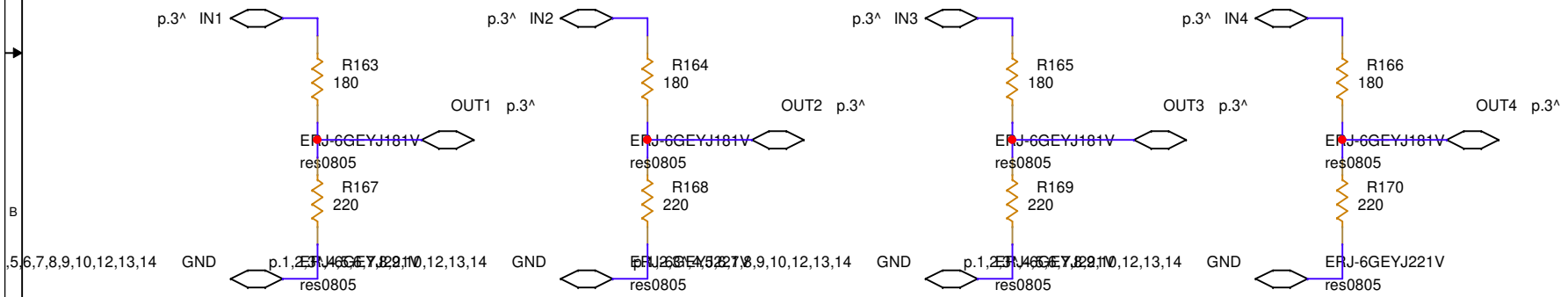

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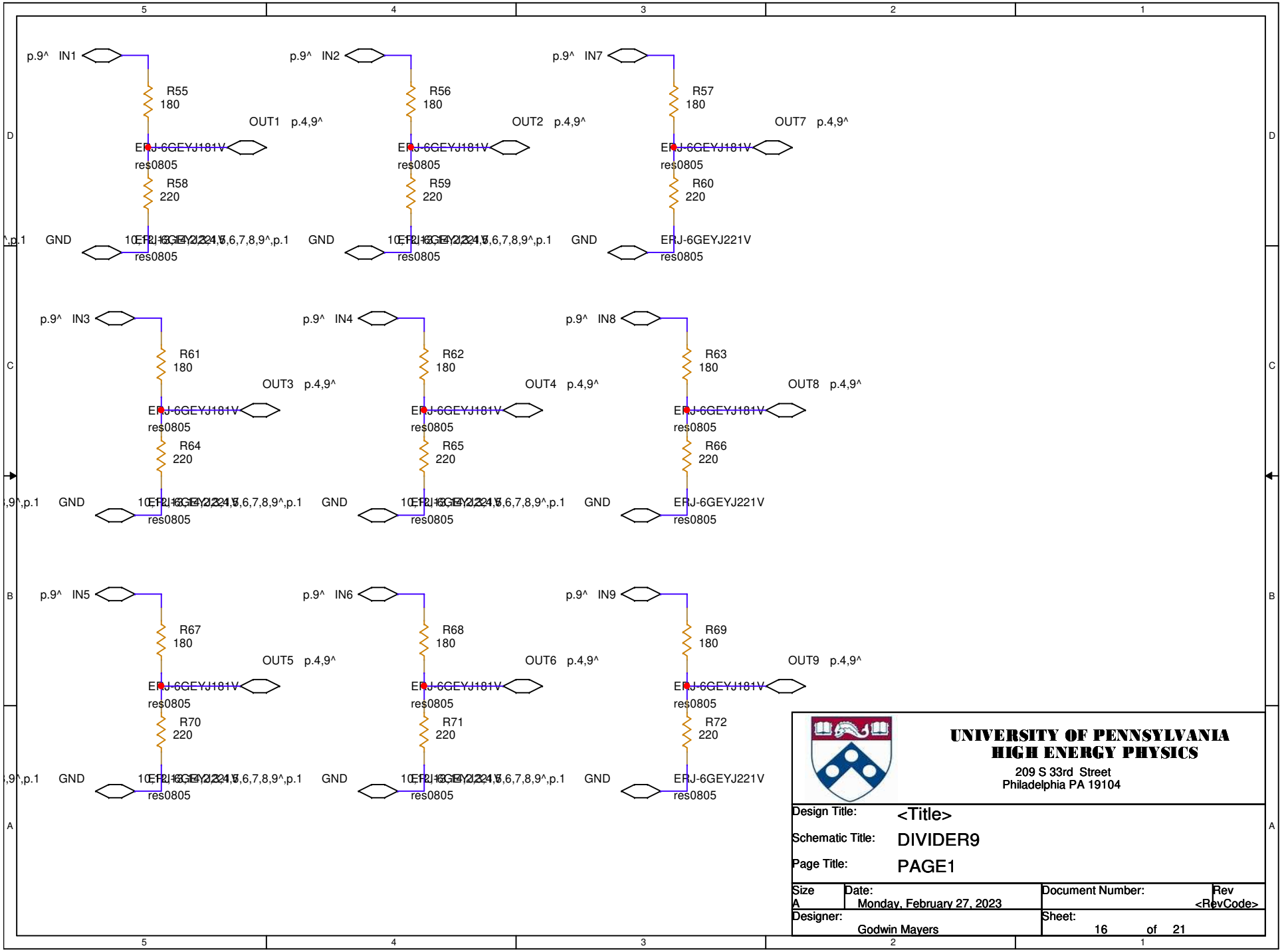
p.9^ IN1
R55
180
OUT1 p.4,9^
ERJ-6GEYJ181V
res0805
R58
220
GND
ERJ-6GEYJ221V
res0805
p.9^ IN2
R56
180
OUT2 p.4,9^
ERJ-6GEYJ181V
res0805
R59
220
GND
ERJ-6GEYJ221V
res0805
p.9^ IN7
R57
180
OUT7 p.4,9^
ERJ-6GEYJ181V
res0805
R60
220
GND
ERJ-6GEYJ221V
res0805
p.9^ IN3
R61
180
OUT3 p.4,9^
ERJ-6GEYJ181V
res0805
R64
220
GND
ERJ-6GEYJ221V
res0805
p.9^ IN4
R62
180
OUT4 p.4,9^
ERJ-6GEYJ181V
res0805
R65
220
GND
ERJ-6GEYJ221V
res0805
p.9^ IN8
R63
180
OUT8 p.4,9^
ERJ-6GEYJ181V
res0805
R66
220
GND
ERJ-6GEYJ221V
res0805
p.9^ IN5
R67
180
OUT5 p.4,9^
ERJ-6GEYJ181V
res0805
R70
220
GND
ERJ-6GEYJ221V
res0805
p.9^ IN6
R68
180
OUT6 p.4,9^
ERJ-6GEYJ181V
res0805
R71
220
GND
ERJ-6GEYJ221V
res0805
p.9^ IN9
R69
180
OUT9 p.4,9^
ERJ-6GEYJ181V
res0805
R72
220
GND
ERJ-6GEYJ221V
res0805
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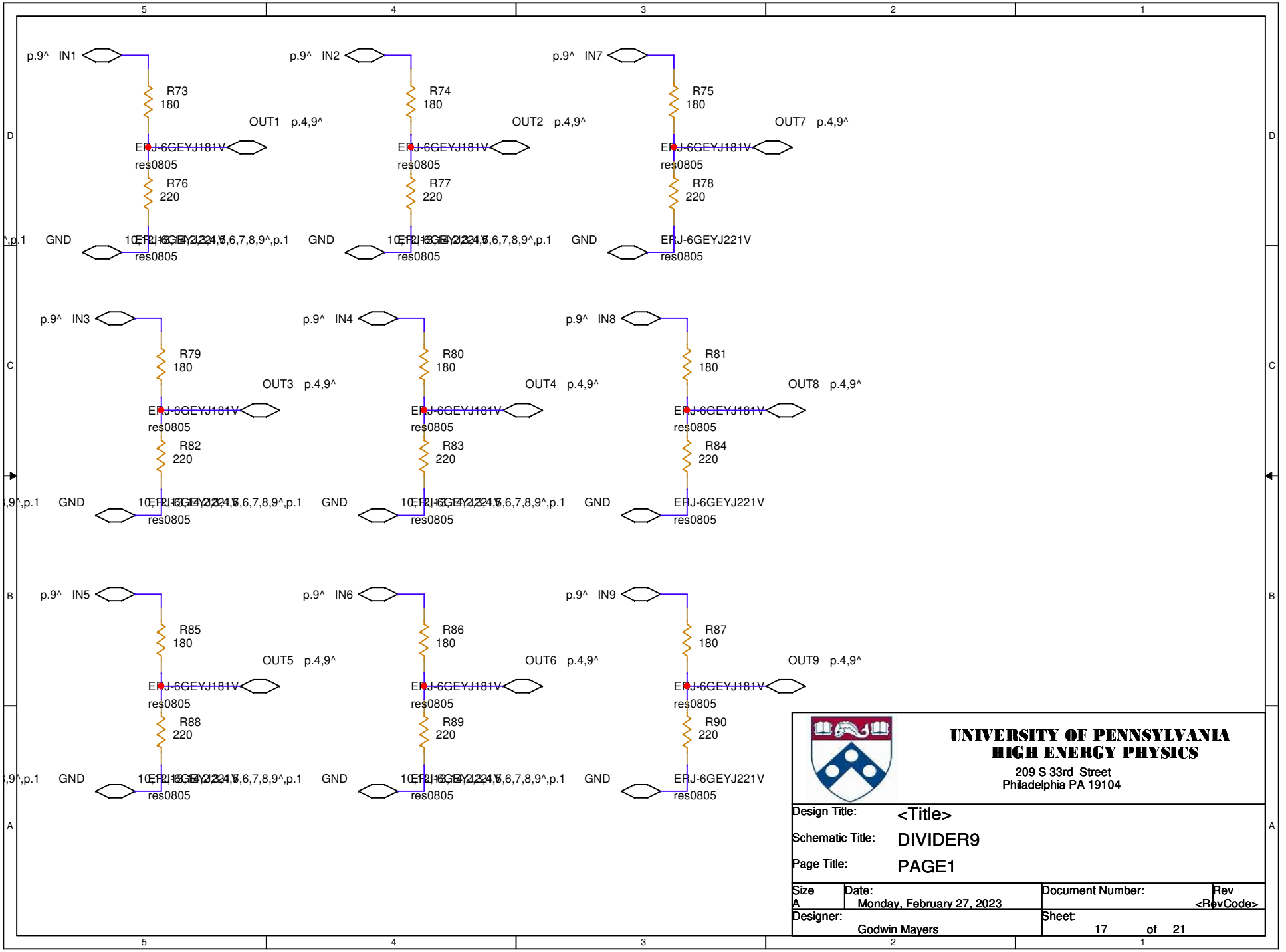
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R73
180
OUT1 p.4,9^
ERJ-6GEYJ181V
res0805
R76
220
GND
ERJ-6GEYJ221V
res0805
p.9^ IN2
R74
180
OUT2 p.4,9^
ERJ-6GEYJ181V
res0805
R77
220
GND
ERJ-6GEYJ221V
res0805
p.9^ IN7
R75
180
OUT7 p.4,9^
ERJ-6GEYJ181V
res0805
R78
220
GND
ERJ-6GEYJ221V
res0805
p.9^ IN3
R79
180
OUT3 p.4,9^
ERJ-6GEYJ181V
res0805
R82
220
GND
ERJ-6GEYJ221V
res0805
p.9^ IN4
R80
180
OUT4 p.4,9^
ERJ-6GEYJ181V
res0805
R83
220
GND
ERJ-6GEYJ221V
res0805
p.9^ IN8
R81
180
OUT8 p.4,9^
ERJ-6GEYJ181V
res0805
R84
220
GND
ERJ-6GEYJ221V
res0805
p.9^ IN5
R85
180
OUT5 p.4,9^
ERJ-6GEYJ181V
res0805
R88
220
GND
ERJ-6GEYJ221V
res0805
p.9^ IN6
R86
180
OUT6 p.4,9^
ERJ-6GEYJ181V
res0805
R89
220
GND
ERJ-6GEYJ221V
res0805
p.9^ IN9
R87
180
OUT9 p.4,9^
ERJ-6GEYJ181V
res0805
R90
220
GND
ERJ-6GEYJ221V
res0805
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Designer: Godwin Mayers
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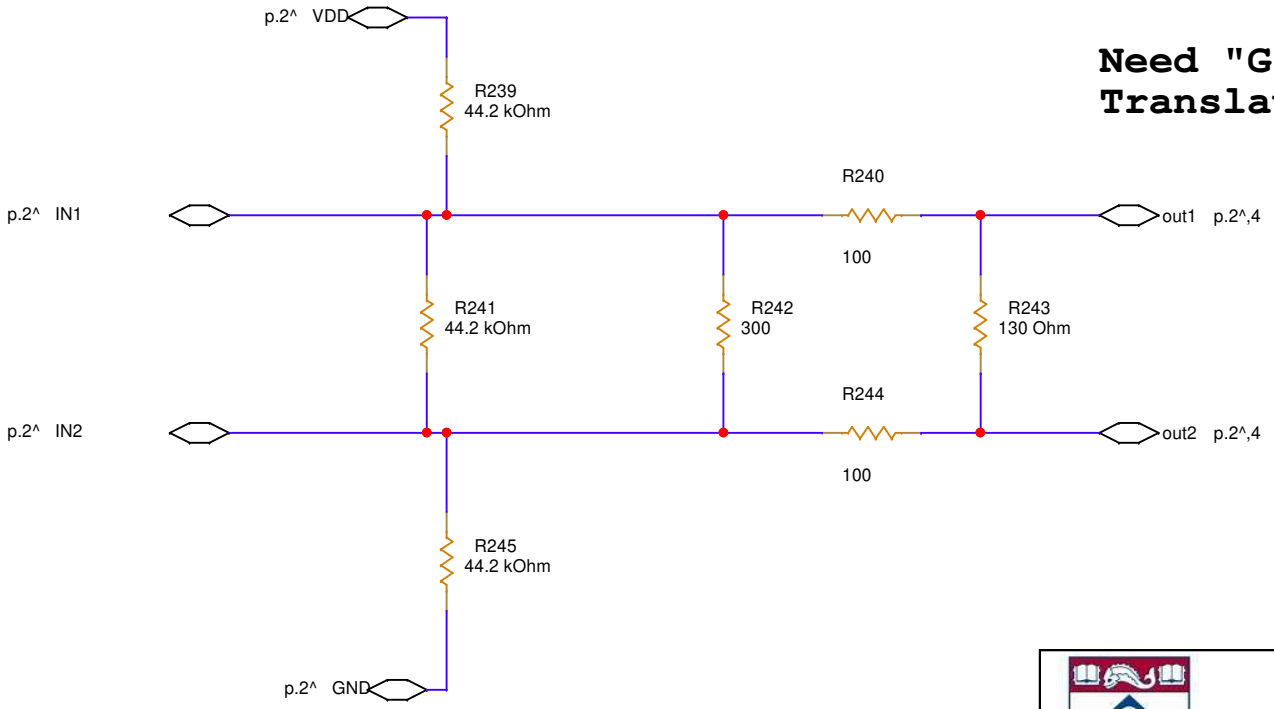

Need "G" network
Translates LVDS --> QLVDS

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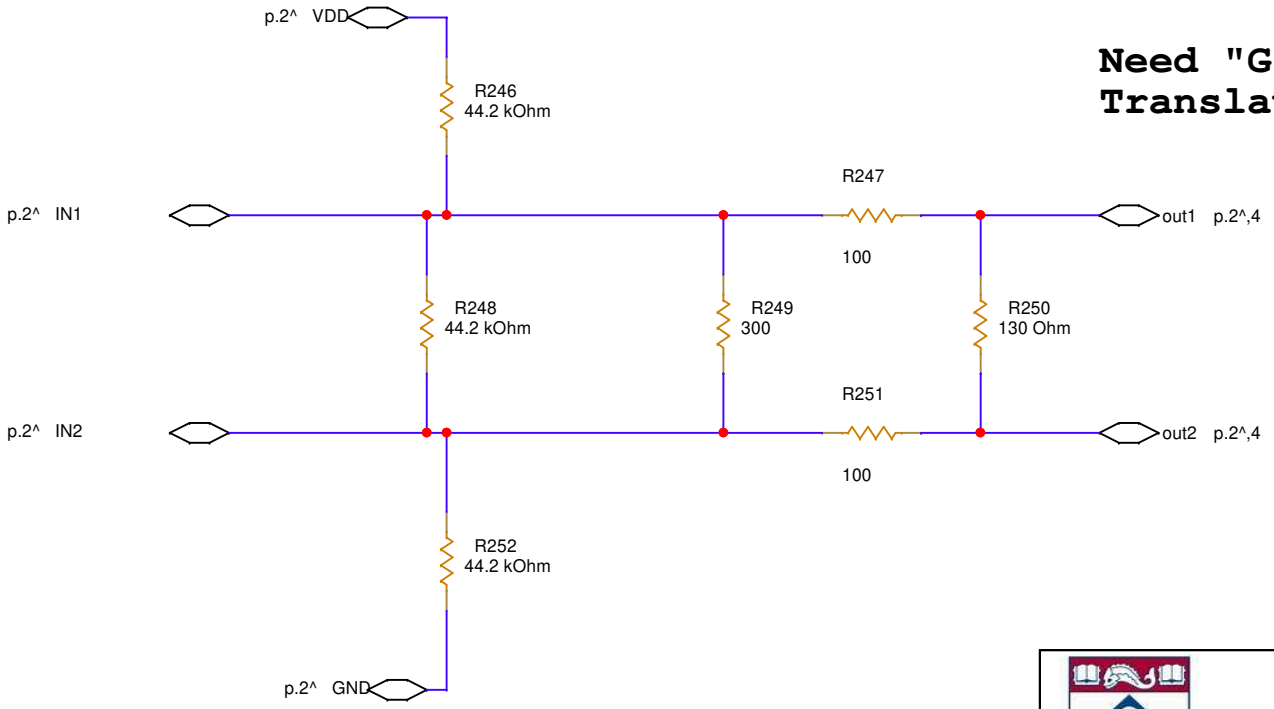

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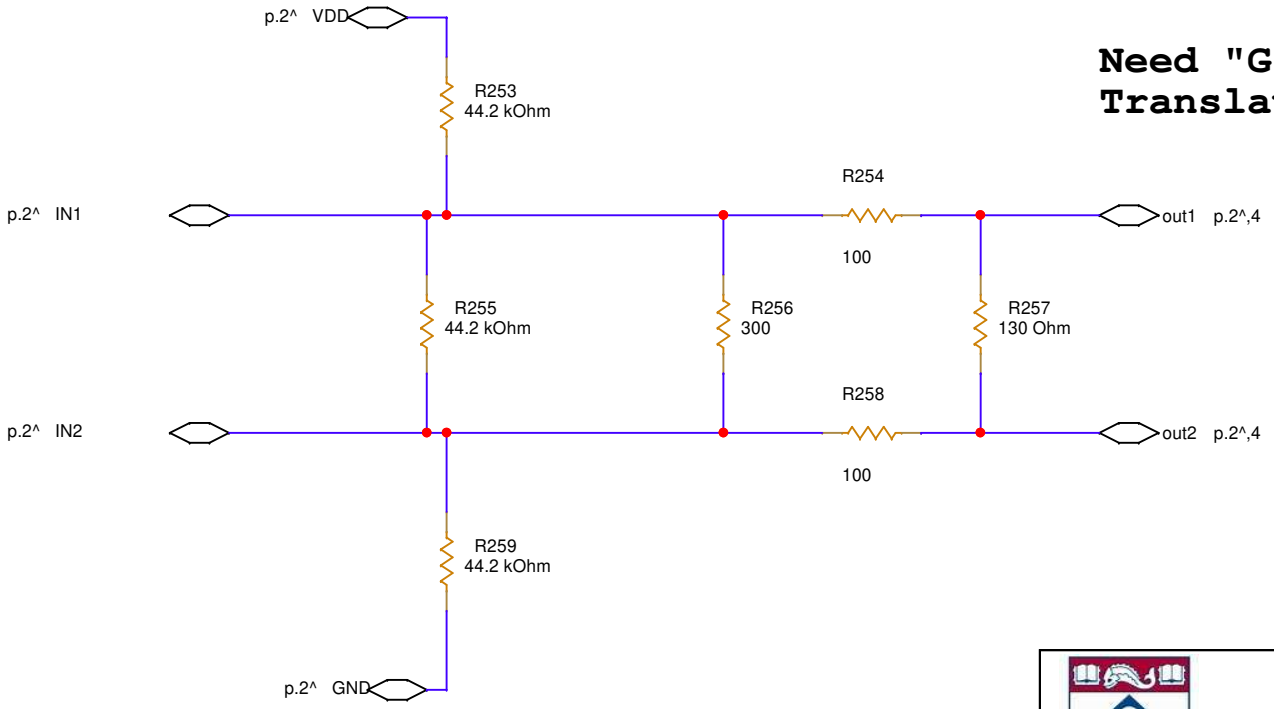

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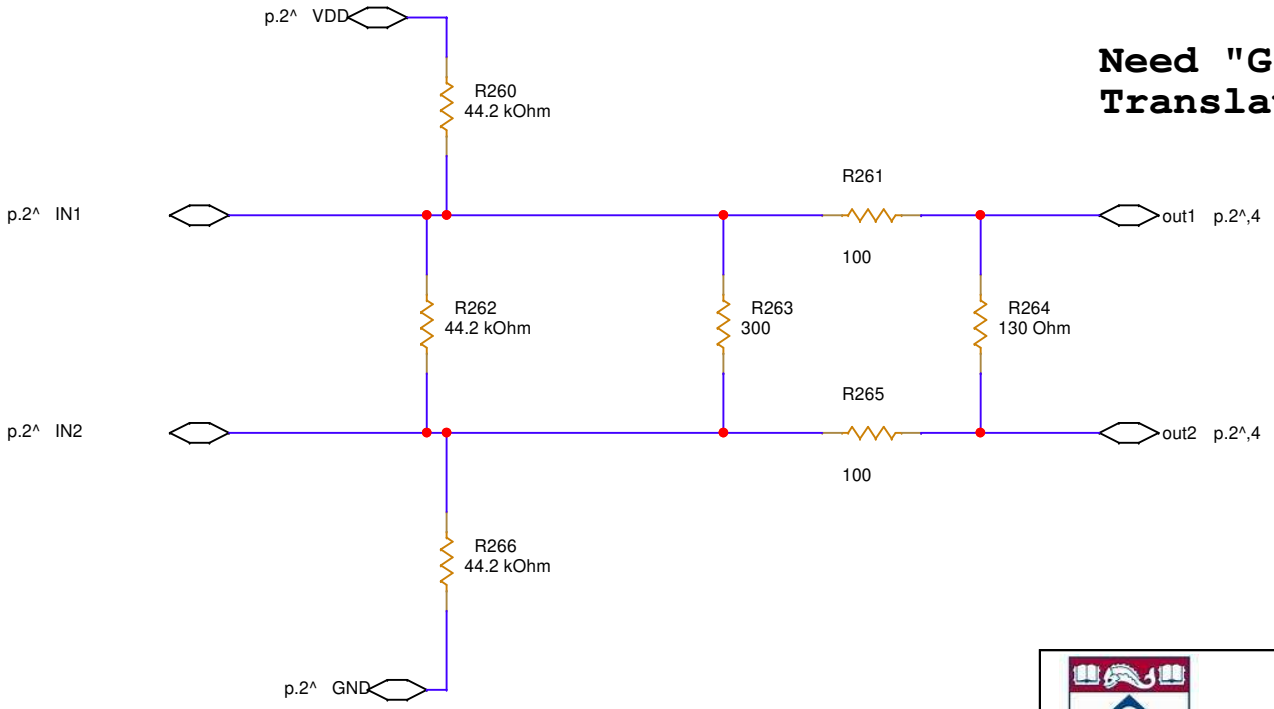

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