CHITTAGONG UNIVERSITY OF ENGINEERING AND TECHNOLOGY

DEPARTMENT OF ELECTRONICS AND TELECOMMUNICATION ENGINEERING

VLSI Technology Sessional

ETE 404

Project

BCD to Excess-3 Decoder

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Level: 04, Term: 01

Date of Submission: 10-11-2024

Full schematic view in cadence:

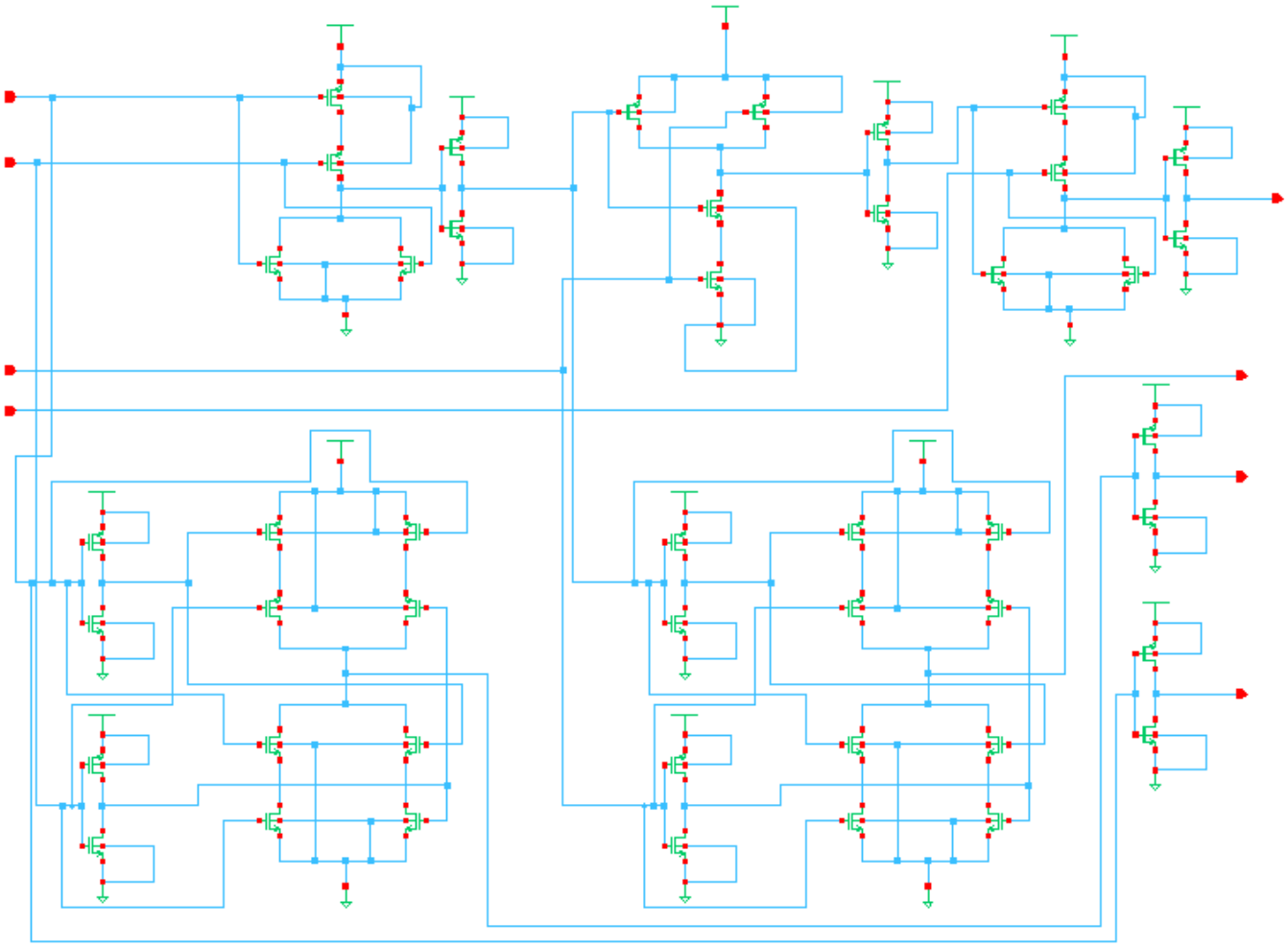

Fig. 1: Full schematic of BCD to Excess-3 Decoder

The Gates that are used:

NOT:

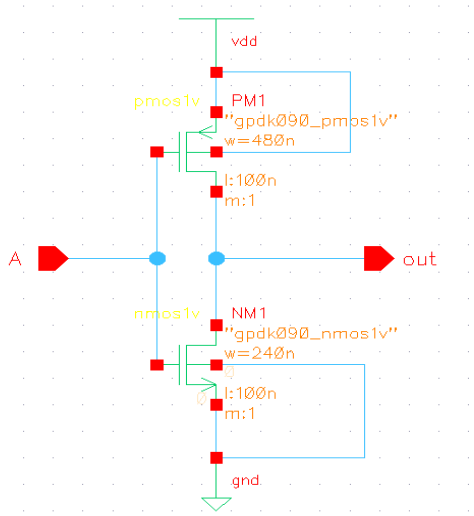

Fig. 2: Schematic of NOT gate

AND:

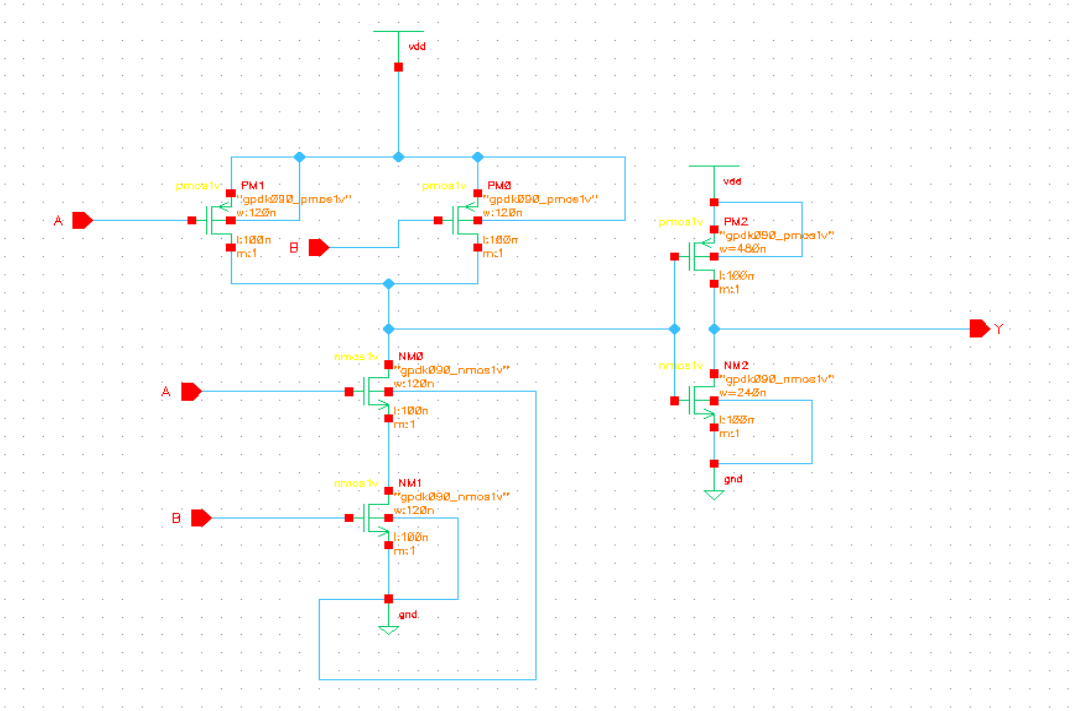

Fig. 3: Schematic of AND gate

OR:

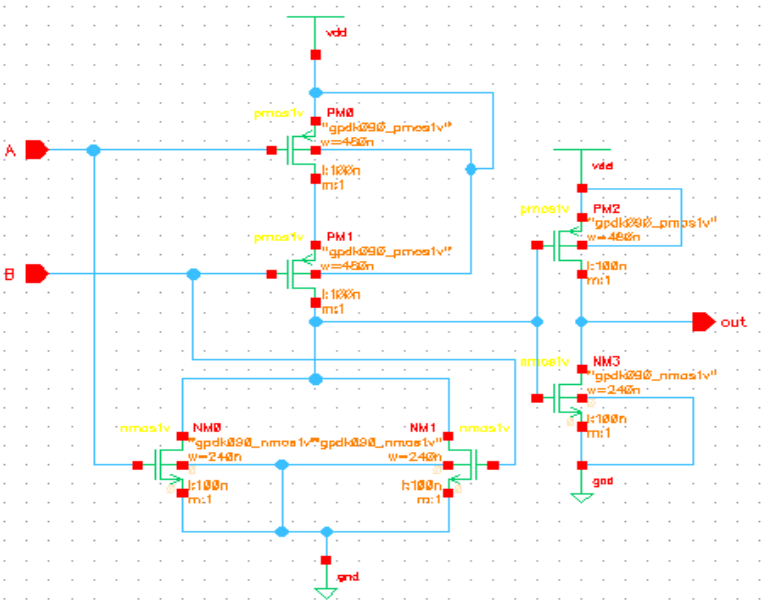

Fig. 4: Schematic of AND gate

X-OR:

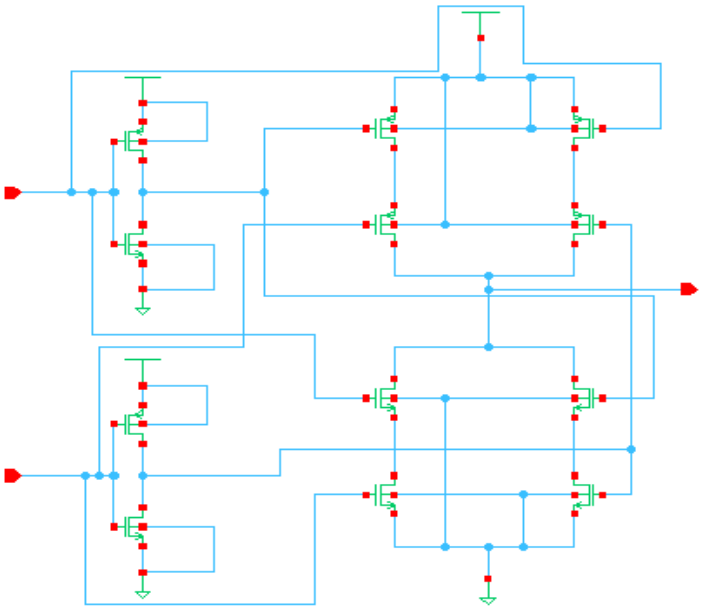

Fig. 5: Schematic of X-OR gate

OUTPUT:

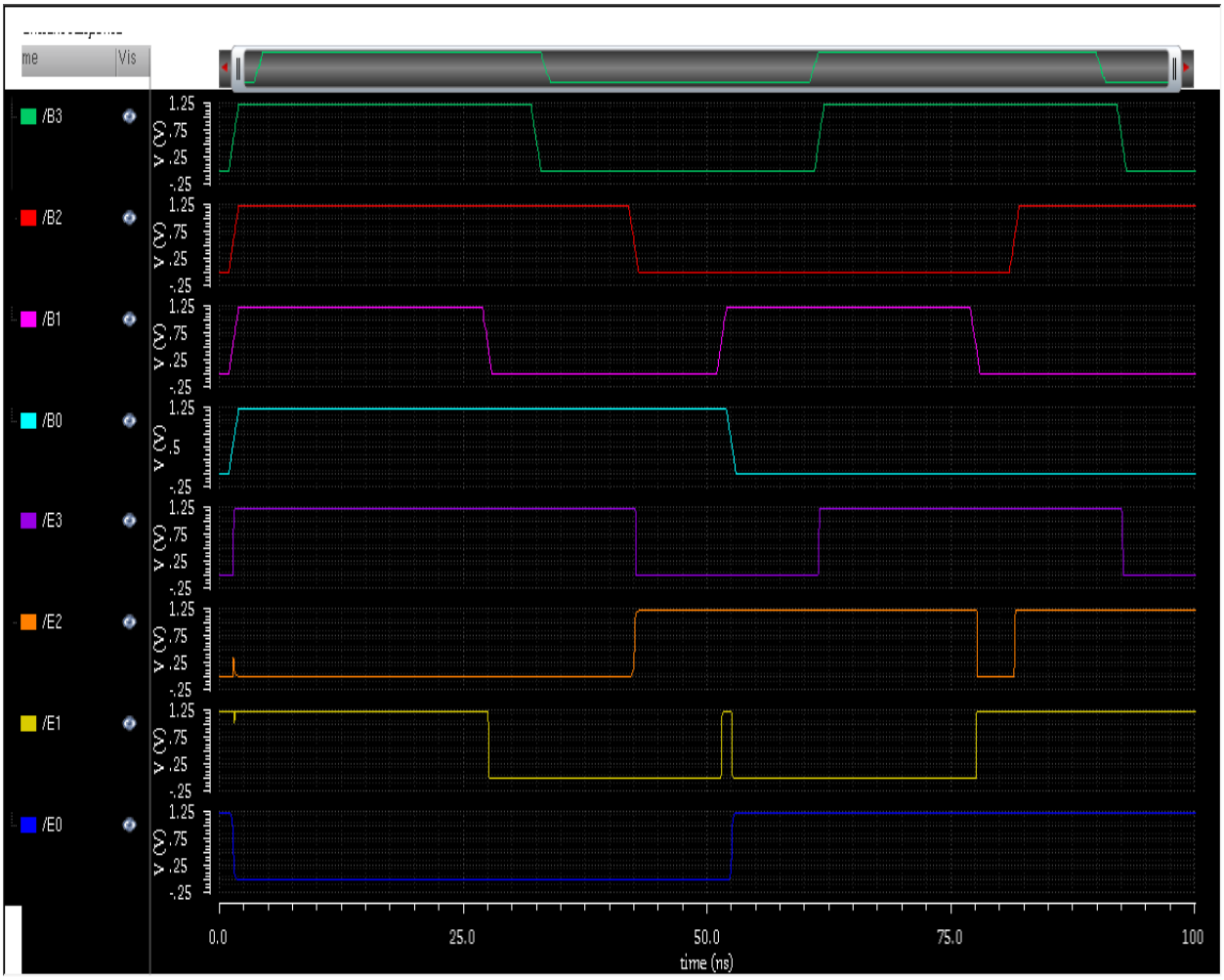

Fig. 6: Output of BCD to Excess-3 Decoder

Power graph:

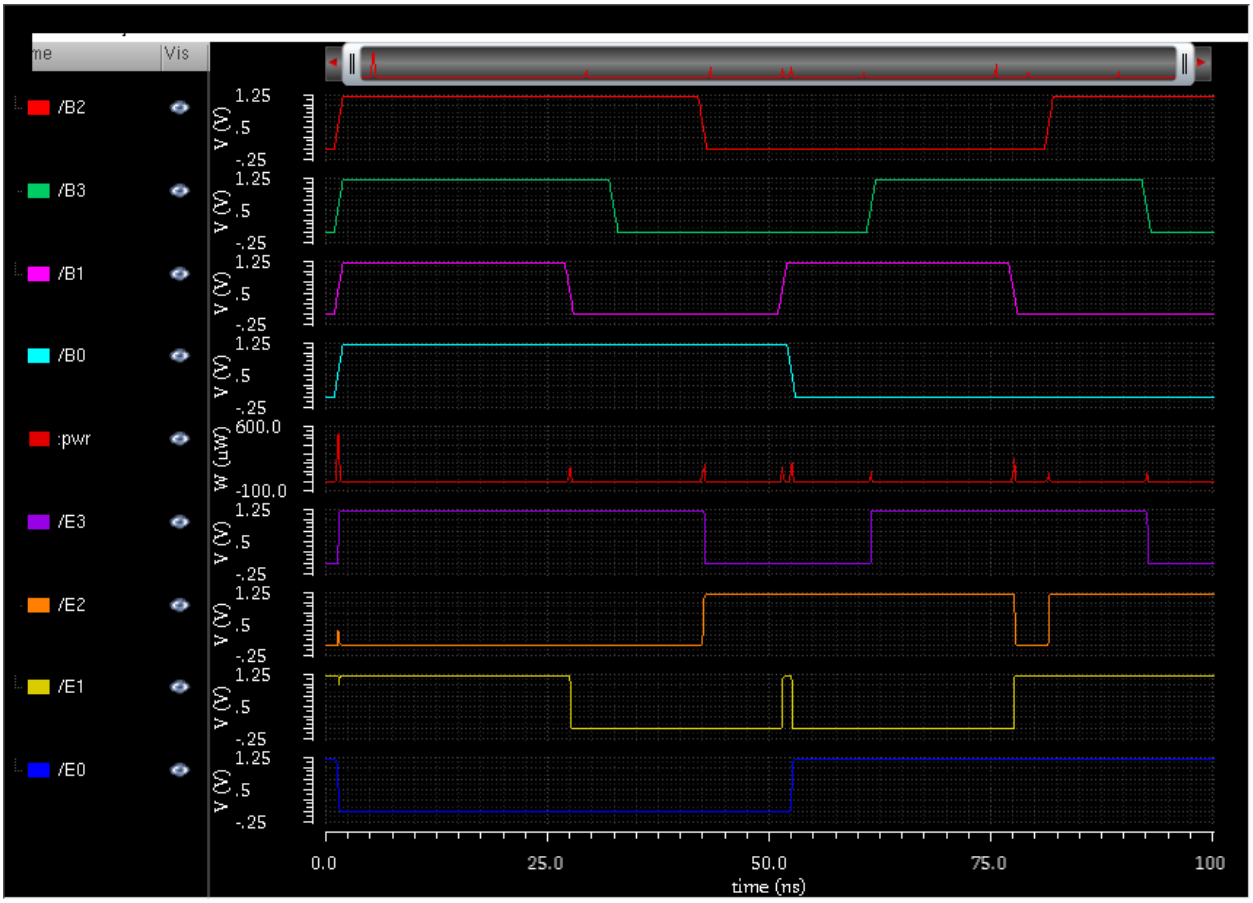

Fig. 7: Power graph of BCD to Excess-3 Decoder

Power measurement:

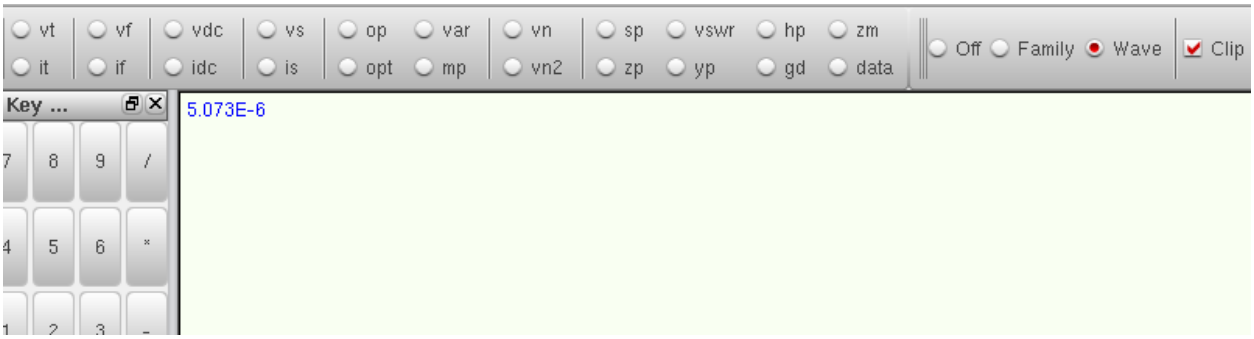

Fig. 8: Power measurement of BCD to Excess-3 Decoder