Audio Transmission And Reception over RF

Final MTP Phase-II

Electronic Systems

Anil Kumar Garg (173074018)

under the guidance of

Prof. Shalabh Gupta

Department of Electrical Engineering
Indian Institute of Technology, Bombay.

Jun 30 ,2020

Introduction

1. Access for gradually tapered spaces like ground tunnels and enemy occupied buildings is very difficult.
2. For solving this problem, a camera and audio receiver is mounted on trained animal.
3. Camera captures the images and sends back to the control center.
4. Control center sends the audio command to the animal via transmitter to receiver.
5. Trained animal performs the action as per command

Image Source: IITB EE Communication Lab Documents

Basic Audio Trans-Receiver

Block Diagram

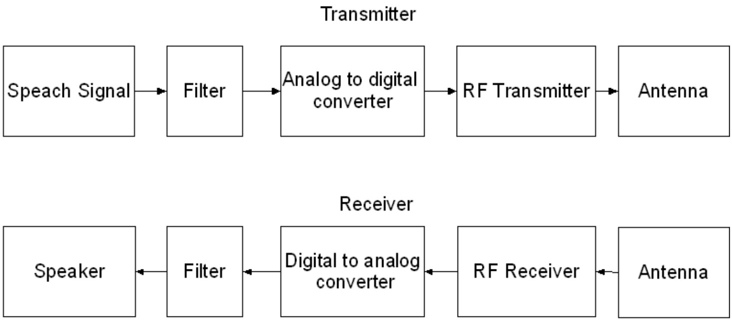


Figure: Audio on RF

Motivation

Problem??

1. ADC Resolution: **12bits** (Need 2 bytes to store the sampled value)
2. Considering ADC sampling rate **8000 samples/sec**
3. For 100 samples, capturing time is : **12.5 msec** ($100 \times 125\ \mu$ sec)
4. Considering RF data Transmitting bit Rate (symbol rate): **50 kbps**
5. If consider 14 bytes RF frame overheads then time required to transmit one RF packet : 34.2 msec $[\frac{214\times8}{50000}]$
6. Transmitting time > Sampled capturing time

Real time data transmission is not possible

Motivation

Solution??

1. ADC Resolution: **12bit** (Need 2 bytes to store the sampled value)
2. Considering ADC sampling rate **8000 samples/sec**
3. For 100 samples, capturing time is : **12.5 msec** ($100 \times 125\ \mu$ sec)
4. Considering RF data Transmitting bit Rate (symbol rate): **50 kbps**
5. Apply **compression technique** and convert 16 bits data into 4 bits encoded signal.
6. If consider 14 bytes RF frame overheads then time required to transmit one RF packet : 10.56 msec $[\frac{66 \times 8}{50000}]$
7. Transmitting time $<$ Sampled capturing time

Real time data transmission is now possible

Motivation

Proposal

1. For one to one data transfer from transmitter to receiver, symbol rate is required 200 kbps at 8000 sampling rate.
2. Using the technique of **ADPCM**, same data can be transferred with symbol rate 50 kbps.
3. 75% reduction in communication data bit-rate for same performance.
4. Effective task handling and processor utilization is required during implementation.
5. Fast ADPCM encoder- decoder algorithm for ARM controller at lower operating speed.
6. Synchronization between transmitter and receiver.

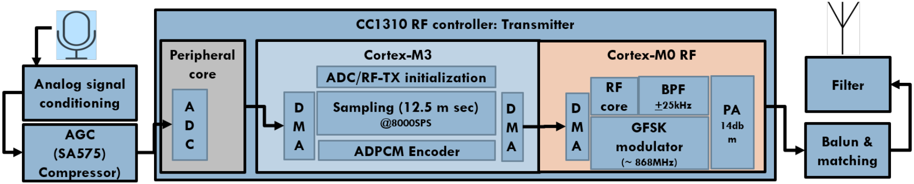
MTP Phase-2 Activities

Completed

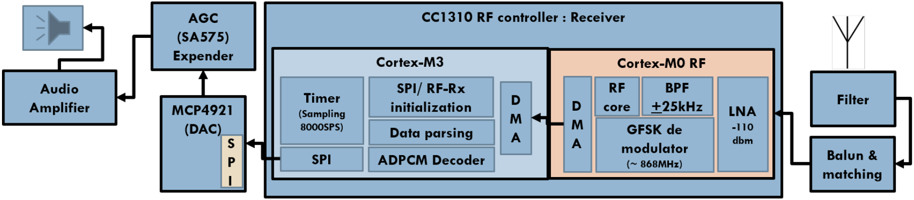
1. ADPCM technique implementation and testing
2. Implementation and testing at higher sampling rate (8kSPS)
3. Synchronization between transmitter and receiver
4. DAC interface with higher sampling
5. MIC interface and signal conditioning
6. Speaker interface with audio amplifier
7. Simulation and Prototype development
8. Design calculation and costing
9. Schematic design and BOM creation
10. Schematic design with **automatic gain controller**.
11. Testing and troubleshooting
12. Reporting,documentation and version control

System Block Diagram

Transmitter - Receiver



(a) Audio on RF Transmission



(b) Audio on RF Reception

Hardware Block Diagram

Transmitter

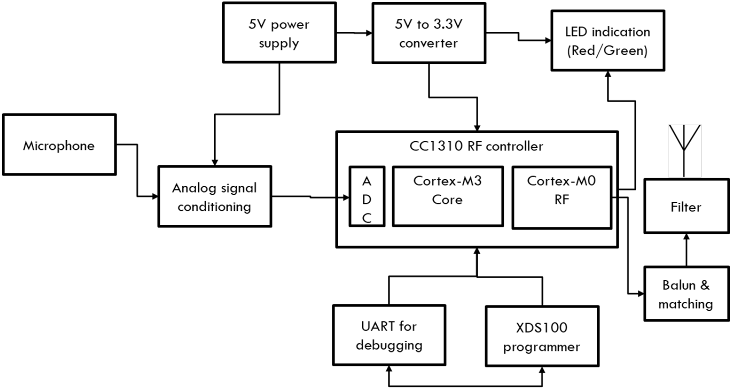


Figure: Audio on RF Transmission

Hardware Block Diagram

Receiver

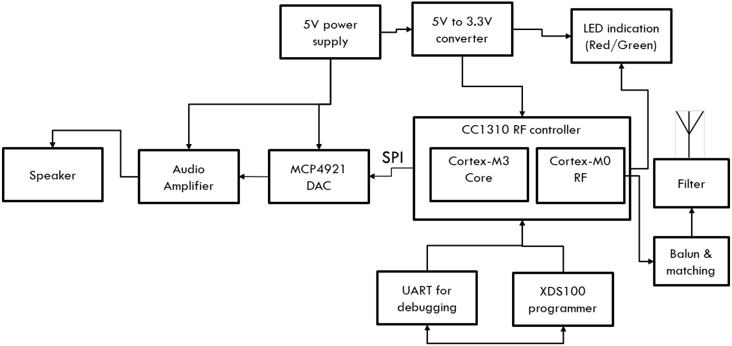
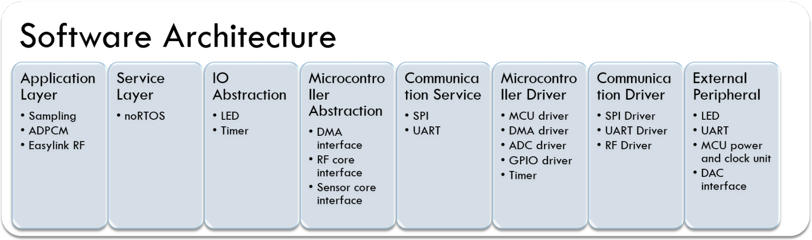


Figure: Audio on RF Reception

Software Architecture

Transmitter and Receiver

1. For Radio interface **RF Simplelink proprietary TI library** is used.
2. **ADPCM** technique is used for data compression and expansion.
3. **noRTOS** for avoiding extra processor overheads.
4. **DMA ping pong** mechanism for peripheral data transmission for better processor utilization.
5. **SmartRF studio** for RF command configuration.
6. Simultaneous processing of RF , main and sensor core.



RF Frame

EasyLink API reference and Frame Structure

RF Frame Transmission

1. EasyLink layer is initialized by calling **EasyLink_init()**.
2. TX is enabled by calling **EasyLink_transmitAsync()**
3. Entering TX can be immediate or scheduled
4. An Async operation can be cancelled with **EasyLink_abort()**

RF Frame Reception

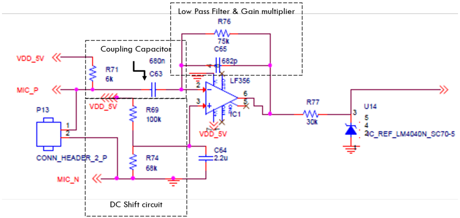
1. EasyLink layer is initialized by calling **EasyLink_init()**.
2. RX is enabled by calling **EasyLink_receiveAsync()**
3. Entering RX can be immediate or scheduled
4. An Async operation can be cancelled with **EasyLink_abort()**

Preamble	Syncword	Length	Address	Seq no	Code	Index	CRC
4B	4B	1B	1B	2B	50B	2B	2B

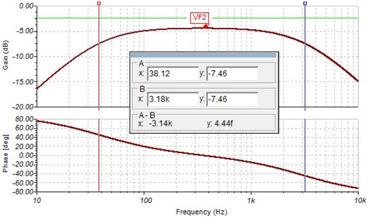
Analog Signal Conditioning

Schematic

1. Input coupling capacitor for DC blocking and passing signal above freq 40 Hz
2. A low pass filter of cutoff frequency 3 Khz in feedback circuit.
3. A 2V DC shift for uni-polar analog signal detection



(a) Mic Interfacing

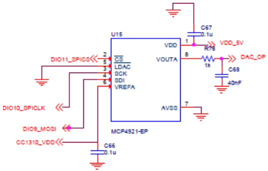


(b) Frequency Response

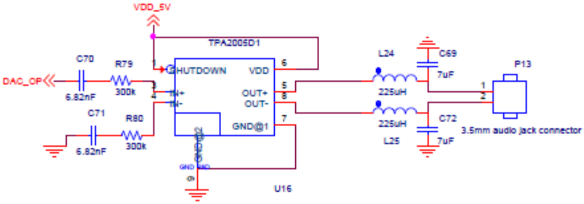
Audio Amplifier and LC Filter

Schematic

1. 12 bits resolution DAC with fast **settling time 4.5 μ sec**
2. TPA2005D1 Class D audio amplifier as audio driver with unity gain.
3. Audio amplifier and LC filter for pass-band **frequency range 75 Hz to 4 kHz**



(a) MCP4921 Interface

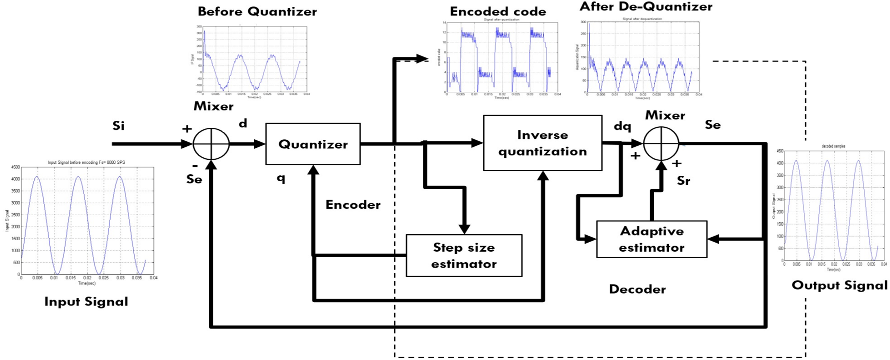


(b) Audio amplifier and LC filter

Adaptive Differential Pulse Code Modulation Technique

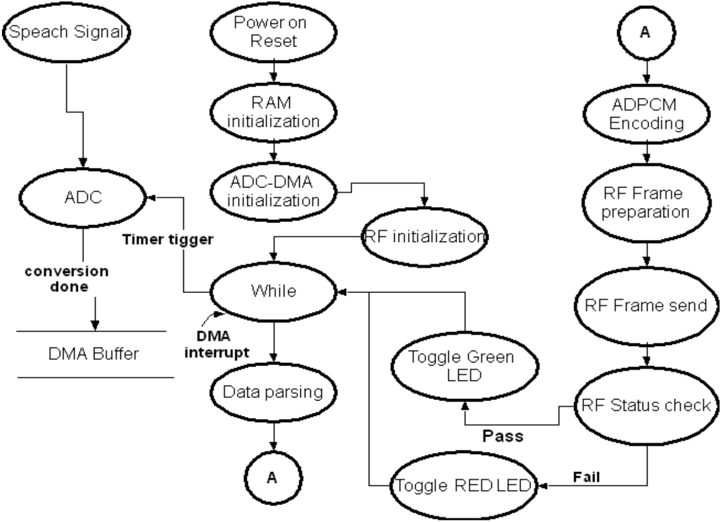
Code Generation and Decoding

1. Inbuilt decoder in encoder logic
2. Index and size of quantization is fixed in a **lookup table** during the initialization.
3. **Synchronization** between encoder and decoder.



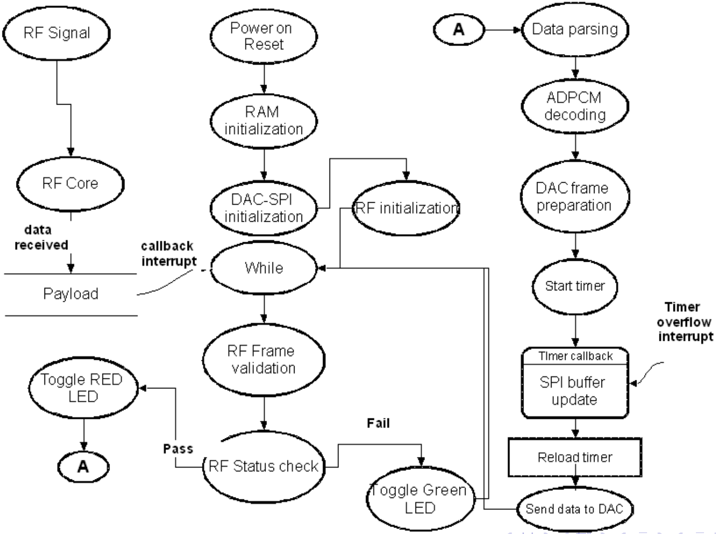
Data Flow Diagram

Transmitter



Data Flow Diagram

Receiver



Firmware Memory Utilization

Transmitter and Receiver

Name	Origin	Length	Used	Unused	% **Utilization**
FLASH	00000000	00020000	0000ae4a	000151b6	**34%**
SRAM	20000000	00005000	000019b0	00003650	**32%**

Table: Transmitter :CC1310 Memory utilization

Name	Origin	Length	Used	Unused	% **Utilization**
FLASH	00000000	00020000	0000b02e	00014fd2	**34%**
SRAM	20000000	00005000	00001a50	000035b0	**33%**

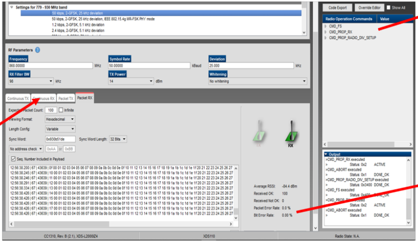
Table: Receiver :CC1310 Memory utilization

RF Range Test

Tested In Phase-1

1. Testing is done on uncompressed signal (Without ADPCM)
2. Able to detect signal up to -84.4 dbm as received signal strength indicator
3. Radio configuration and data testing has been done via **SmartRF studio** on fixed data stream.

Frequency: 868Mhz
Symbol rate: 50kbps
Deviation: 25 KHz
Rx filter BW: 96 kHz
Tx power : 14 dBm



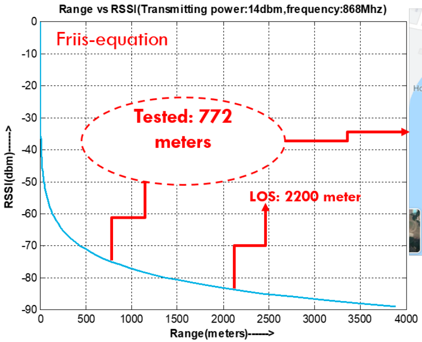
Radio operation commands:
1. CMD_FS
2. CMD_PROP_RX
3. CMD_PROP_RADIO_DEV_SETUP

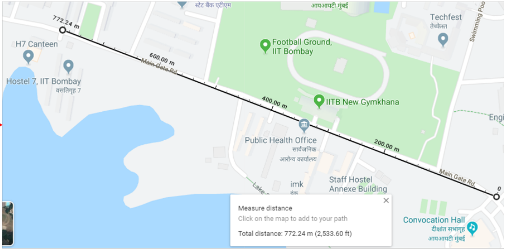
Average RSSI: -84.4 dBm
Received OK: 100
Received not OK: 0
Packet error rate: 0.0%
Bit error rate: 0.00%

RF Range Test

Tested In Phase-1

1. Range has been checked **H7 Canteen and convocation hall** inside IITB campus.
2. Testing has been done via **SmartRF studio** on fixed data stream.
3. Google map and GPS error is excluded in range value

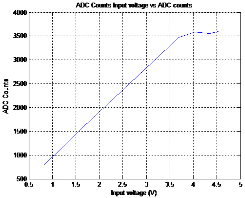




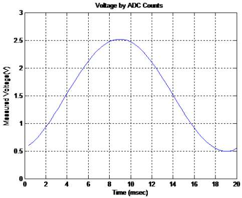
Test Setup

Analog Input vs ADC output

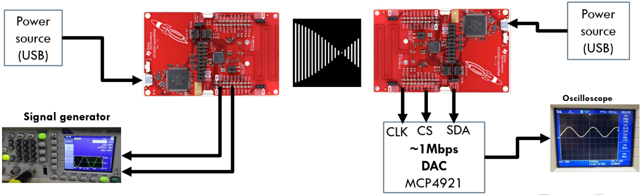
1. 12 bits ADC resolution with internal ref voltage 4.3V.
2. Fast ADC conversion time : 5 μseconds



(a) ADC with DC



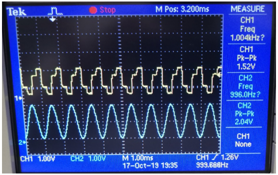
(b) ADC with AC



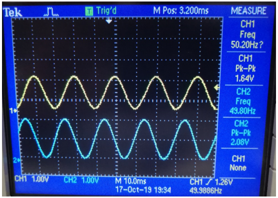
Prototype Testing

Transmitter Analog Input vs Receiver DAC output

1. Data captured at ADC sampling frequency 4kHz without delta modulation.
2. DAC output frequency: 1.004kHz @ 1.52 V_{PP}
3. ADC Input frequency: 1kHz @ 2 V_{PP} $\longrightarrow$



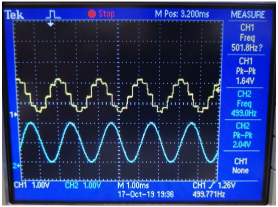
1. DAC output frequency: 50.2Hz @ 1.64 V_{PP}
2. ADC Input frequency: 50Hz @ 2 V_{PP} $\longrightarrow$



Prototype Testing

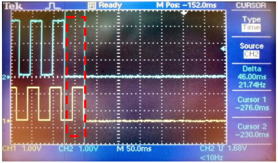
Transmitter Analog Input vs Receiver DAC output

1. Data captured at ADC sampling frequency 4kHz without delta modulation.
2. ADC Input frequency: 500Hz @ $2V_{PP}$
3. DAC output frequency: .502kHz @ $1.64V_{PP}$



Input - Output Delay:

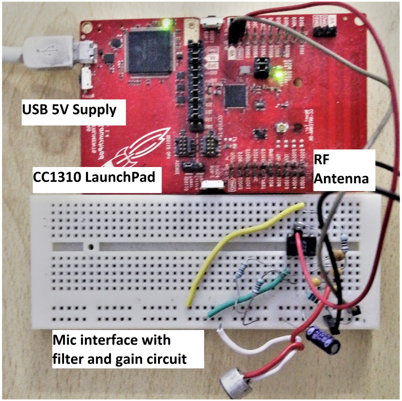
1. Input to output delay is 46 msec @4kSPS sampling rate.
2. Measured delay is improved up-to 30 msec in Phase 2 by increasing sampling rate @8kSPS.



Hardware Prototype

Transmitter

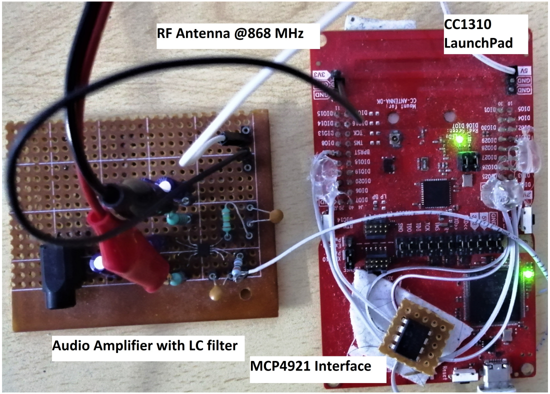
1. Final prototype with audio input and delta modulation encoder.
2. LED is indicating the healthiness of communication
3. Power supply is given by USB power bank.



Hardware Prototype

Receiver

1. Final prototype with audio output and delta modulation decoder.
2. LED is indicating the healthiness of communication
3. Power supply is given by USB power bank.

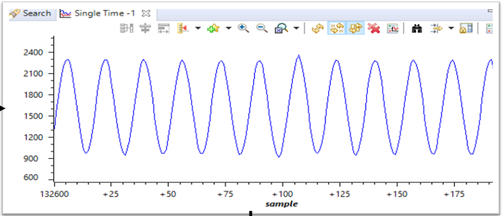


Modular Testing

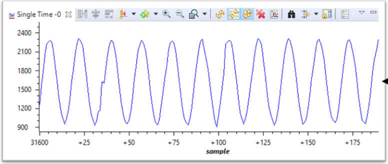
Transmitter: signal before encoder vs Receiver : signal after decoder

1. ADC and DAC sampling rate is 8KSPS.
2. Delta modulation is implemented during testing
3. Results are captured on CCS IDE developed by TI.

Input Injection from PC 3.5mm jack



Transmitter ADC Samples before ADPCM encoding



Receive Samples after ADPCM decoding

BOM and Costing

Transmitter

1. Total cost of electronics is coming approximately **10.38$**.
2. Cost is calculated as reference of DigiKey price from quantity 500 to 4K as per applicable.
3. Mechanical, PCB , Antenna , battery cost is excluded

Quantity	Parts	Cost ($)
1	LS L296-P2Q2-1 RLED	0.11821
1	LS LPL296-J2L2-25 GLED	0.11821
1	BLM18HE152SN1 Inductor	0.06619
1	LF356 Opamp	0.297
1	CC1310F128RGZT	4.8564
1	TPS79601DR	2.3403
1	LM4040N	0.5292
1	32.768kHz Xtal	0.77
1	24MHz Xtal	0.77
27	capacitors	0.04131
11	Resistors	0.01474
6	Indicators	0.4662

BOM and Costing

Receiver

1. Total cost of electronics is coming approximately **12.04$**.
2. Cost is calculated as reference of DigiKey price from quantity 500 to 4K as per applicable.
3. Mechanical, PCB , Antenna , battery cost is excluded

Quantity	Parts	Cost ($)
1	LS L296-P2Q2-1 RLED	0.11821
1	LS LPL296-J2L2-25 GLED	0.11821
1	BLM18HE152SN1 Inductor	0.06619
1	TPA2005D1	0.35
1	CC1310F128RGZT	4.8564
1	TPS79601DR	2.3403
1	MCP4921EP	1.49
1	32.768kHz Xtal	0.77
1	24MHz Xtal	0.77
1	3.5mm audio jack connector	0.4832
31	capacitors	0.0474
9	Resistors	0.0121
8	Indicators	0.6216

Practical Demonstration

https://www.youtube.com/watch?v=i4fzVxK4Fyc

Conclusion

- A prototype proof of concept is developed for audio transmission and reception.
- Delta modulation technique is implemented for utilizing same channel bandwidth (Symbol rate 50 kbps) with higher sampling rate (8kSPS).
- Hardware filter implementation for noise suppression.
- Prototype is tested up-to 750 meters line of sight at 14dbm power transmission via mono-pole PCB antenna
- Proprietary protocol to synchronize the transmitter and receiver during delta modulation
- Smart processor handling for effective utilization

Future Work

- Interfacing with automatics gain controller (companding circuit) and testing
- Can be replaced the DAC MCP4921 and driver circuit with **codec circuit** for better voice quality and noise suppression.
- High power and high efficient antenna designing to communicate between transmitter and receiver.
- Forward error correction (FEC) mechanism for frame auto correction for long range communication.
- PCB layout and product development testing with new hardware.

References

- "RF operation state chart" [Online][Accessed : Sep 20,2019] http://dev.ti.com/tirex/content/simplelink_cc13x0_sdk_1_30_00_06/docs/proprietary-rf/html/rf-core/execution-and-status-codes.html
- "callback events for CMD_PROP_RX" [Online], [Accessed : Sep 20,2019] http://dev.ti.com/tirex/content/simplelink_cc13x0_sdk_1_30_00_06/docs/ proprietary-rf/html/rf-core/callback-events.html.
- "Packet format" [Online], [Accessed : Sep 20,2019] http://dev.ti.com/tirex/content/simplelink_cc13x0_sdk_1_30_00_06/docs/ proprietary-rf/html/rf-proprietary/packet-format.html.
- "MCP4921/4922 12-Bit DAC with SPI™ Interface", Datasheet by Microchip Technology Inc. DS21897B-page 1 , 2007 Microchip Technology Inc.
- "Adaptive Differential Pulse Code Modulation Using PIC® Microcontrollers AN643", By Rodger Richey 2007 Microchip Technology Inc.. DS00643C-page 1

Q & A ??

Thank You!!!