```
// 2:1 Multiplexer
module mux_2_1(
  input sel,
  input i0, i1,
  output y
);
  assign y = (sel) ? i1 : i0;
endmodule

// Testbench
module mux_2_1_tb;
  reg i0, i1, sel;
  wire y;

  // Instantiate the MUX
  mux_2_1 uut(
    .sel(sel),
    .i0(i0),
    .i1(i1),
    .y(y)
  );

  initial begin
    $monitor("Time=%0t | sel=%b i0=%b i1=%b | y=%b", $time, sel, i0, i1, y);

    // Apply test cases
    i0 = 0; i1 = 1; sel = 0; #1;
```

```
    sel = 1; #1;
    i0 = 1; i1 = 0; sel = 0; #1;
    sel = 1; #1;

    $stop;
  end
endmodule
```