West Bengal State University

B.A./B.Sc./B.Com. (Honours, Major, General) Examinations, 2011

Part – III

COMPUTER SCIENCE — HONOURS

Paper - V

Duration : 4 Hours] [Maximum Marks : 100

Candidates are required to give their answers in their own words as far as practicable.

The figures in the margin indicate full marks.

Answer Q. No. **1** and any *five* from the rest taking at least *one* from each Group.

1. Answer any *ten* of the following : $10 \times 2 = 20$

a) Define loosely coupled and tightly coupled processors. To which category does distributed system belong ?

b) What do you mean by MIPS ?

c) Why is Displacement Addressing mode needed for 8085 microprocessor ?

d) What is the minimum size of ROM required to store the complete truth table of an 8×8 MUX ?

e) What are open collector and tri-state gates ?

f) Is the ROM an essential component to start up a PC ? Justify.

g) If $73_X = 54_Y$, what are the possible values of X and Y ?

h) What is Bus Idle Machine Cycle in 8085 MPU ?

i) What is the function of DAD Instruction in 8085 MPU ?

j) What is Cycle Stealing in DMA system ?

k) What is the advantage of multiplexing the address bus with data bus in 8085 MPU ?

l) How does the 8085 MPU come to know about the number of bytes to be fetched from memory to execute an insruction ?

m) What is locality of reference ? Where is it used ?

n) What is the advantage of Normalized floating point number ?

o) What is the role of Address Latch Enable (ALE) signal in 8085 MPU ?

GROUP - A

2. a) Explain the Instruction cycle highlighting the sub-cycles and sequence of steps to be followed.

b) Draw and explain the single-bus and three-bus organizations of the data path inside processor.

c) Explain the function to be performed by a typical I/O interface with a typical input or output interface.

d) Define pipelining. 5 + 6 + 3 + 2

3. a) The 8085 microprocessor has 16 address lines and 8 data lines, with the low-order 8-bits of the address multiplexed with the data lines. It is required to interface the 8085 with a 64 kB memory chip which has separate address and data lines. Show a schematic diagram for the connection, showing only the relevant signal lines.

b) For an I-O device that can transfer blocks of data at very high speed, there are two alternative modes of data transfer : using interrupt-driven and DMA transfer mode. Which of the two alternatives would you choose and why ?

c) Draw a schematic diagram of a 2's complement adder/subtractor, using a normal parallel adder and gates as basic building blocks. 6 + 6 + 4

4. a) Define instruction stream. Explain with a logical diagram of interrupt cycle during execution of a program.

b) A 2-D RAM has N storage cells organized as N_X rows and N_Y columns. The number of address drivers needed is $N_X + N_Y$.

If $N = M^2$, where M is an integer, that is N is a perfect square, show that the number of address drivers needed is a minimum iff $N_X = N_Y = M$.

c) Why is 0-address instruction needed ? Explain with a suitable example. Is there any relation of Stack pointer to handle the above instruction ? Justify.

(2 + 4) + 6 + (2 + 2)

5. a) What do you mean by bit-sliced ALU ? Draw the logic diagram of a 16-bit sliced ALU composed of 4-bit slices and explain its operations.

b) How quickly can a CLA (ALU) add two 32-bit operands ? Illustrate with the help of a suitable diagram.

c) Distinguish between *n*-bit carry save adder and carry look ahead adder.

d) Design and explain a suitable circuit that performs multiplication of two signed integers. What is the complexity of the above algorithm ? (2 + 4) + 3 + 2 + 5

6. a) Assume that the accumulator contains FBH and register D contains CDH. What will be the contents of the accumulator for (AC) and flags (Z) and carry (CY), when following instruction is executed ?

i) ADD B

ii) XRA A

iii) ORA 8 CH.

b) Clearly explain, how an Interrupt Service Routine is invoked after an interrupt signal is received on the INTR of 8085.

c) If the access times of the main memory and the cache are 50 ns and 10 ns respectively, and the cache hit ratio is 0·96, what will be the effective memory access time ?

d) Differentiate between Software and Hardware interrupt. 3 + 5 + 4 + 4

GROUP – B

7. a) What is the advantage of digital transmission over analog transmission ?

b) What do you mean by digital to analog modulation ?

c) Discuss different mechanisms for modulating digital data into an analog signal.

d) Give an example where bit rate and baud rate both are the same.

e) Why cannot we use a LAN protocol like the Ethernet for use in a WAN ?

2 + 2 + 8 + 2 + 2

8. a) Write an algorithm and describe with example how checksum detects error.

b) How does FDM combine multiple signals into one ?

c) What is the relationship between the number of slots in a frame and the number of input lines for TDM ?

d) What is the advantage of shielded twisted pair over unshielded twisted pair cable ?

e) Give a description of infrared signal. 6 + 3 + 2 + 2 + 3

9. a) What is the advantage of layered architecture ?

b) Briefly describe the functions of data link layer, transport layer and physical layer in OSI model.

c) What is the advantage of star topology over mesh topology ?

d) What is Delta Modulation ? Where is it used ? 2 + 8 + 4 + 2

10. a) What is transmission impairment ? Discuss briefly different types of transmission impairments.

b) What is Channel Capacity ? What key factors affect the channel capacity ?

c) Which media are used for satellite communication ? Describe their characteristics. (2 + 6) + (2 + 2) + (1 + 3)

11. a) Distinguish between circuit switching and packet switching.

b) What are the different approaches to packet switching network ? Describe each briefly.

c) Compare UDP and TCP.

d) Explain the operation of Token ring. 3 + (1 + 4) + 4 + 4

GROUP – C

12. Write short notes on any *four* of the following : 4 × 4

a) CSMA / CD protocol

b) Web Browser *vs* Web Server

c) IIS

d) Broadcasting

e) Video Chat

f) HTTP *vs* FTP.