# GCNear: A Hybrid Architecture for Efficient GCN Training with Near-Memory Processing

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Abstract—Recently, Graph Convolutional Networks (GCNs) have become state-of-the-art algorithms for analyzing non-euclidean graph data. However, it is challenging to realize efficient GCN training, especially on large graphs. The reasons are many-folded: 1) GCN training incurs a substantial memory footprint. Full-batch training on large graphs even requires hundreds to thousands of gigabytes of memory to buffer the intermediate data for back-propagation. 2) GCN training involves both memory-intensive data reduction and computation-intensive features/gradients update operations. Such a heterogeneous nature challenges current CPU/GPU platforms. 3) The irregularity of graphs and the complex training dataflow jointly increase the difficulty of improving a GCN training system's efficiency.

This paper presents GCNear, a hybrid architecture to tackle these challenges. Specifically, GCNear adopts a DIMM-based memory system to provide easy-to-scale memory capacity. To match the heterogeneous nature, we categorize GCN training operations as memory-intensive Reduce and computation-intensive Update operations. We then offload Reduce operations to on-DIMM NMEs, making full use of the high aggregated local bandwidth. We adopt a CAE with sufficient computation capacity to process Update operations. We further propose several optimization strategies to deal with the irregularity of GCN tasks and improve GCNear's performance. Comprehensive evaluations on twelve GCN training tasks demonstrate that GCNear achieves  $24.8 \times$  /  $2.2 \times$  geomean speedup and  $61.9 \times$  /  $6.4 \times$  (geomean) higher energy efficiency compared to Xeon E5-2698-v4 CPU and NVIDIA V100 GPU. To deal with deep GCN models and the ever-increasing graph scale, we also propose a Multi-GCNear system. Compared to state-of-the-art Roc and DistGNN systems, Multi-GCNear achieves up to  $2.1\times$  and  $3.1\times$  higher training speed, respectively.

#### I. INTRODUCTION

In recent years, Graph Convolutional Network (GCN) has emerged as a state-of-the-art algorithm to analyze non-euclidean graph data. Given a graph, a GCN model gets the vertex-level representation with several stacked GCN layers. In each layer, all the vertexes first aggregate their neighbors' hidden features, then use one or more fully-connected layers to transform the features and produce the outputs. The final layer's features are treated as the vertex-level representations, which can be used on various down-stream tasks, such as node classification [1]–[3], point-cloud [4]–[7], recommendation systems [8]–[12], smart traffic [13]–[15], IC design [16]–[18], physical system simulation [19], and chemical prediction [20].

Various GCN accelerators have been proposed to accelerate GCN inference [21]–[29]. However, existing accelerators and GPU/CPU platforms do not easily support GCN training at scale because GCN training tasks have many peculiar challenges. Firstly, GCN training incurs a large memory footprint. To enable back-propagation, we have to buffer a huge amount

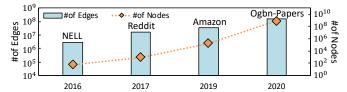


Fig. 1. Trend of increasing graph scale used for GCN research.

of intermediate data. Even the middle-scale Reddit dataset [30] containing 114 million edges will take up 58 GB of memory using PyG-GPU framework [31], exceeding most GPUs' capacity. In the meanwhile, as illustrated in Figure 1, the scale of graphs applied in GCN researches has been growing exponentially in recent years [3], [30], [32], [33]. Though mini-batch training strategies based on neighbor-sampling strategies [30], [32], [34], [35] can reduce the memory requirement, they are proved to have lower accuracy compared to full-batch training due to approximation errors [30], [36]–[39].

Secondly, GCN training has both memory-intensive (e.g. 0.5 Ops/Byte) features/gradients reduction and computation-intensive (e.g. 256 Ops/Byte) features/gradients update operations. Neither PIM/NMP-based graph processing accelerators [40]–[44] (optimized for memory access) nor traditional DNN accelerators [45]–[50] (optimized for computation) can well-handle such a discrepancy in GCN training. Thirdly, the complex GCN training dataflow, along with the irregularity of real-world graphs (e.g., the sparse connectivity and diverse input feature dimensions of graphs), jointly increase the difficulty of optimizing a GCN training system's efficiency.

To tackle these challenges, we propose GCNear, a novel hybrid architecture that harnesses both near-memory processing (NMP) and centralized processing to achieve high-throughput, energy-efficient, and scalable GCN training on large graphs. Specifically, we make the following contributions in this paper:

- We analyze the full-batch GCN training procedure in detail to reveal its large memory footprint and the heterogeneous nature of training operations. We then categorize the involved operations as memory-intensive Reduce and computation-intensive Update operations. (Section III)
- We propose GCNear, the first hybrid GCN training accelerator leveraging both DIMM-based Near-Memory Engines (NMEs) and a Centralized ASIC Engine (CAE) to provide easy-to-scale memory capacity and match the heterogeneous nature of GCN training. We offload Reduce operations to NMEs to take full advantage of the high aggregated local bandwidth. For computation-intensive Update operations,

CAE provides sufficient computation capacity. (Section IV)

- To deal with irregular input graphs and further improve GCNear's performance, we elaborate on the training flow and propose several optimizations involving data reuse, data mapping and dataflow scheduling, etc. We also propose a Multi-GCNear system to tackle the emerging super-large graphs and deep models. (Section V&VII-A)
- We conduct extensive experiments on various GCN training tasks to validate the superiority of GCNear over commercial CPU/GPU platforms. We also compare the proposed Multi-GCNear system with two state-of-the-art distributed training systems Roc and DistGNN. (Section VI&VII-A)

On twelve different GCN training tasks, GCNear achieves  $24.8\times$  /  $2.2\times$  geomean speedup and  $61.9\times$  /  $6.4\times$  higher energy efficiency (geomean) compared to Xeon E5-2698-v4 CPU and NVIDIA V100 GPU. Compared to the distributed training systems Roc [37] and DistGNN [36], Multi-GCNear also shows up to  $2.1\times$  and  $3.1\times$  speedup, respectively.

## II. BACKGROUND

#### A. Notations

Notation	Description
$V, E$ $\mathcal{N}(v)$	Sets of vertexes and edges The neighbors of vertex $\boldsymbol{v}$
$ \begin{array}{c} \mathcal{N}(v) \\ \tilde{\mathcal{N}}(v) \\ D_v \\ L \end{array} $	The set containing $v$ and $v$ 's neighbors: $\{\mathcal{N}(v)\} \cup \{v\}$ The degree of vertex $v$ Total layers in the model
$egin{array}{c} h_v^l \ d^l \ a_v^l \end{array}$	Hidden feature vector of vertex $v$ at the $l$ -th layer Hidden feature vectors' dimension at the $l$ -th layer
$W^l$	Aggregated feature vector of vertex $v$ at the $l$ -th layer Weight matrix in layer $l$
$z_v^l$ $\sigma$	Pre-activation feature, namely $a_v^l \cdot W^l$ Activation function, e.g. ReLU
$rac{\mathcal{L}}{\delta_v^l}$	The loss value calculated with outputs and labels  The gradients of $h_v^l$ , namely $\frac{\partial \mathcal{L}}{\partial h_v^l}$
$rac{\delta_v^l}{\widehat{\delta}_v^l},$	Masked gradients of $h_v^l\colon \delta_v^l\odot\sigma'(z_v^l)$ Aggregated masked gradients for vertex $v$

To facilitate the discussion of GCN algorithms, we summarize the used notations in Table I. Assume that we train on an input graph G=(V,E), where V and E are sets of vertexes and edges. We denote the neighbors of vertex v as  $\mathcal{N}(v)$  and the degree of vertex v as  $D_v$ . There are in total L layers in a GCN model. In the l-th layer, there is a trainable weight matrix  $W^l$ . We denote the hidden feature vector of vertex v at layer l as  $h^l_v$ . Other notations will be described later.

#### B. GCN Forward

Generally, a Graph Convolutional Network is composed of several GCN layers. Each GCN layer computes with two separated steps: a neighbor aggregation step and a feature combination step. Their operations are abstracted as follows:

$$a_v^l = \text{Aggregate}(h_u^{l-1} | u \in \widetilde{\mathcal{N}}(v)) \tag{1}$$

$$h_v^l = \text{Combine}(a_v^l) \tag{2}$$

The aggregation step gathers each vertex v's neighbors and uses an aggregator function to merge the features, while the

combination step transforms the features with one or more fully-connected layers. For the example in Figure 2, a classic GCN [3] adopts *Weighted Sum* as the aggregator (step (1)):

$$a_v^l = \sum_{u \in \widetilde{\mathcal{N}}(v)} \frac{1}{\sqrt{D_v D_u}} h_u^{l-1} \tag{3}$$

The edge's weight is calculated with degrees of both source and destination vertexes, and  $a_v^l$  denotes the aggregation result. In combination steps (e.g., step ②), a learnable weight matrix  $W^l$  transforms  $a_v^l$ , followed by an activation function  $\sigma$ :

$$h_v^l = \sigma(a_v^l \cdot W^l) \tag{4}$$

The l-th layer's outputs  $h_v^l$  then serve as the inputs of layer l+1. By stacking L such layers (step  $(1)\sim(4)$ ), a GCN model can capture L-hop information from the input graph. Features of the final layer are read out and used on several downstream tasks such as node classification and graph classification.

#### C. GCN Backward

We take node classification as a representative task. After forward, we calculate the cross-entropy loss on a labeled graph G containing N vertexes with Equation 5, where  $y_v$  and  $h_v^L$  denote vertex v's label and output feature vector.

$$\mathcal{L} = \frac{1}{N} \sum_{v=1}^{N} CrossEntropyLoss(h_v^L, y_v)$$
 (5)

After computing  $\mathcal{L}$  (step ③), we want to derive each layer's weight gradients. For this goal, we first compute the gradients of each layer's hidden features. The last layer's gradients can be calculated according to the loss function (step ⑥). For the other layers, we compute  $\frac{\partial \mathcal{L}}{\partial h_v^l}$ , namely  $\delta_v^l$  using the chain-rule:

$$\delta_{v}^{l} = \frac{\partial \mathcal{L}}{\partial h_{v}^{l}} = \sum_{u \in \widetilde{\mathcal{N}}(v)} \frac{\partial \mathcal{L}}{\partial h_{u}^{l+1}} \cdot \frac{\partial h_{u}^{l+1}}{\partial h_{v}^{l}} = \sum_{u \in \widetilde{\mathcal{N}}(v)} \delta_{u}^{l+1} \cdot \frac{\partial h_{u}^{l+1}}{\partial h_{v}^{l}}$$

$$= \sum_{u \in \widetilde{\mathcal{N}}(v)} \delta_{u}^{l+1} \odot \sigma'(z_{u}^{l+1}) \cdot \frac{1}{\sqrt{D_{u}D_{v}}} \cdot W^{l+1^{T}}$$

$$= (\sum_{u \in \widetilde{\mathcal{N}}(v)} \frac{1}{\sqrt{D_{u}D_{v}}} \widehat{\delta}_{u}^{l+1}) \cdot W^{l+1^{T}}$$
(6)

If ReLU activation function is adopted,  $\sigma'(z_v^l)$  serves as a binary mask. We denote the masked gradients  $\delta_v^l \odot \sigma'(z_v^l)$  as  $\widehat{\delta}_v^l$ , which can be derived recursively (steps  $\widehat{\bigcirc}$  and  $\widehat{\bigcirc}$ ):

$$\widehat{\delta}_{v}^{l} = \left(\sum_{u \in \widetilde{\mathcal{N}}(v)} \frac{1}{\sqrt{D_{u}D_{v}}} \widehat{\delta}_{u}^{l+1}\right) \cdot W^{l+1^{T}} \odot \sigma'(z_{v}^{l}) \tag{7}$$

After that, l-th layer's weight gradients, namely  $\frac{\partial \mathcal{L}}{\partial W^l}$  can be derived as follows (e.g., the bottom formulation of step \$):

$$\frac{\partial \mathcal{L}}{\partial W^{l}} = \sum_{v=1}^{N} \frac{\partial z_{v}^{l}}{\partial W^{l}} \cdot \frac{\partial \mathcal{L}}{\partial z_{v}^{l}} = \sum_{v=1}^{N} a_{v}^{l^{T}} \cdot \frac{\partial \mathcal{L}}{\partial h_{v}^{l}} \cdot \frac{\partial h_{v}^{l}}{\partial z_{v}^{l}} 
= \sum_{v=1}^{N} a_{v}^{l^{T}} \cdot \delta_{v}^{l} \odot \sigma'(z_{v}^{l}) = \sum_{v=1}^{N} a_{v}^{l^{T}} \cdot \hat{\delta}_{v}^{l}$$
(8)

The weight gradients are used to update the model weights through gradient descent:  $W^l = W^l - \eta \frac{\partial \mathcal{L}}{\partial W^l}$ , where  $\eta$  denotes the learning rate. Such a training process iterates for several epochs until the model training reaches convergence.

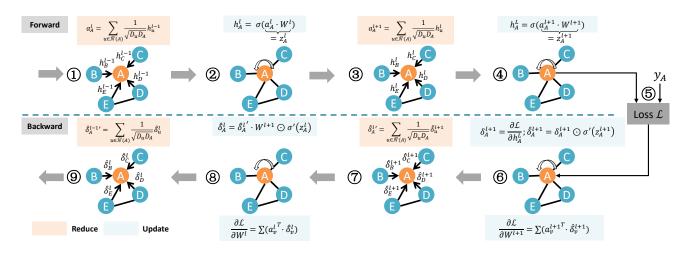


Fig. 2. Computation flow of GCN training. ①③: Forward aggregation. ②④: Forward combination. ⑤: Loss computation. ⑥⑧: Feature/weight gradients computation. ⑦⑨: Feature gradients aggregation. Operations marked with orange and blue denote Reduce and Update operations, respectively.

TABLE II			
VARIANTS	OF	GCNS	

Variant	Aggregation	Combination
GCN [3]	$a_v^l = \sum_{u \in \tilde{\mathcal{N}}(v)} \frac{1}{\sqrt{D_v * D_u}} h_u^{l-1}$	$Relu(a_v^l \cdot W^l)$
GIN [51]	$a_v^l = (1 + \epsilon) \cdot h_v^l + \sum_{u \in \mathcal{N}(v)} h_u^l$	$\boxed{\mathit{MLP}^l(a_v^l, W^l, b^l)}$
SAGEConv [30]	$a_v^l = Mean(h_u^l   u \in \widetilde{\mathcal{N}}(v))$	$Relu(a_v^l, \cdot W^l)$
GAT [11]	$ \begin{vmatrix} \alpha_{vu} = Softmax(\sigma(\mathbf{a}^T[W_1^l h_v^l    W_2^l h_u^l])) \\ a_v^l = \sum_{u \in \widetilde{\mathcal{N}}} \alpha_{uv} \cdot h_u^l \end{vmatrix} $	$\boxed{Elu(a_v^l \cdot W^l)}$

In Figure 2, operations are marked with orange and blue. We categorize them as Reduce (data reduction operations along edges) and Update (vertex-centric features/gradients transformation) operations and demonstrate that they have distinct computational characteristics in section III.

#### D. Variants of GCNs

Apart from the classic GCN, several GCN variants are also proposed. We list three representative variants in Table II. Among them, GIN [51] and SAGEConv [30] use Sum and Mean operators for aggregation. GAT [11] leverages a selfattention mechanism to implement its aggregator. It first calculates the attention coefficient  $\alpha_{uv}$ , which measures the importance of vertex v to v's neighbor u. Then the aggregation results are the weighted sum of neighbors' features. Except for GIN, which adopts Multi-Layer-Perception (MLP) for combination, both SAGEConv and GAT use a single fully-connected layer for combination. We omit the backward formulations, but it is easy to find that the operations of these GCN variants are also composed of data-reduction operations along edges and vertex-centric features/gradients update operations. Without loss of generality, we still use the classic GCN as the representative example to continue our discussions.

## E. Full-batch Training VS. Mini-batch Training:

On real-world tasks, the input graphs can be too large to train on a single GPU. Mini-batch training is then proposed

IABLE III								
	BUFFERI	ED VARI	ABLES I	DURING	TRAIN	ING		
Step	1 1 2	③	(	4)	(	6)	7	8
Buffered Variables	$\begin{vmatrix} a_v^l & a_v^l \\ a_v^l & z_v^l \\ h_v^l \end{vmatrix}$	$\begin{vmatrix} a_v^l \\ z_v^l \\ a_v^{l+1} \end{vmatrix}$	$\begin{vmatrix} a_v^l \\ z_v^l \\ a_v^{l+1} \end{vmatrix}$	$\begin{array}{c} z_v^{l+1} \\ h_v^L \end{array}$	$\begin{vmatrix} a_v^l \\ z_v^l \\ a_v^{l+1} \end{vmatrix}$	$\widehat{\delta}_v^{l+1}$	$\begin{vmatrix} a_{v}^{l} \\ z_{v}^{l} \\ \widehat{\delta}_{v}^{l'} \end{vmatrix}$	$\widehat{\delta}_{v}^{l}$

to mitigate this problem via neighborhood sampling [30], [32], [34], [35]. They sample vertexes and their neighbors to create a mini-batch that can fit into GPUs. However, it has been widely admitted that due to approximation errors, in some cases, minibatch training achieves lower accuracy compared to full-batch training [30], [36]–[39]. Moreover, a system supporting full-batch training can also conduct mini-batch training by adding an extra sampler. Therefore, in this paper, we focus on the most challenging problem—full-batch training.

#### III. CHALLENGES ANALYSIS

## A. Characterising GCN Training

Large Memory Footprint: For GCN training tasks, the widely adopted GAS (Gather-ApplyEdge-Scatter) programming model consumes GPU-memory that is proportional to the number of graph edges [31]. Because it needs to stack the source features into a  $|E| \times d$  intermediate feature matrix with indexSelect API of PyTorch. Therefore, training on the Reddit dataset [30] containing 114 million edges requires 58 GB of memory to hold all the intermediate matrices and incurs over 300 GB of DRAM access with PyG framework [52]. DGL framework [53] has an optimized memory management but it is still hard to train on a larger dataset such as Amazon [32] with a single GPU. For dedicated GCN accelerators [21], [23], [24], [54], they usually avoid duplicating vertexes like the GAS model by adopting a fine-grained vertex-centric dataflow. However, to buffer the features for back-propagation still incurs O(LNd) space. As listed in Table III, a two-layer GCN model needs to buffer up to five times more data than total hidden features. For Ogbn-Papers dataset containing 111 million vertexes [33], at least 568 GB of memory will be

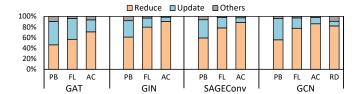


Fig. 3. Training time breakdown on V100 GPU.

consumed to train a two-layer model with a hidden size of 256. What is worse, the irregular graph operations incur O(L|E|d) memory accesses, making the system both memory-capacity and memory-bandwidth bounded.

Training Bottlenecks: Apart from the memory capacity issue on large graphs, we also analyze the bottlenecks of GCN training. We profile the execution time of operators using PyTorch-profiler [55] on an NVIDIA V100-32GB GPU with PyG [52] framework. Four GCN algorithms introduced in Section II and four middle-scale graph datasets namely PubMed (PB) [56], Flicker (FL) [35], Amazon-Computer (AC) [57] and Reddit (RD) [30] are adopted as benchmarks. According to Figure 2, we classify the operations involved in GCN training as three categories: (1) Irregular Reduce operations that mainly use *Index-Elementwise-Gather-Scatter* operators to compute neighbor features/gradients reduction along edges (marked with orange). (2) Regular Update operations for feature updates and gradients computation with Matmul operators. (marked with blue) (3) The remaining operations such as loss computation are classified as Others. As shown in Figure 3, in general Reduce and Update operations are the main bottlenecks during GCN training. The Reduce operations are more time-consuming on V100 GPU in most cases, and Update operations also take considerable time on PB and FL datasets, especially for GAT models. Note that on CPU platforms, Update operations will take up more training time due to CPUs' poor computation capacity.

The Heterogeneous Nature: We analyze the arithmetic intensity of Reduce and Update operations of GCN training theoretically. We notice that GCNs' weights are usually small in size. For example, a 4-layer GCN with input-size, outputsize, and hidden-size = 256 only has about 1MB weights in total. We can store the weights in on-chip SRAM and reuse them among vertexes. Therefore, the theoretical arithmetic intensity of Update operations for features/gradients update relying on *Matmul* operators is  $\frac{2 \times d_{in} \times d_{out}}{4B \times d_{in}} = 0.5 \times d_{out}$ Ops/Byte, where  $d_{in}, d_{out}$  represent input and output dimensions of a layer. On the contrary, for Reduce operations, massive amounts of features/gradients should be loaded from DRAM and can hardly be reused. Then the arithmetic intensity is  $\frac{2\times |\tilde{\mathcal{N}}(v)|\times d_{in}}{4B\times |\tilde{\mathcal{N}}(v)|\times d_{in}}=0.5$  Ops/Byte, if using *Weighted Sum* as the aggregator. Obviously, Reduce operations are much more memory-intensive than Update operations. We also conduct CPU-based profiling using Intel-Vtune [58] to prove this assertion. As shown in Table IV, we profile the average arithmetic intensity and MPKI of all cases. Reduce operations show a much lower arithmetic intensity and worse data locality than Update and Others, which is inefficient to accelerate with

TABLE IV				
CHARACTERIZATI	ON OF GCN TI	RAINING ON C	PU	
Operations	Reduce	Update	Others	
Ops per DRAM Byte	0.84	22.6	715	
L2 Cache MPKI	65.7	3.4	1.2	
L3 Cache MPKI	15.2	0.33	0.01	

traditional neural network accelerators [45], [47], [48], [50], [59] optimized for computation-intensive workloads.

#### B. Near-Memory-Processing to the Rescue?

To enable full-batch training on large graphs, some GPU-based distributed training systems are proposed [37]–[39]. They benefit from GPUs' high memory bandwidth and computation capacity, but the memory capacity is still hard to scale up. For instance, a server with eight V100 GPUs only provides 256 GB total memory and can not deal with super-large graphs like Ogbn-Papers [33]. DistGNN [36] leverages the easy-to-scale DIMM-based memory system and trains on CPUs. According to their setup, a single-socket machine equipping 1.5TB memory can train a 3-layer GCN on Ogbn-Papers. However, such a CPU-based method suffers from limited memory bandwidth and inadequate computation capacity.

Recently, DIMM-based near-memory-processing paradigm (NMP) has been proposed to provide memory-capacity proportional bandwidth and computation capacity. Chameleon [60] is a pioneering work that proposes to integrate CGRA cores to buffer-chips of commodity DDR4 LRDIMMs [61] to enable general-purpose near-memory computation. RecNMP [62] and TensorDIMM [63] also propose to accelerate the inference of Deep Learning Recommendation Model (DLRM) adopting such a paradigm. Similar to GCN training, DLRM inference tasks also face memory capacity and bandwidth challenges, which motivates us to leverage the DIMM-based NMP technique to accelerate full-batch GCN training.

However, to design a practical NMP architecture for efficient GCN training is not trivial. Firstly, unlike DLRM which is only bounded by the memory-intensive embedding table operations [64], GCN training also has computation-bounded Update operations due to the heterogeneous nature. For instance, a two-layer GIN model trained on Ogbn-Papers dataset with a hidden size of 256 incurs more than 100 TFLOPs computation for just one iteration. It takes a server CPU several minutes to finish. Secondly, unlike DLRM tasks that respond to batched quires, GCN training must consider the graph structure. Due to the sparse connectivity and irregularity of real-world graphs and the complex training dataflow, it is difficult to optimize a GCN training system's efficiency.

To overcome these challenges, we propose GCNear, a novel GCN training accelerator with a hybrid architecture. It combines both DIMM-based near-memory processing engines and a centralized ASIC engine to match the heterogeneous nature of GCN training and provide easy-to-scale memory capacity (Section IV). Several optimization strategies are also proposed to further boost the training efficiency (Section V).

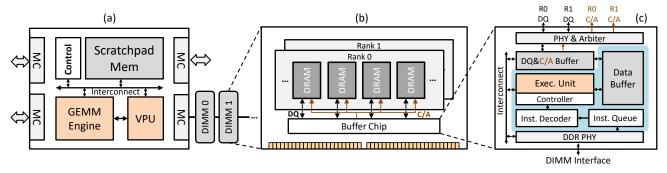


Fig. 4. GCNear architecture overview. (a): Centralized ASIC Engine (CAE). (b): NMP-enabled DIMM. (c): Near-Memory Engine (NME).

#### IV. GCNEAR ARCHITECTURE

#### A. Overview

**Design:** As illustrated in Figure 4, GCNear accelerator consists of a Centralized ASIC Engine (CAE) and multiple NMP-enabled DIMMs. The CAE equips a powerful GEMM engine and a vector-processing unit (VPU) to deal with computation-intensive Update operations. NMP-enabled DIMMs are connected to CAE's four memory channels, each containing a Near-Memory Engine (NME) for memory-intensive Reduce operations. Such a DIMM-based CAE/NMEs hybrid architecture matches the heterogeneous nature of GCN training. More importantly, we can easily scale up the memory capacity and processing ability by connecting more DIMMs to the memory channels. Multiple GCNear accelerators can be further connected to shape a Multi-GCNear system to tackle super-large graphs and deep models (discussed in Section VII-A).

Workflow: Figure 5 depicts the base workflow of GCNear. The adjacent matrix (compressed in CSR format) and feature vectors of graph G for training are initially stored in DRAM. We split the vertexes in G and assign them to different DIMMs. In the figure, we use two DIMMs (DIMM-0 and DIMM-1) for illustration, which hold the data of blue and grey vertexes, respectively. According to the GCN training flow introduced in Section II, we traverse every destination vertex in each forward and backward step and conduct Reduce or Update operations. If the operation to run belongs to Reduce type (operations marked with orange in Figure 2), CAE generates customized GCNear instructions and sends them through the memory channel interfaces to control each NME. NMEs decode the instructions and perform partial reduction locally. Then, they send partial results back to CAE. CAE is responsible for merging these partial results received from different NMEs to get the final reduction results. If the operation to run belongs to Update type (operations marked with blue in Figure 2), CAE computes with the merged results buffered on-chip or directly reads the required data from DRAM without near-memory reduction. The updated features or gradients will be written back to DRAM. After a training epoch finishes, CAE updates the weights with the calculated gradients. Note that we process Reduce and Update operations with respect to the adjacent destination vertexes in a pipelined manner since they have no data dependency in the same training epoch. Such a training process is executed

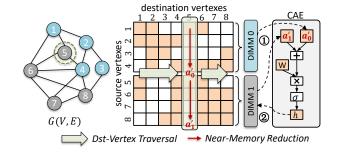


Fig. 5. Base workflow. ①: For Reduce operations, NMEs perform nearmemory reduction, then send partial results to CAE. ②: CAE merges partial results, performs Update operations, then writes vertex data to DRAM.

for many epochs, after which the trained model weights will be read out from CAE's on-chip buffer.

We can find that for Reduce operations, our near-memory reduction workflow decreases the DRAM read via memory channels from  $|\tilde{\mathcal{N}}(v)| \times d$  to no more than  $\#DIMMs \times d$  for destination vertex v. The latter is usually much smaller than the former. Considering that NMEs in different DIMMs work in parallel, GCNear can utilize the high aggregated local bandwidth. Moreover, for computation-intensive Update operations, CAE provides sufficient computation capacity. Such a workflow relies on specialized CAE and NME architectures, which will be introduced in the following sections.

# B. CAE Architecture

Centralized ASIC Engine (CAE) is mainly responsible for the computation-intensive Update operations. It also merges partial reduction results produced by NMEs. As shown in Figure 4-(a), the CAE engine has both a GEMM engine (implemented with systolic array architecture) and a vector-processing unit (VPU). A scratchpad memory is equipped to buffer the temporary data and model weights. Four customized memory controllers support sending GCNear instructions to NMP-enabled DIMMs. A controller (can be implemented with a RISC-V core) schedules the whole training process according to the input graph's adjacent matrix and the model's configuration. A high-bandwidth on-chip network connects all the components. We also have an optional router (omitted in the figure) for inter-chip communication, which will be used to build the Multi-GCNear system (Section VII-A).

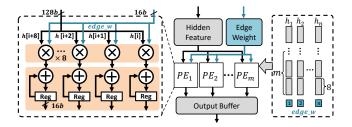


Fig. 6. Execution Unit (EU) architecture in each NME.

#### C. NME Architecture

Similar to previous works [60], [62], [63], [65], the Near-Memory Engine (NME) resides in the buffer chip of DDR4 LRDIMM [61]. Each NMP-enabled DIMM equips one NME. In Figure 4-(c), we mark the customized components with blue. There are five main components: Instruction Queue, Instruction Decoder, Execution Unit, Data Buffer, and a Controller. NME works as follows: it receives NMP instructions from CAE, which arrive in the Instruction Queue. Instruction Decoder decodes these instructions. Then, the light-weighted controller starts local execution following the decoded instruction. Execution Unit handles data reduction calculation. The controller is also responsible for generating regular DDR4 Command/Address and data signals (DDR.C/A and DDR.DQ) and sending them to all DRAM devices across parallel ranks in a DIMM (two ranks in the example). Since NMEs can access their local DRAM devices in parallel, the aggregated local bandwidth can be much higher than traditional centralized computing architectures. For example, a configuration of four DIMMs in a channel with two ranks per DIMM could achieve 8× higher equivalent bandwidth. Furthermore, we equip an SRAM data buffer in NME to explore data locality in graph structure (Section IV-D). If data is already in the buffer, we can avoid querying DRAM devices to speed up the execution and save energy. Apart from near-memory processing, if NME receives standard DDR commands from the CAE-side memory controller, it will bypass execution units and directly conducts Read/Write/Precharge commands, etc.

**Execution Unit:** The Exec.Unit (Figure 6) in each NME is responsible for near-memory reduction calculation of Reduce operations. According to Figure 2, data reduction can be formulated as the weighted sum of n feature/gradient vectors:  $\sum_{u=1}^{n} h_u * edge\_w_u$ , where  $edge\_w$  denotes edge weight (Scalar). For GCN, the edge weight is  $\frac{1}{\sqrt{D_u D_v}}$ . For GAT, it is an estimated importance factor. The execution unit adopts an intra-feature parallelism data flow. There are in total m PEs, each computing eight elements every cycle. The results are added to partial sums stored in registers. Since each element in a vector  $h_u$  shares the same edge weight,  $edge_w$  is broadcast to each multiplier. Therefore, m PEs compute  $8 \times m$  elements of a vector in parallel. If a vector cannot consume all PEs, the free PEs can be assigned to another vector. Also, if the vector  $h_u$  is longer than  $8 \times m$ , it needs multiple rounds to finish the computation. EU also supports Sum and Mean operators used in GIN and SAGEConv by setting  $edge_w$  to 1 and 1/n.

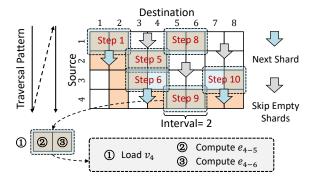


Fig. 7. Narrow shard based data reuse.

#### D. Data Reuse with Narrow-Shard Strategy

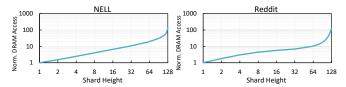


Fig. 8. Shard Shape Exploration.

To further reduce DRAM access, we explore data reuse through sharding strategies [21], [43], [66], [67]. In Figure 7, DIMM-0 computes partial reduction of destination vertexes  $v_1$ - $v_8$ . We partition the edges into multiple  $R \times C$  shards and process one shard each step. For each shard, we first load R source vertexes from DRAM (e.g., operation ①), then the computation of edges within the same shard (operations ②,③) can reuse the loaded source vertexes. The partial results of C destination vertexes are reused by the following shards of the same inverval. Therefore, we have to buffer R source vertexes and R partial sum on chip, at least R0 partial sum on chip, at least R1 partial results of R2 partial sum on chip, at least R3 pace should be allocated. Considering the limited buffer size in NMEs, how to determine R3 and R4 becomes an important problem.

We assume that at most 129 feature vectors can be buffered on chip, and explore different shard configurations. As shown in Figure 8, setting R=1 and C=128 brings the lowest DRAM access on both NELL and Reddit datasets. It is easy to explain such a result: The R dimension affects inter-shard source vertex reuse. For example, in Figure 7. if R=4 then source vertexes  $v_1$ - $v_4$  are always on-chip from step 1 to step 11. However, for real graphs with millions of vertexes, Even setting a large R (e.g., R=128) can hardly bring any meaningful inter-shard reuse. The loaded source vertexes are evicted quickly due to poor data locality. Therefore, it is natural to let R=1 and enlarge C for better inner-shard source vertex reuse. We call it Narrow-Shard strategy.

Moreover, our Narrow-Shard strategy supports skipping empty shards to save useless data read. (e.g., step 8 to step 9 in the figure skips two empty shards). Adopting narrow shards also enables us to conduct fine-grained inter-shard scheduling during execution, which is introduced in Section V-B.

# E. GCNear-ISA

We design a specialized GCNear-ISA to drive the shardbased near-memory reduction workflow. As demonstrated in

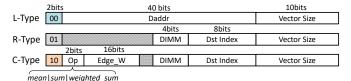


Fig. 9. GCNear ISA.

Figure 9, GCNear-ISA consists of three types of instructions:

**L-Type:** L-Type instruction is used to load vertex data from DRAM devices to NME's data buffer. According to our Narrow-Shard strategy, one source vertex will be loaded each time. Therefore, L-type instruction has Daddr and Vector Size fields to indicate the size and start address of a feature/gradient vector. NME's controller will generate standard DDR read commands according to the received L-type instruction and send them to DRAM devices to load data. For standard DDR4 with a burst length of 8 (BL-8), loading a vector longer than 64B demands multiple burst-read commands.

**C-Type:** C-Type instruction controls the calculation of nearmemory reduction. The Op field defines which type of operation will be executed. The Edge\_W field (we use 16bits for BF16 format) carries the edge weight, e.g.,  $\frac{1}{\sqrt{D_v D_u}}$  that will be multiplied to source vertex's data vector. After multiplication, we index the buffered partial results by Dst Index bits (denotes the destination's <u>relative index</u> within an interval) and add it to the multiplication results. Taking operation ② in Figure 7 as an example, we multiply edge  $e_{4-5}$ 's weight and source vertex  $v_4$ 's data vector and then index destination  $v_5$ 's partial results with Dst Index = 0 ( $v_5$  is the first vertex within the interval). C-Type instructions rely on CAE's controller to analyze the adjacent matrix and determine which edge should be processed. For GCN and GAT, CAE is also responsible for calculating the edge weights. Such a design keeps the NME-side controller as light-weighted as possible.

**R-Type:** R-Type instruction is used to read out partial results from the NME-side data buffer upon all shards within the same interval finish computing. The Dst Index and Vector Size bits jointly determine which bytes to read. To read out multiple destination vertexes within an interval, the controller will issue a sequence of R-Type instructions.

R-Type and C-Type instructions also have DIMM fields to indicate which DIMM in a channel should receive the instruction. L-Type does not have this field explicitly because Daddr already includes the DIMM index according to our data mapping (Section IV-F). Since R-Type and C-Type operations do not involve DRAM data access, the latency is determined. We denote the latency as  $tNME\_RD$  and  $tNME\_CD$ , respectively. The L-Type instruction will be decoded into standard DDR commands to read data from DRAM devices. Our data mapping guarantees that the feature bytes of a vertex will be mapped into the same DRAM row, the latency is  $tCL + \lceil \frac{Vector\ Size}{Burst\ Size} \rceil \times tBL$  (row buffer hit) or  $tRC + tRCD + tCL + \lceil \frac{Vector\ Size}{Burst\ Size} \rceil \times tBL$  (row buffer miss). CAE-side memory controllers rely on these extra timing constraints to schedule instructions.

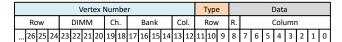


Fig. 10. Data mapping for vertex data. 'R.' is short for Rank.

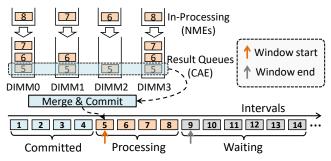


Fig. 11. Asynchronous Interval Scheduling.

# F. Data Mapping

Figure 10 demonstrates the data mapping of GCNear. The intermediate data for GCN training can be indexed using [VertexNumber|Type|Data]. Data indexes the bytes within a feature/gradient vector. Type indicates the data's type, including feature  $h_v^l$ , gradients  $\hat{\delta}_v^l$  or pre-activation feature  $z_v^l$ , etc. We split a data vector to the parallel ranks of each DIMM for higher local bandwidth. We make sure that each subvector is stored sequentially in a DRAM row. We also store consecutive vertexes in the same row. Thus, the adjacent shards will have a higher chance to read source vertex from the same activated row (open-page policy). We store close vertexes in different banks for better bank-level parallelism. Note that the mapping can be adjusted according to different tasks and system configurations. For example, we can assign more column bits to Data field to hold longer feature vectors or extend DIMM bits if more DIMMs are connected.

#### V. OPTIMIZATIONS

#### A. Asynchronous Interval Scheduling

Our base workflow requires synchronizing the partial reduction results among DIMMs. Thus, the latency is determined by the slowest DIMM for each interval. Unfortunately, we observe that the number of valid shards in the same interval can vary greatly among DIMMs due to the irregularity in graph structures, resulting in workload imbalance problems. For instance, we profile on Amazon [32] and NELL [3] datasets and estimate the the max idle time (longest\_idle\_cycles / longest\_finish\_cycles  $\times 100\%$ ) of DIMMs. With interval = 64, Amazon suffers about 20% max idle time on average, while NELL even has more than 80% max idle time, resulting in a severe resource underutilization problem.

We propose an Asynchronous Interval Scheduling strategy to mitigate this problem. As illustrated in Figure 11, we set several result queues in CAE, each receiving partial reduction results from a single DIMM. We then allow the CAE-side controller to issue near-memory reduction instructions for interval i+1 immediately after a DIMM returns the partial results of interval i, if interval i+1 is within the *Processing* window. Once every DIMM returns results of interval i, CAE

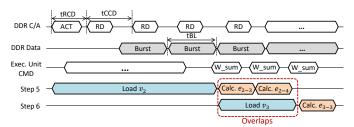


Fig. 12. Timing diagram of Inter-Shard Scheduling

merges these partial results, commits interval i and right-shifts Processing window. The window size is determined by the depth of result queues in CAE. By this means, we can schedule multiple intervals asynchronously and mitigate the workload imbalance problem caused by local irregularity in graphs.

# B. Inter-Shard Scheduling

In Figure 7, computing each shard needs a load and multiple edge calculation operations. If vertex loading and edge computation are executed sequentially, either the memory devices or the execution unit will be idle at a certain time. To improve resource utilization, we can schedule L-Type and C-Type instructions of the adjacent shards and overlap their memory access with computation. We use Step-5 and Step-6 in Figure 7 as an example to demonstrate the intershard scheduling strategy. As shown in the timing diagram in Figure 12, supposing the feature size is 128B, after two rounds of burst read,  $v_2$ 's feature vector has been loaded to NME's data buffer. Then the calculation of  $e_{2-3}$ ,  $e_{2-4}$  can be launched immediately. In the meantime, the CAE-side controller issues the load instruction for Step-6, which is executed by NME concurrently. In this way, Step-6's data loading overlaps with Step-5's edge calculation. This strategy mitigates the total delay of near-memory reduction and increases the utilization of both the execution unit and DRAM bandwidth.

# C. Interchange the Execution Order

We notice that for some tasks the input feature vectors are longer than those of the hidden features. For example, Reddit's input feature length is 602, and NELL's input feature length even reaches 61278, while the hidden size is usually 128 or 256. To reduce DRAM access and save NME's data buffer, we can interchange the execution order of the first layer if linear aggregators are adopted. For instance, we can calculate the combination of GCN first:  $a_u^1 = h_u^1 \cdot W^1$ , then aggregation:  $h_v^2 = \sigma(\sum_{u \in \tilde{\mathcal{N}}(v)} \frac{1}{\sqrt{D_u D_v}} \cdot a_u^1)$  without affecting the output values. The original execution order incurs roughly  $2 \times |E| \times d_1 + N \times d_2$  DRAM access for the first layer, where  $d_1$  and  $d_2$  denote the input and output feature dimensions. After interchanging the execution order, the memory access becomes  $2 \times |E| \times d_2 + N \times d_1$ . Since N << |E|, the data access reduces about  $\frac{d_1}{d_2} \times$ . With hidden size = 256, we can estimate that the theoretical DRAM access reduces roughly  $7.8 \times$  and  $2.3 \times$  for NELL and Reddit, respectively. Similar techniques are also adopted by AWB-GCN [22] to reduce overall computation.

## VI. EVALUATION

## A. Methodology

System Configuration: Table V summarizes the system

TABLE V				
System Parameters and Configurations				
Me	emory System Configuration			
4 channel	2400, 32GB (4Gb, x72) LRDIMM s × 4 DIMMs × 2 ranks, FR-FCFS try RD/WR queue, Open policy			
Г	PRAM Timing Parameters			
tRC=56, tRCD=17, tCL=17, tRP=17, tBL=4 tCCD_S=4, tCCD_L=6,tRRD_S=4, tRRD_L=6, tFAW=26				
NMP Parameters				
Data Buffer	128KB, Dual Ports, Word size = 16B Area = 0.21 mm <sup>2</sup> , Power = 40.2 mW			
Execution Unit	16 PEs, 8 MACs per PE @500MHz Area = 0.42 mm <sup>2</sup> , Power = 178.1 mW			
CAE Parameters				
GEMM Engine   128×128 Systolic Array @700MHz Area = 27.3 mm², Power = 6291.4 mW				
VPU	VPU SIMD-16 Cores $\times 32$ @700MHz Area = 0.82 mm <sup>2</sup> , Power = 296.6 mW			
Scratchpad Memory   16MB, 8 Banks, Dual Ports, Word size = 64B Area= 33.7 mm², Power = 5519.2 mW				

TABLEX

parameters of GCNear prototype. For the memory system, we connect four DDR4-2400 LRDIMMs to each channel. According to Micron's LRDIMM datasheet [61], each DIMM has 32GB capacity. In total GCNear equips 512GB memory, which is much larger than V100 GPU's. For NME, we set 16 PEs. Each PE contains eight MACs. Running at 500MHz, an NME provides a peak performance of 128GFLOPS. For CAE, we adopt a  $128 \times 128$  systolic array as the GEMM engine, providing about 22TFLOPS computation capacity running at 0.7GHz. The VPU is composed of 32 SIMD-16 cores and has 700GFLOPS peak performance. The scratchpad memory is 16MB, which can be flexibly divided into weight buffer, input/output buffer, edge buffer, result queues, etc. We adopt BF16 as the data format. BF16 has the same accuracy as FP32 for NN training [68] but is more cost-efficient. We estimate CAE and NME's area and power using 16nm and 28nm technologies, respectively. The GEMM and VPU's area and power are measured according to TPU-v2 [59], [69] and HyGCN [21]. To estimate the overhead of NME's logic parts, we implement Exec. Unit with Chisel and synthesize the generated RTL using Synopsys Design Compiler 2016 under TSMC 28nm. We get the area and power of all SRAM buffers with CACTI [70]. As we can see, the main components of NME incur moderate area (0.63 mm<sup>2</sup>) and power (218.3mW) overhead, given that a single DIMM usually consumes several watts and the buffer chip takes up about 100 mm<sup>2</sup> [71].

Simulation Methodology: To evaluate the performance of GCNear, we first implement a customized GCN training framework with C++ to support our narrow shard based training dataflow given a graph's adjacent matrix and the model's configuration. It generates Reduce, Update, and other operators on-the-fly and sends them to a cycle-level GCNear simulator. Specifically, we extend DRAMsim3 simulator [72] to support GCNear-ISA, taking NME's timing constraints and power consumption into consideration. To evaluate CAE's performance, we obtain GEMM's execution cycles using SCALE-Sim [73]. The VPU cycles are calculated

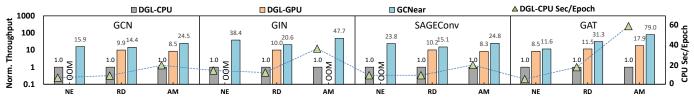


Fig. 13. Performance comparisons. OOM is short for "Out of Memory".

TABLE VI							
	GRAPH DATASETS						
Graph   #Vertexes   #Edges   #Labels   #Features							
NELL (NE)	65,755	266,144	210	61,278			
Reddit (RD)	232,965	114,615,892	41	602			
Amazon (AM)	2,449,029	123,718,280	47	100			
Ogbn-Papers (OP)	111,059,956	1,615,685,872	172	128			

according to VPU's parallelism and the size of features. We model on-chip buffers' access latency using CACTI [70] and inject these parameters into our simulator.

**Benchmarks:** Table VI lists the benchmarking graph datasets used for evaluation, including NELL (NE) [3], Reddit (RD) [30], Amazon (AM) [32] (Amazon is also called Ogbn-Products in some papers), and Ogbn-Papers (OP) [33]. We adopt four GCN models mentioned above, namely the classic GCN [3], GIN [51], SAGEConv [30], and GAT [11], as benchmarking models. In the default configuration, each model has two layers with the hidden size of 256. Given that NE's superlong input feature makes it impossible to keep the first layer's weights on-chip, we load it from DRAM each time.

Baselines: Since there is no other full-batch training accelerator at present, we mainly compare GCNear with CPU/GPU platforms using the DGL framework [53]. We adopt a DGX-1 workstation equipping Xeon E5-2698-v4 CPU (4 Channels, 256GB DDR4-2400) and V100 32GB GPUs to evaluate the training performance of DGL-CPU (MKL-2020.2) and DGL-GPU (CUDA-10.2/cudnn 7.6). We test on a single GPU because DGL does not support full-batch training on multi-GPUs. Due to the capacity limitation, neither the DGL-GPU nor DGL-CPU can train on the super-large OP dataset. Thus in Section VII-A, we adopt two distributed full-batch training systems: DistGNN [36] and Roc [37] as the baselines. Considering that GCNear adopts BF16 data format (two Bytes per element) while the baselines all use FP32 (four Bytes per element), we double the vector size when simulating GCNear's data transmission for fair comparisons.

## B. Main Results

Training Throughput: We first estimate the training throughput of GCNear and the CPU/GPU baselines on 12 benchmarking tasks. The performance is measured with end-to-end training seconds per epoch and then normalized to the CPU baseline. As depicted in Figure 13, DGL-GPU suffers OOM problems on four tasks due to limited memory capacity. Though DGL-CPU successfully tackles these tasks with 256GB memory, it shows quite a low training speed due to its limited memory bandwidth and computation capacity. GCNear demonstrates superior training speed compared to these two baselines. Specifically, GCNear achieves 24.8× and

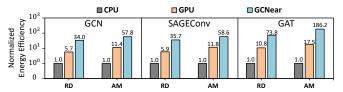


Fig. 14. Energy-efficiency comparisons.

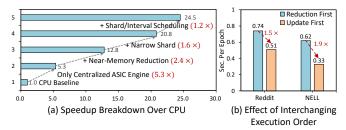
2.2× geomean speedup compared to DGL-CPU and DGL-GPU (we omit OOM cases). On GAT and GIN tasks, GCNear achieves higher speedup than the GCN and SAGEConv, because GAT and GIN involve much more computation.

Energy-efficiency: We measure GCNear's per-epoch energy consumption and then compare it with CPU and GPU baselines (we omit OOM cases). The CPU system's energy consumption is estimated with PyRAPL [74]. We test the GPU's running power using PyNVML [75]. We then calculate the GPU energy with the product of average power and per-epoch time. Values are normalized to the CPU baseline. As shown in Figure 14, GCNear has 61.9× and 6.4× higher energy-efficiency (geomean) compared to CPU/GPU platforms. High training throughput and low power consumption brought by the ASIC engine and saved data transmission with near-memory reduction jointly lead to GCNear's high energy efficiency for GCN training.

## C. Performance Analysis

**DRAM Access Saving:** By offloading Reduce operations to NMEs, the DRAM access via memory channels is substantially reduced. For the three evaluated graphs, RD and AM benefit from 95.7% and 78.3% memory access saving on average. NE shows the lowest 18.1% reduction ratio because of its very low average degree (Avg. Degree = 8). The speedup on NE mainly comes from execution order interchange and faster Update operations accelerated by CAE. The saved DRAM access dramatically reduces the system's energy consumption. Assuming the off-chip IO cost is 22pJ/b [62], 58.5% and 47.8% of DRAM energy is saved on RD and AM tasks.

**Speedup Breakdown:** To better understand the contributions of different design points to GCNear's high performance, we evaluate on the AM-GCN task and demonstrate the speedup breakdown in Figure 15-(a) with DGL-CPU as baseline. As we can see, directly adopting CAE for GCN training without near-memory reduction gets  $5.3\times$  speedup, thanks to CAE's much higher computation capacity than CPU. Performing near-memory reduction in a naive way brings  $2.4\times$  speedup because of the utilizing of high aggregated in-DIMM bandwidth. Adopting the Narrow-Shard strategy contributes to  $1.6\times$  speedup by exploring data reuse. At last, interval scheduling and shard scheduling bring  $1.2\times$  speedup



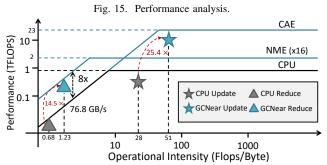


Fig. 16. Roofline analysis on AM dataset.

by eliminating idle time and improving resource utilization (Interval scheduling contributes about  $1.1\times$ ). Considering that AM dataset does not need to interchange the execution order to save memory access, we evaluate the Execution Order Interchange strategy on RD and NE. As shown in Figure 15-(b). Interchanging order of the first layer successfully brings  $1.5\times$  and  $1.9\times$  speedup on RD-GCN and NE-GCN tasks, thanks to the reduced memory access in the first layer. In conclusion, our designs and optimizations all demonstrate significant effectiveness in accelerating GCN training.

**Roofline Analysis:** We also adopt the roofline model to analyze the performance of GCNear and DGL-CPU baseline. To fully demonstrate the superiority of GCNear, we evaluate on GIN, which has the lowest Reduce arithmetic intensity and highest Update arithmetic intensity among the benchmark models. As shown in Figure 16, both Xeon E5-2698-v4 and GCNear have four memory channels, providing 76.8GB/s memory bandwidth. CPU-Reduce operations suffer from low arithmetic intensity and are bounded by the limited memory bandwidth. In comparison, GCNear's near-memory reduction mechanism provides up to 8× higher aggregated local bandwidth. Moreover, adopting data buffer in NMEs and reusing data with the Narrow-Shard strategy increases the arithmetic intensity of Reduce operations. Therefore, GCNear-Reduce achieves  $14.5 \times$  higher performance compared to CPU-Reduce. Besides, GCNear-Update also shows 25.4× speedup against CPU-Update due to the more powerful CAE and improved arithmetic intensity by buffering all the weights on-chip.

# D. Design Space Exploration

**Shard Interval Size & Window Size:** According to our Narrow-Shard and Asynchronous Interval Scheduling strategies, larger shard intervals and processing windows tend to bring higher data-reuse ratios and better workload balance. To understand the impact of these two parameters on GCNear's performance, we first keep window = 4 and set interval

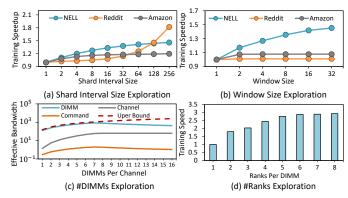


Fig. 17. Design space exploration. (c) and (d) are based on AM datasaet.

from 1 to 256 and evaluate the training speedup on the AM-GCN task. As shown in Figure 17-(a), the RD dataset is more sensitive to shard interval size, while the speedup on NE and AM reaches a plateau when the interval size is larger than 128. Considering that a too large interval will increase the area and power overhead of NMEs, we set interval = 128 in our prototype. We then keep interval = 128 and set window from 1 to 32. In Figure 17-(b), NE benefits a lot from large window size, but RD and AM are less sensitive to window size because of their less severe workload imbalance problems. Since the space complexity of result queues is  $\#DIMMs \times interval \times window \times d$ , it is better to set the window size to a relatively small value (e.g., set window = 4 in our prototype) for saving CAE's area and energy.

DIMMs Per Channel: More DIMMs bring larger capacity and higher aggregated local bandwidth. However, DIMMs connected to the same channel time divide the channel's command/data bandwidth to receive instructions and send back partial reduction results. Thus the channel bandwidth can also become the bottleneck. We explore the number of DIMMs per channel. Figure 17-(c) shows that the effective aggregated in-DIMM bandwidth reaches a maximum and then decreases. Adding too many DIMMs increases the number of partial results transmitted via the channel bus and finally saturates the channel bandwidth. We solve this scalability issue by proposing a Multi-GCNear system in Section VII-A. We also observe that the command bandwidth will not become the bottleneck thanks to our coarse-grained instructions.

Ranks Per DIMM: An NME can access ranks in parallel to achieve #Rank× higher local bandwidth. To study the benefits of rank-level parallelism, in Figure 17-(d), we explore the number of ranks per DIMM from 1 to 8. The speedup will also be saturated when near-memory reduction is bounded by the channel bandwidth or NME's computation capacity. Adding multiple ranks in a DIMM and driving them in parallel will increase the complexity of NME's interface and control logic. Therefore we consider two ranks per DIMM in our prototype.

#### VII. DISCUSSION

## A. Multi-GCNear System

To deal with super-large graphs (e.g., OP in Table VI) or deep models (more than two layers), we connect multiple

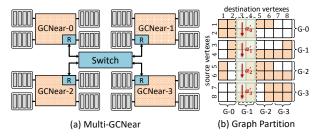


Fig. 18. Multi-GCNear system and the graph partition.

#### TABLE VII

DADAMETERS	OE	DISTRIBUTED	CVCTEMO
PARAMETERS	OF	DISTRIBUTED	SYSTEMS

Configuration	Total Memory   Computation Capacity
Roc [37]   8 NVIDIA-V100, 2 no	odes   256GB   126 TFLOPS
DistGNN [36]   32 Intel Xeon 9242 C	CPU   > 2TB   226 TFLOPS
Multi-GCNear   4 GCNear accelerat	or   2TB   100 TFLOPS

GCNear accelerators with a switch to build a Multi-GCNear system (Figure 18-(a)). We also propose a two-level reduction dataflow for Multi-GCNear. As illustrated in Figure 18-(b), we first partition the input graph and assign the sub-graphs to different accelerators. In each accelerator, source vertexes in the sub-graph are assigned to the connected DIMMs following the method in Figure 5. We then assign Reduce and Update operations concerning different destination vertexes to each accelerator. As shown in the figure, GCNear-1 (G-1) is responsible for computing destination vertexes  $v_3$  and  $v_4$ . However, parts of the source vertexes for Reduce operations are distributed in other accelerators. Therefore, Reduce operations will have two conditions: (1) The source vertexes are in G-1's DIMMs. G-1 performs near-memory reduction and merging as usual. (2) The source vertexes are in other accelerators' DIMMs. For example, source vertexes  $v_1, v_2$  are assigned to G-0. Apart from near-memory reduction in G-0's DIMMs, G-0's CAE merges the partial results and then sends them to G-1 for further merging. Thus, the burden of interchip communication is mitigated. We call this workflow Two-Level Reduction. All the weight gradients will be gathered to G-0 to update the model weights. Then the updated weights are broadcast to other accelerators. Considering the weights' small size, the synchronization overhead is negligible.

Comparisons with Roc and DistGNN: We evaluate the performance of Multi-GCNear by extending our simulator and compare it with two state-of-the-art full-batch training systems, namely Roc [37] and DistGNN [36]. Systems' parameters are listed in Table VII. We assume the switch of Multi-GCNear provides the same bandwidth as Roc's NVLink. We adopt the same model and graph settings from their papers and use their reported performance numbers for comparison. As shown in Figure 19, our Multi-GCNear system achieves about  $3.1 \times$  speedup on the largest OP dataset (3-layer GCN, hidden size = 256) and is also  $1.6 \times$  faster on AM than DistGNN with 32 CPU sockets. On deep model tasks (four-layer GCN), Multi-GCNear also achieves about 2.1× speedup on AM dataset and 1.08× speedup on the RD dataset, compared to the Roc system built with eight V100 GPUs. We can further extend the Multi-GCNear system by connecting more accelerators. We leave the evaluation to future work.

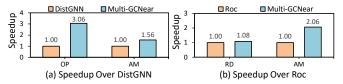


Fig. 19. Comparisons with DistGNN and Roc.

#### B. Uneven Vertex Partition

In this paper, we partition vertexes evenly for both the single GCNear accelerator and the Multi-GCNear system. An uneven vertex partition strategy considering graph structure information (e.g., graph community [76], [77]) can potentially improve data locality and further reduce data transmission [25], [32], [78]. However, uneven graph partition usually requires complicated pre-processing, which can be very time-consuming on large graphs [79]. Therefore, we leave the study of efficient uneven vertex partition to our future work.

## VIII. RELATED WORK

## A. GCN Acceleration

Recently, plenty of GCN/GNN accelerators have been presented [21]–[29], [80] for efficient GCN inference. As far as we know, GraphACT [54] is the only GCN training accelerator. However, it only supports mini-batch training. In each training epoch, a mini-batch subgraph is sampled from the full graph which can fit in the FPGA's on-chip memory. Our GCNear accelerator targets the more accurate but challenging full-batch training tasks. We argue that GCNear can also support mini-batch training through adopting a sampling-based workflow. There are also several mini-batch/full-batch training frameworks [31], [36]–[39], [81], [82]. They are all based on general-purpose CPU/GPU platforms.

## B. DRAM-based Near-Memory Processing

Many prior works propose 3D/2.5D-stacked memory based NMP accelerators for graph processing [40]–[44], DNN acceleration [83]–[91], or general-purpose applications [92]–[96]. A recent work also adopts 3D-stacked memory to accelerate GCN inference [97]. Due to their limited memory capacity (≤128GB) and high cost, they are not suitable for supporting full-batch GCN training. Chameleon [60] proposes to implement NMP by adding CGRA cores to the data buffer on LRDIMM [61] to break the capacity limitation. Several works adopt this paradigm and build efficient recommendation systems [62], [63], [98], [99]. Our work is the first to leverage DIMM-based NMP to accelerate full-batch GCN training.

#### IX. CONCLUSION

In this paper, we propose GCNear, a hybrid architecture leveraging both near-memory processing and centralized processing to accelerate full-batch training on large graphs. Comprehensive evaluations on twelve tasks demonstrate that GCNear achieves much higher training speed and energy efficiency compared to CPU/GPU platforms. We also propose a Multi-GCNear system to deal with super-large graphs and deep models. Compared to two state-of-the-art distributed training solutions, Multi-GCNear also achieves better performance.

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