

EEE 468 –VLSI Circuit and Design Laboratory
Level-4 Term-2
Final Project Presentation

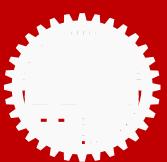
16-bit Carry-Lookahead Adder

SUBMITTED BY – G2-
1906081, 1906174, 1906192, 1906193
GROUP 03
07 DECEMBER 2024

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BANGLADESH UNIVERSITY OF ENGINEERING AND TECHNOLOGY
DEPARTMENT OF ELECTRICAL AND ELECTRONIC ENGINEERING

Outline

Summary

Introduction

Design RTL

Directed Testbench

Layered Testbench

Synthesis

PnR with DRC

Optimization

Acknowledgement and References



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16-bit Carry-Lookahead Adder

Designed an optimized 16 Bit Carry Lookahead Adder

RTL Design

**Directed
Testbench**

**Layered
Testbench**

Synthesis

**PnR with
DRC**

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Introduction

United States Patent Office

2,966,305

Patented Dec. 27, 1960

2,966,305

SIMULTANEOUS CARRY ADDER

Gerald B. Rosenberger, Wappingers Falls, N.Y., assignor
to International Business Machines Corporation, New
York, N.Y., a corporation of New York

Filed Aug. 16, 1957, Ser. No. 678,573

8 Claims. (Cl. 235—175)

For simplification let $x_n y_n = D_n$ and $x_n + y_n = P_n$. Then

$$C_1 = D_1 + P_1 C_{in}$$

$$C_2 = D_2 + D_1 P_2 + P_1 P_2 C_{in}$$

$$C_3 = D_3 + D_2 P_3 + D_1 P_2 P_3 + P_1 P_2 P_3 C_{in}$$

$$C_4 = D_4 + D_3 P_4 + D_2 P_3 P_4 + D_1 P_2 P_3 P_4 + P_1 P_2 P_3 P_4 C_{in}$$

and

$$C_{45} = D_{45} + D_{44} P_{45} + D_{43} P_{44} P_{45} + \dots + \dots P_1 P_2 P_3 P_4 \dots$$

$$P_{41} P_{42} P_{43} P_{44} P_{45} C_{in}$$

[1] G. B. Rosenberger, "Simultaneous Carry Adder," Dec. 27, 1960 Accessed: Dec. 06, 2024. [Online]. Available: <https://patents.google.com/patent/US2966305>



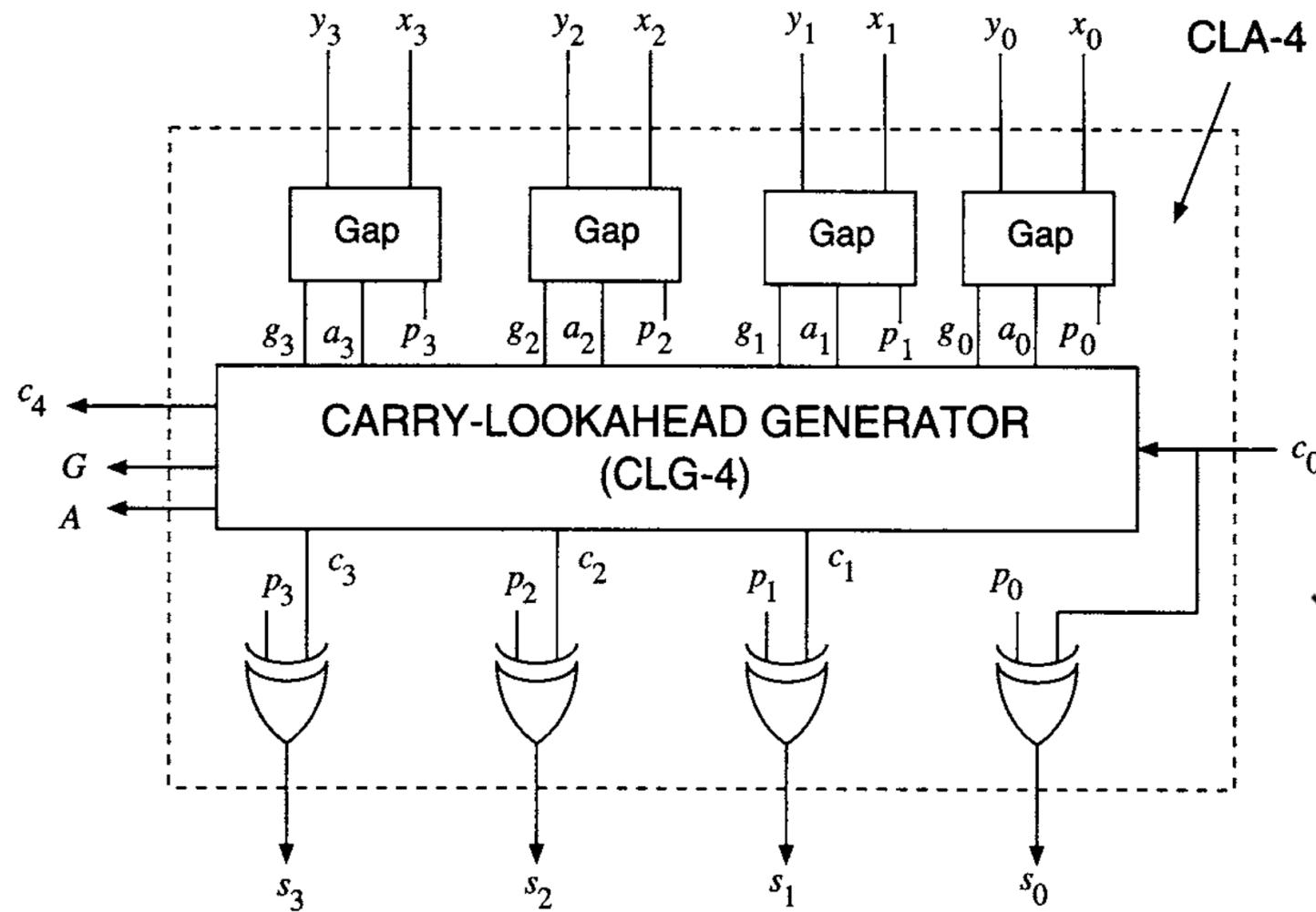
Introduction

A	B	C	G	P	K	C_{out}	S
0	0	0	0	0	1	0	0
		1				0	1
0	1	0	0	1	0	0	1
		1				1	0
1	0	0	0	1	0	0	1
		1				1	0
1	1	0	1	0	0	1	0
		1				1	1

[2] N. H. E. Weste and David Money Harris, *CMOS VLSI design : a circuits and systems perspective*. Noida: Pearson, 2015.



Introduction



$$p_i = x_i \oplus y_i$$

$$g_i = x_i y_i$$

$$s_i = x_i \oplus y_i \oplus c_i = p_i \oplus c_i$$

$$c_{i+1} = g_i + p_i c_i$$

[3] Ercegovac M. D. and Lang T., *Digital arithmetic*. San Francisco, Ca: Morgan Kaufmann Publishers, 2004.



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RTL Design

$$c_{i+1} = g_i + a_i g_{i-1} + a_i a_{i-1} g_{i-2} + \dots + (a_i a_{i-1} \dots a_0) c_0$$

$$c_{i+1} = \text{OR}_{j=0}^i \left(\text{AND}_{k=j+1}^i a_k \right) g_j + \left(\text{AND}_{k=0}^i a_k \right) c_0$$

Optimization-1:

$$T_{1-CLA} = t_{a,g} + \frac{n}{m} t_{clg} + t_s$$



RTL Design

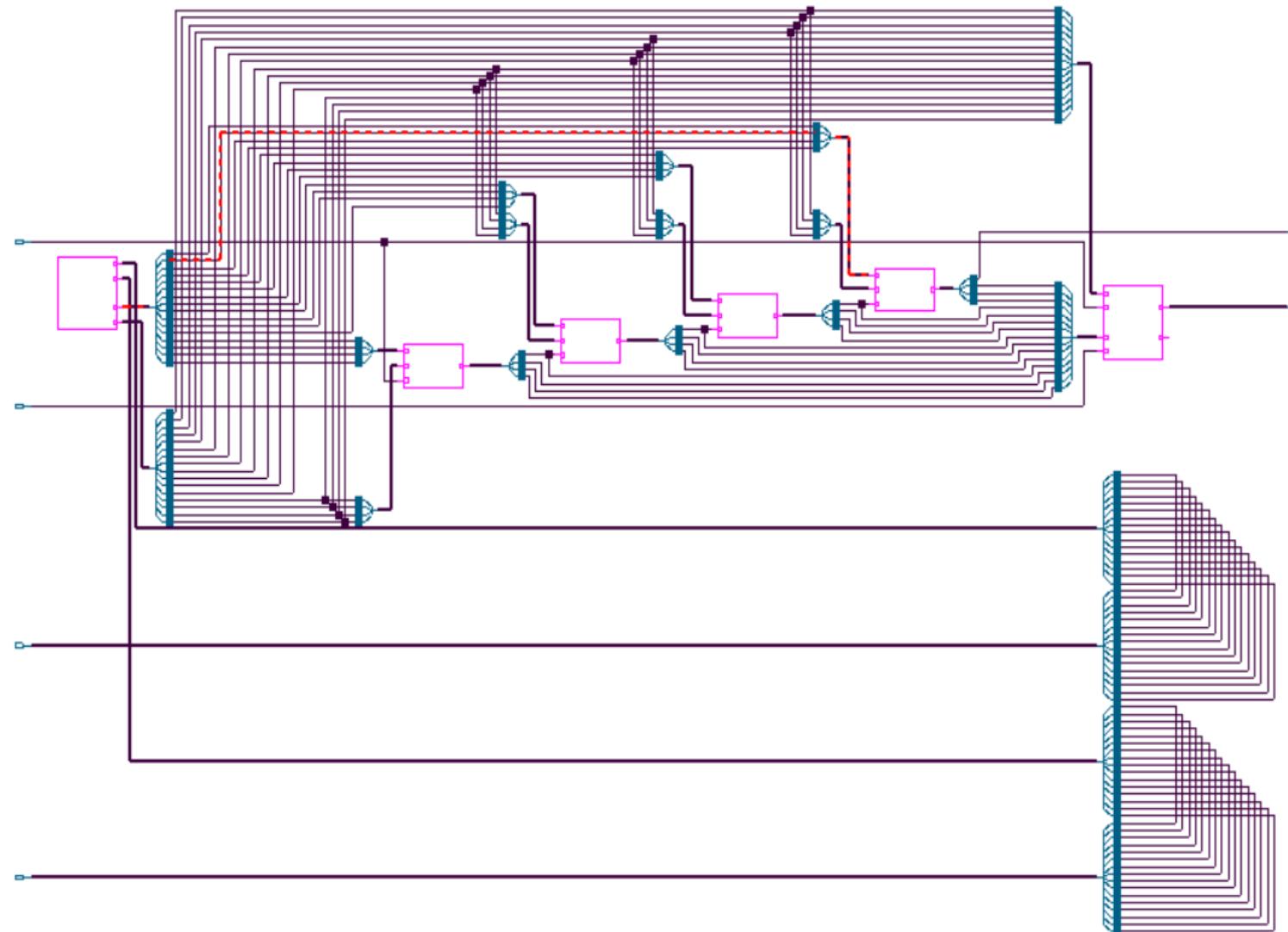
Optimization-1:

$$T_{1\text{-CLA}} = t_{a,g} + \frac{n}{m}t_{clg} + t_s$$

$$\begin{aligned} T_{1\text{-CLA}} &= t_{a,g} + (n/m)t_{clg} + t_s \\ &= t_{a,g} + (16/4)t_{clg} + t_s \\ &= t_{a,g} + 4t_{clg} + t_s \end{aligned}$$

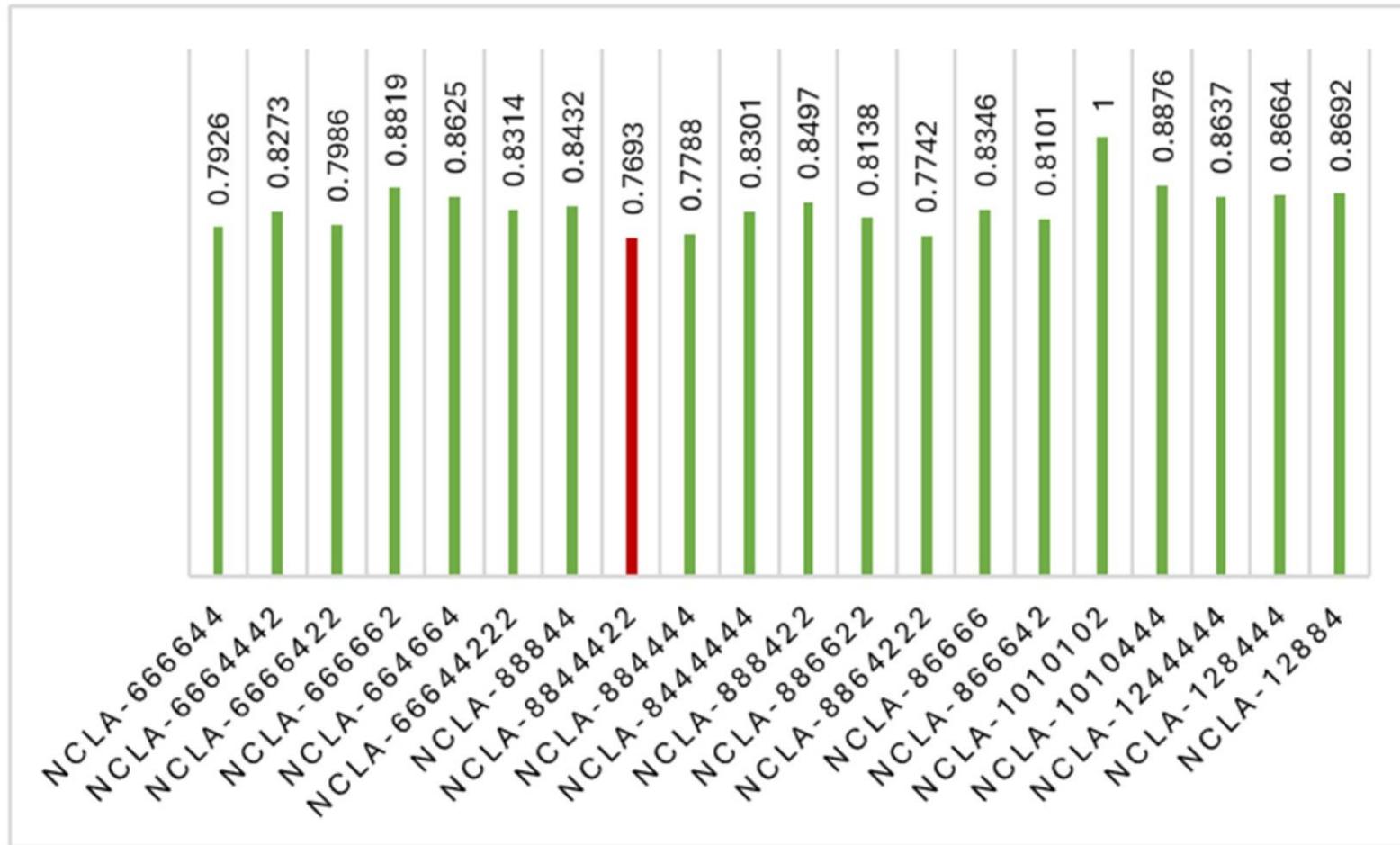


RTL Design



RTL Design (Insert Genus Pic)

Attempted Optimization-1:



[3] P. Balasubramanian and D. L. Maskell, "A New Carry Look-Ahead Adder Architecture Optimized for Speed and Energy," *Electronics*, vol. 13, no. 18, pp. 3668–3668, Sep. 2024, doi: <https://doi.org/10.3390/electronics13183668>.



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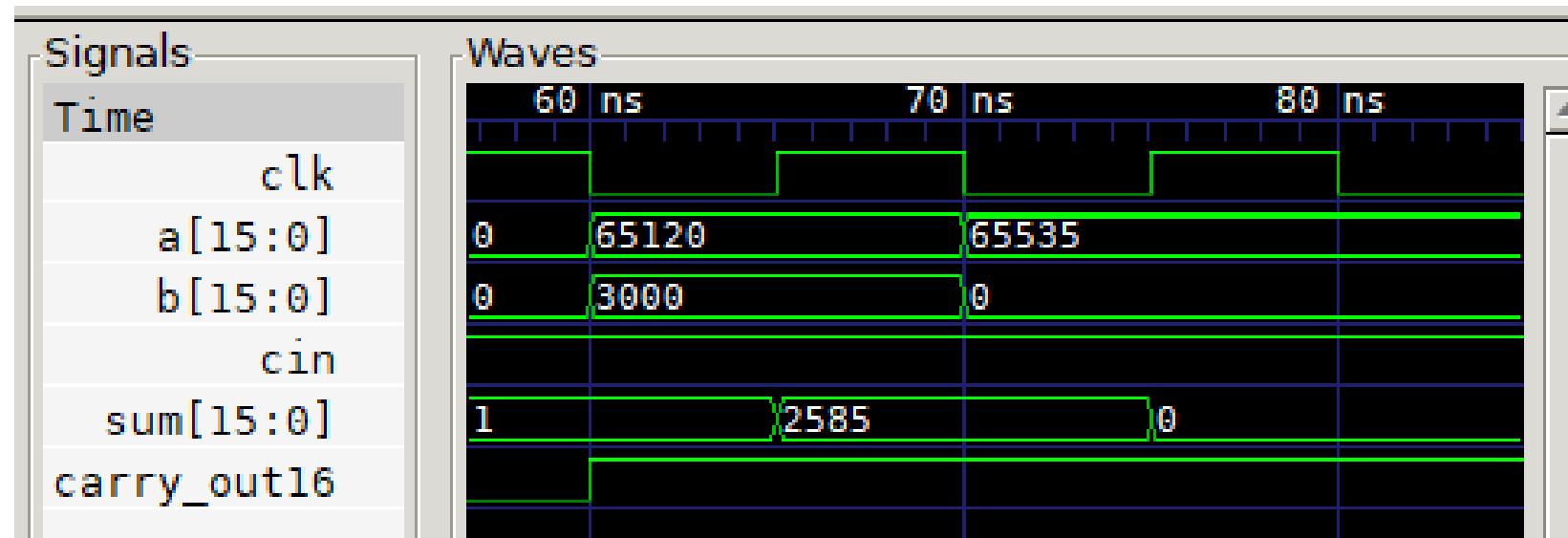
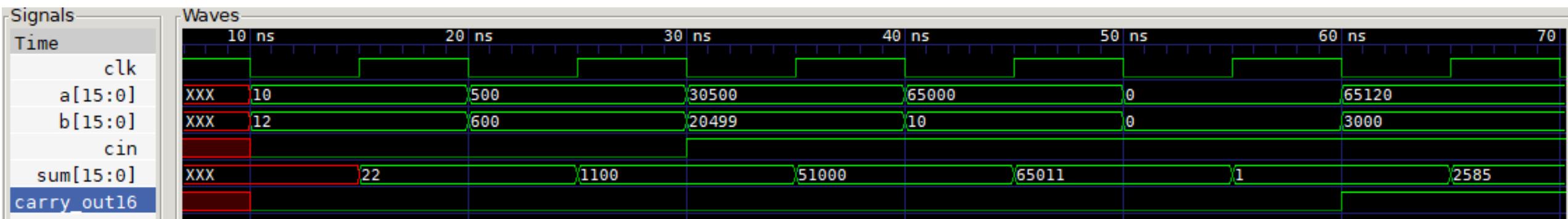
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Directed Testbench



Self Checking Testbench

----- CLA Testbench Results -----						
Time	a (Binary)	b (Binary)	cin	sum (Binary)	sum (Decimal)	carry_out
20000	000000000001010	000000000001100	0	0000000000010110	22	0
	PASS: sum = 0000000000010110					
30000	000000011110100	000001001011000	0	0000010001001100	1100	0
	PASS: sum = 0000010001001100					
40000	0111011100100100	0101000000010011	1	1100011100111000	51000	0
	PASS: sum = 1100011100111000					
50000	111110111101000	000000000001010	1	111110111110011	65011	0
	PASS: sum = 111110111110011					
60000	000000000000000	000000000000000	1	000000000000001	1	0
	PASS: sum = 000000000000001					
70000	111111001100000	0000101110111000	1	0000101000011001	2585	1
	PASS: sum = 0000101000011001					
80000	111111111111111	000000000000000	1	000000000000000	0	1
	PASS: sum = 000000000000000					



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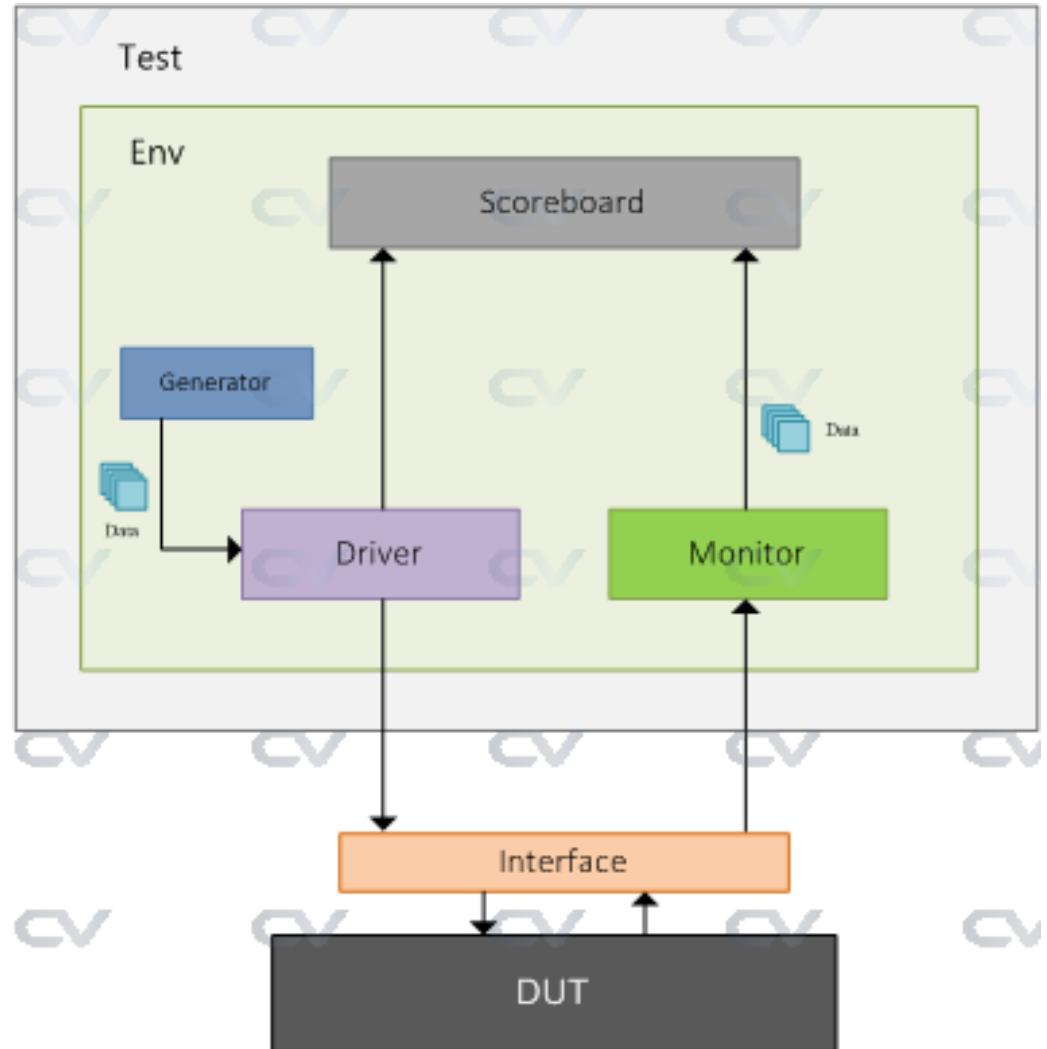
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Layered testbench



```
source xsim.dir/top/xsim_script.tcl
# xsim {top} -autoloadwcfg -runall
Time resolution is 1 ps
run -all
-----Scoreboard Test Starts-----
Data flow: Passed 200 out of Total 200 Tests
-----Scoreboard Test Ends-----
$finish called at time : 2015 ns : File "C:/SPB_Data/EEE468_Jan2024/p_layered_tb.sv" Line 196
exit
INFO: [Common 17-206] Exiting xsim at Fri Dec 6 17:50:52 2024...
```

[4] “SystemVerilog TestBench,” ChipVerify. <https://www.chipverify.com/systemverilog/systemverilog-simple-testbench>



Layered testbench: 3D Space

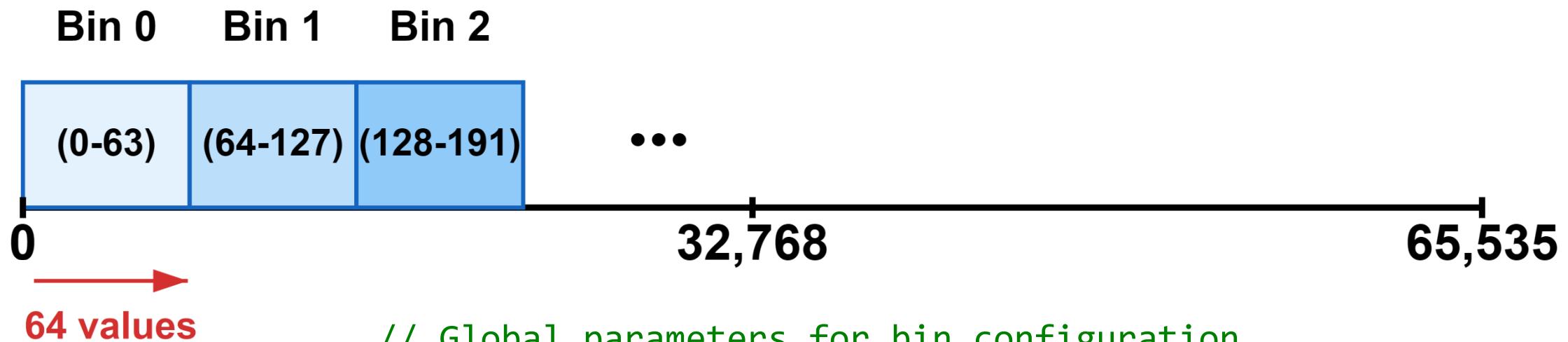
input c 2^2
input [15:0] a $x 2^{16}$
input [15:0] b $x 2^{16}$

$$= 8589934592$$
$$\approx 8.5 \text{ Billion Points}$$

Layered testbench: 3D Space

16-bit Input Range Coverage

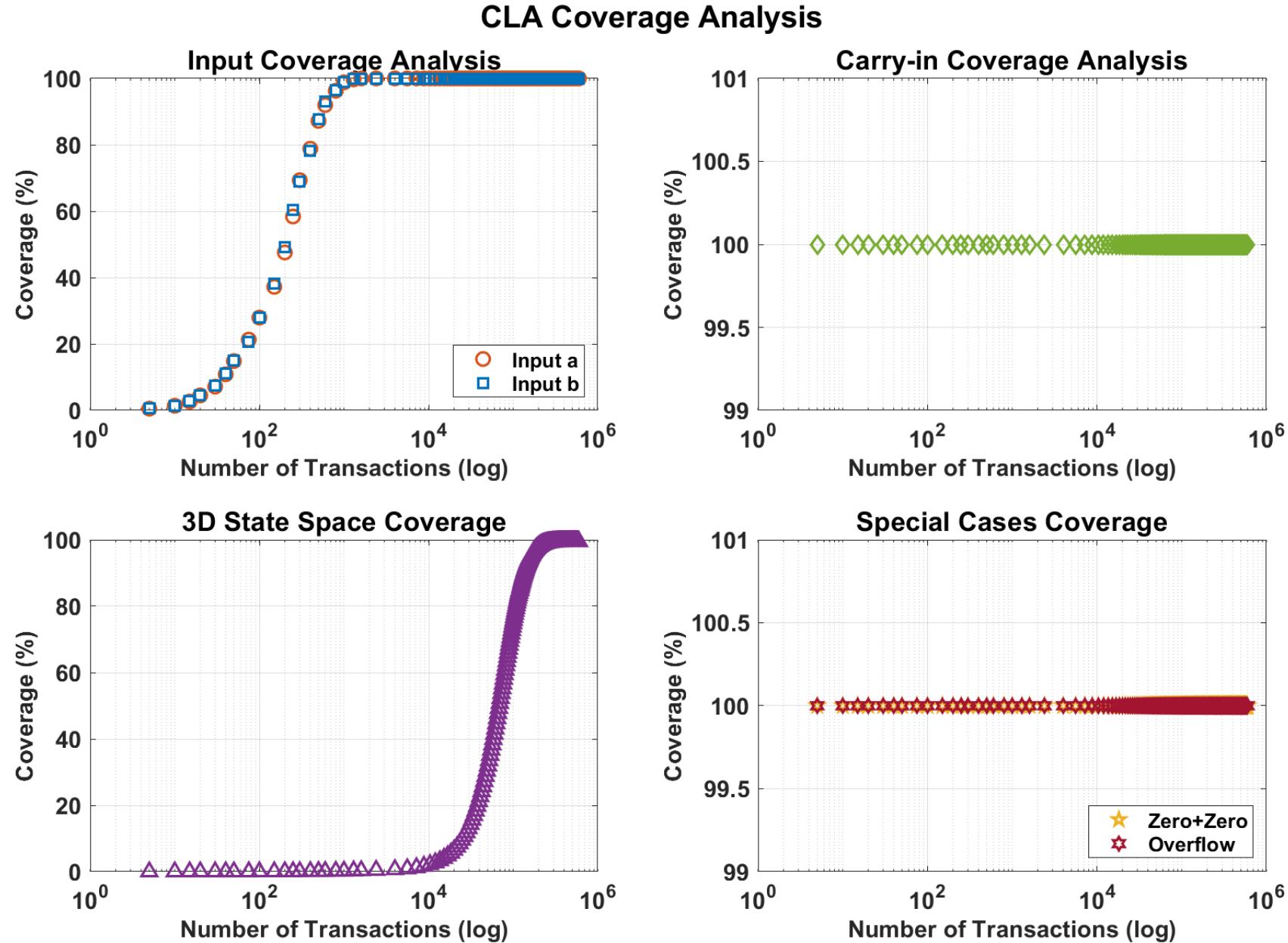
$$1024 \text{ Bins} \times 64 \text{ Values} = 65,536 (2^{16})$$



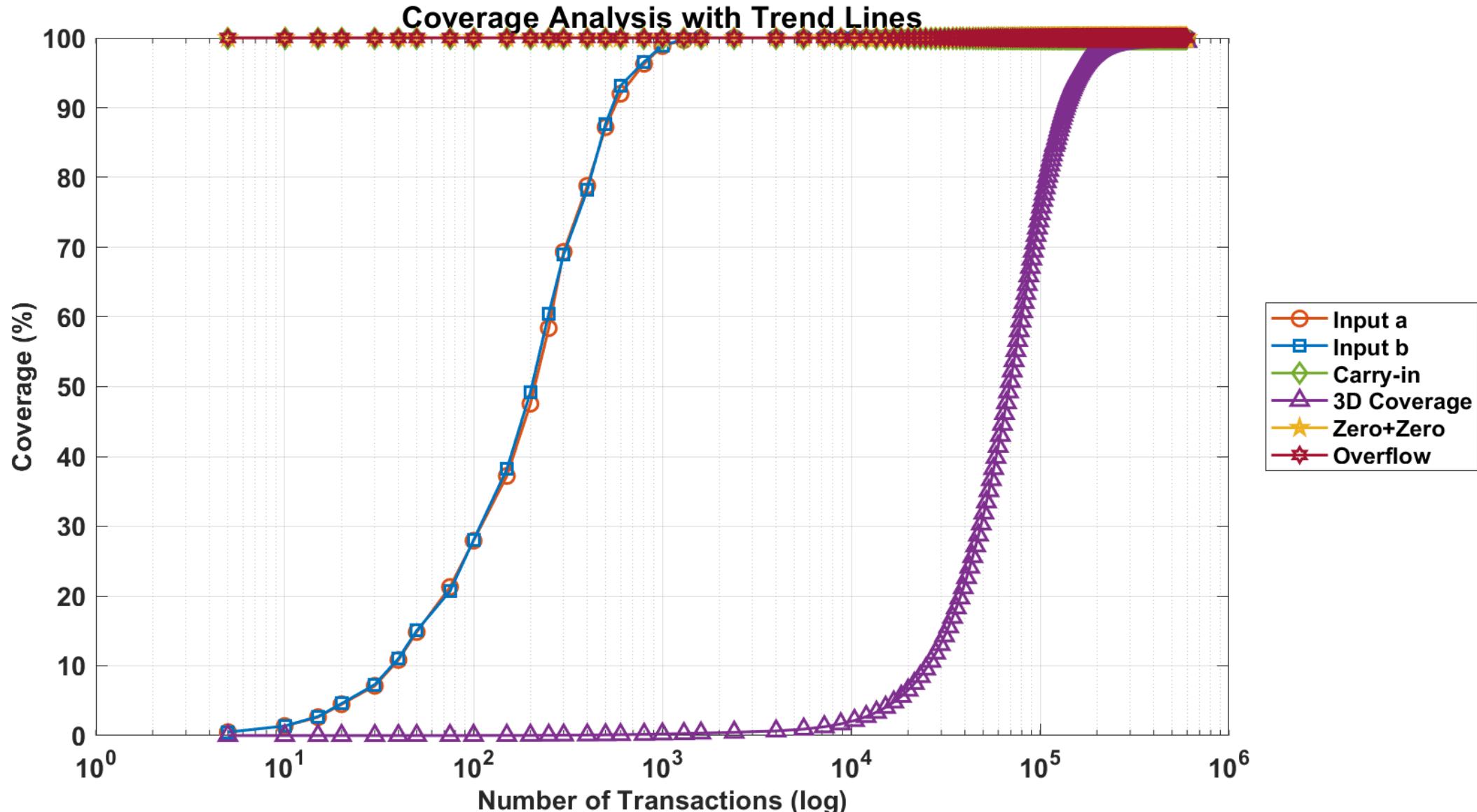
```
// Global parameters for bin configuration
parameter int BIN_COUNT = 1024;
parameter int BIN_BITS = $clog2(BIN_COUNT);
// Basic parameters for coverage tracking
localparam int TOTAL_3D_POINTS = 2 * BIN_COUNT * BIN_COUNT;
```

Layered Testbench: Coverage with Transactions

- Rand Function
- Up to 240k Transactions
- Non-linear Manual Setup
- 1024 Bins for 16 Bit Input Range
- Data Collection in File
- All Compare Function



Layered Testbench: Coverage with Transactions



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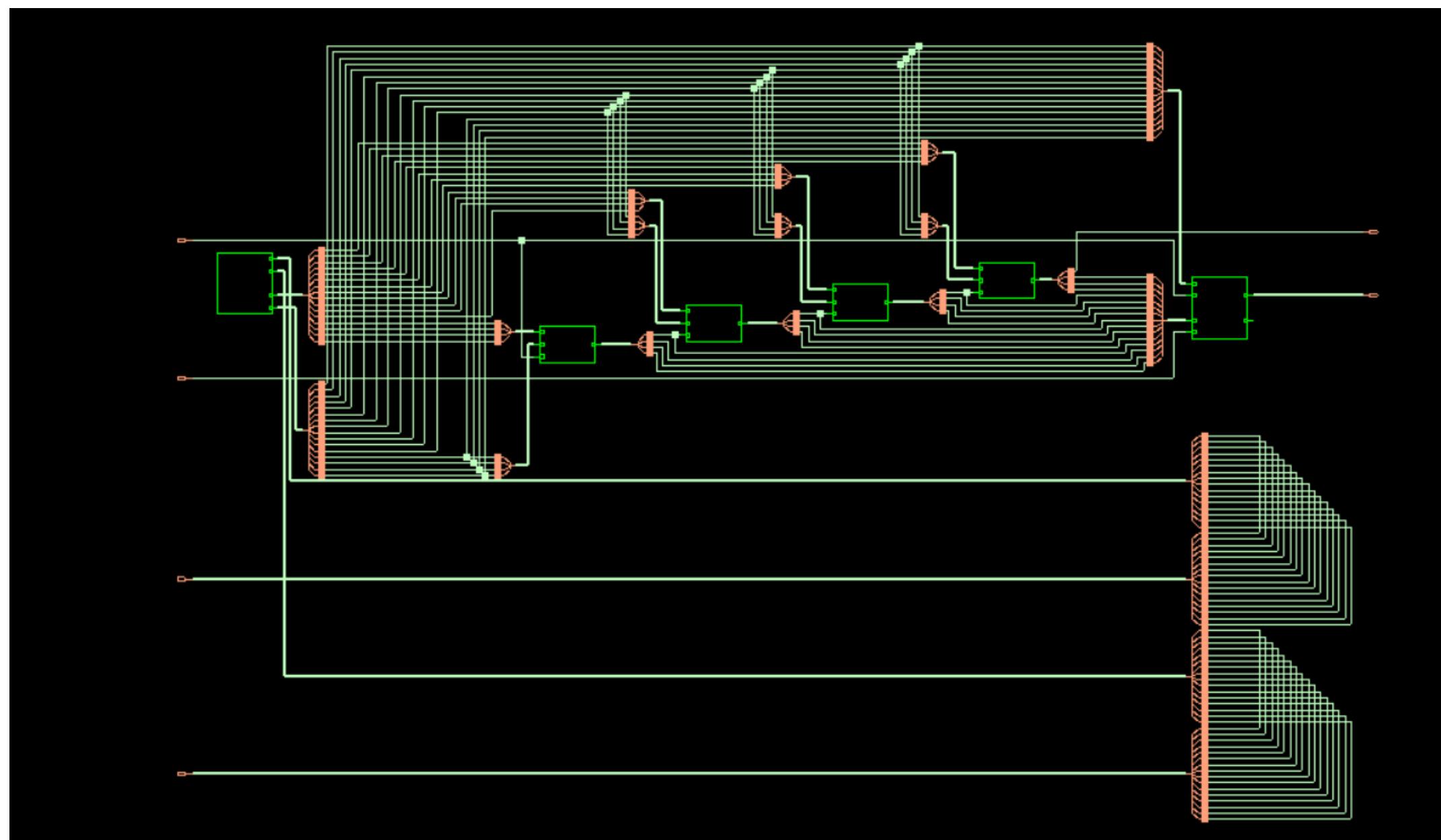


Fig: Schematic of Carry Lookahead Adder



Generated by: Genus(TM) Synthesis Solution 16.13-s036_1 (Dec 20 2016)

Generated on: Dec 07 2024 21:36:01

Module: cla_top

Technology library: slow_vdd1v0 1.0

Operating conditions: PVT_0P9V_125C (balanced_tree)

Wireload mode: enclosed

Type	Cell Area	Area %
datapath	0.00	0.00
external	0.00	0.00
others	169.63	100.00
TOTAL	169.63	100.00

Close

Help

Fig: Report Of Datapath Area

Generated by: Genus(TM) Synthesis Solution 16.13-s036_1 (Dec 20 2016)

Generated on: Dec 07 2024 21:38:24

Module: cla_top

Technology library: slow_vdd1v0 1.0

Operating conditions: PVT_0P9V_125C (balanced_tree)

Wireload mode: enclosed

Instance	Cells	Leakage (nW)	Internal (nW)	Net (nW)	Switching (nW)
cla_top	48	3.42	2650.25	331.28	2981.53
cla_top/carry_unit1	4	0.11	79.29	35.44	114.72
cla_top/carry_unit2	4	0.11	83.87	36.70	120.58
cla_top/carry_unit3	4	0.11	51.52	22.78	74.30
cla_top/carry_unit4	4	0.11	59.45	18.98	78.43
cla_top/gen_prop_inst	0	0.00	0.00	80.58	80.58
cla_top/sum_unit	32	2.98	2376.12	100.30	2476.42

[Close](#)

[Help](#)

Fig: Power Report

SDC Code:

```
# setting up time units
set_units -time 1ns -capacitance pF
# setting the clock period 10ns, as period = 1/freq, here, freq = 100MHz
set clock_period 10;
set top_module "cla_top"
set clock_port {clk};
# setting the input ports in a list to a variable
set input_ports {a, b, cin} ;
# setting the output ports in a list to a variable
set output_ports {sum, carry_out16} ;
# define the clocks
create_clock -period ${clock_period} -waveform {0 6} -name func_clk
[get_ports ${clock_port}]
# setting up constraints for the reset signal
# Define input delays
set_input_delay 0.4 -clock [get_clocks {func_clk}] ${input_ports}
# Define output delays
set_output_delay 0.6 -clock [get_clocks {func_clk}] ${output_ports}
```

- **No Reset Port As Per Project Requirement**
- **No Multicycle Setup Time/Hold Time**



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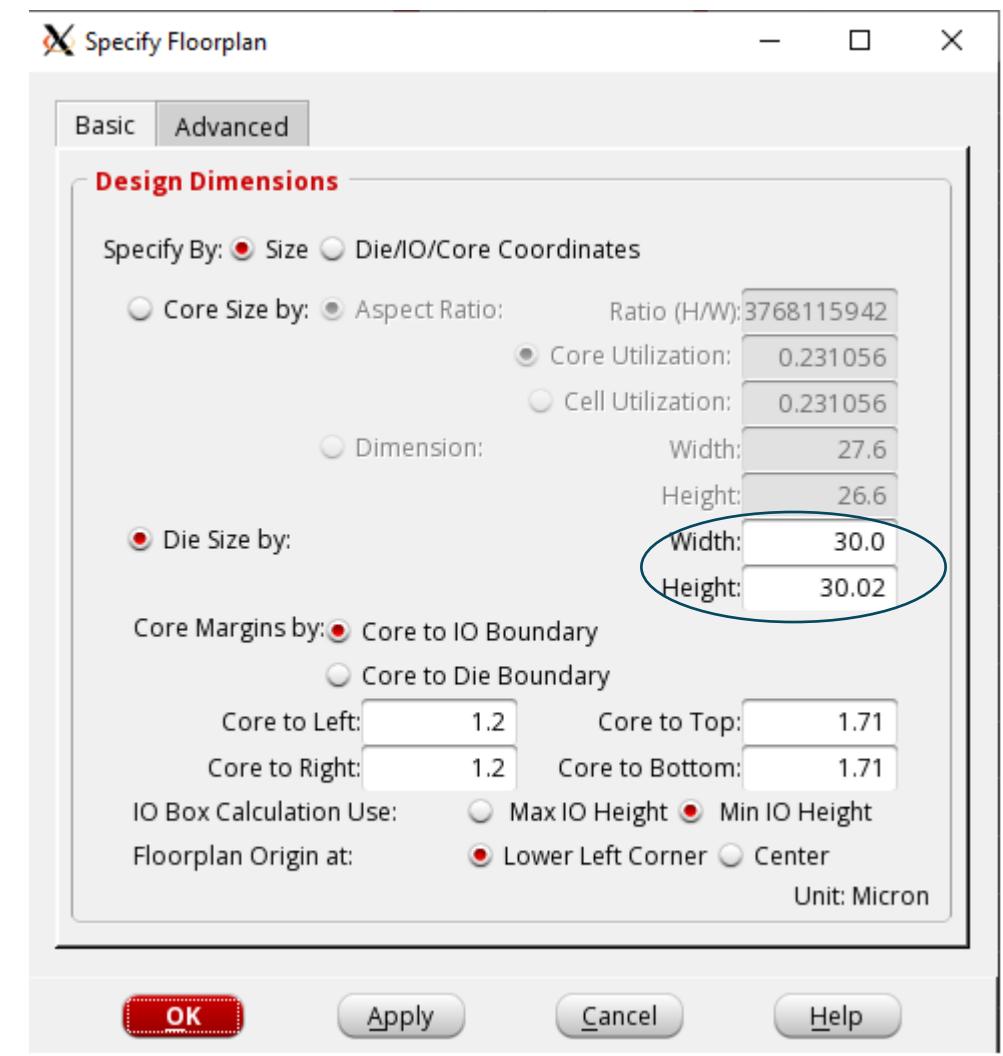
PnR with DRC

Optimization

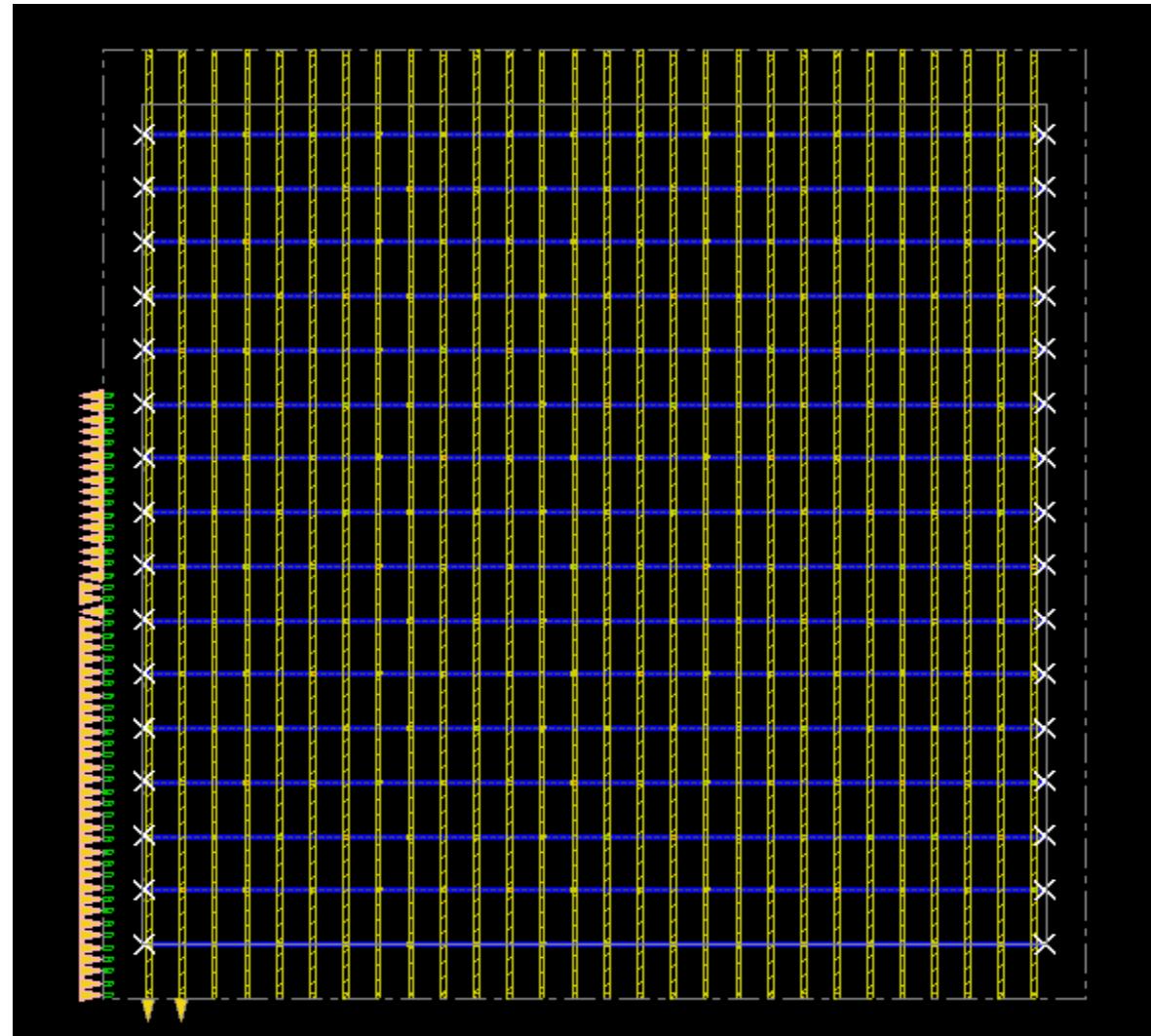
Acknowledgement and References



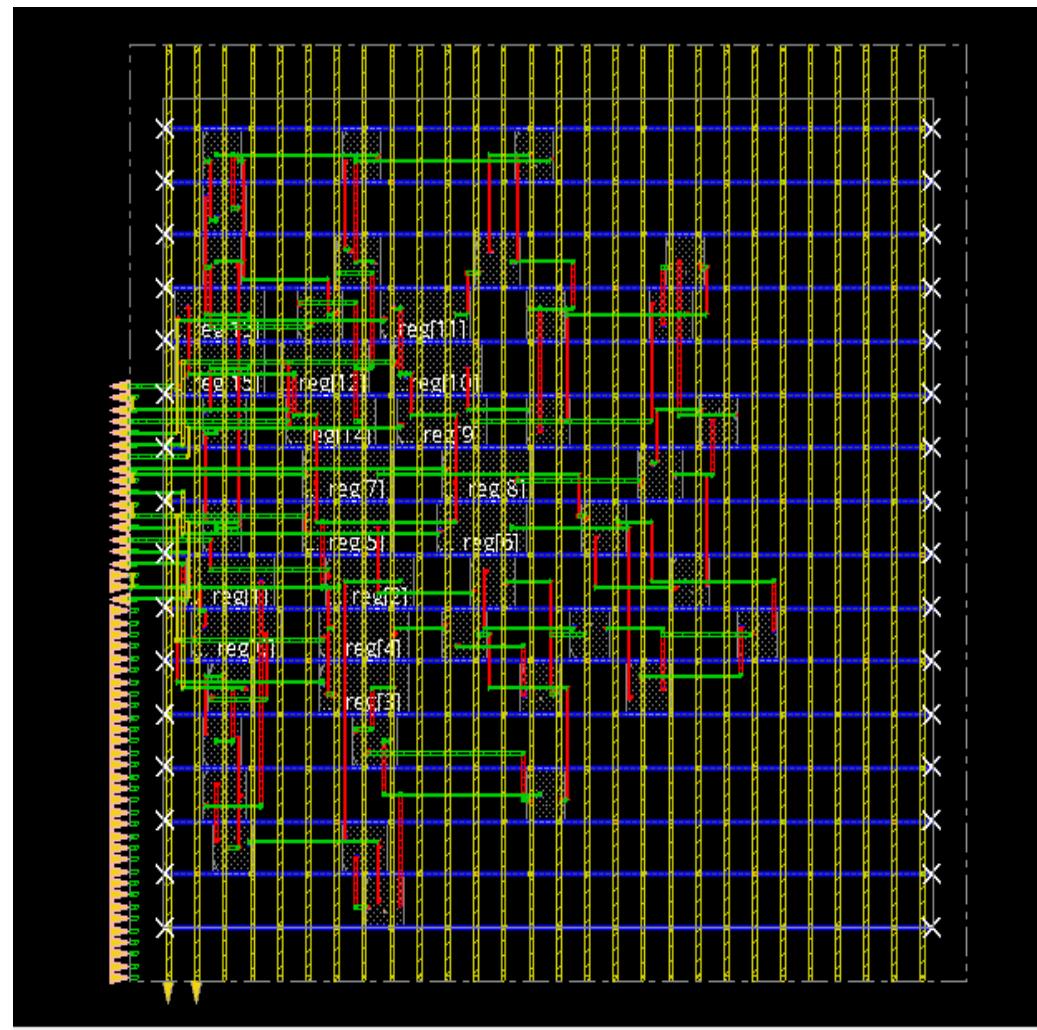
Floorplanning :



Creating Power Mesh



Placement



optDesign Final Summary

Setup views included:

func@BC rcbest0.hold

Setup mode	all	reg2reg	default
WNS (ns):	8.451	N/A	8.451
TNS (ns):	0.000	N/A	0.000
Violating Paths:	0	N/A	0
All Paths:	17	N/A	17

DRVs	Real		Total
	Nr nets(terms)	Worst Vio	Nr nets(terms)
max_cap	0 (0)	0.000	0 (0)
max_tran	0 (0)	0.000	0 (0)
max_fanout	0 (0)	0	0 (0)
max_length	0 (0)	0	0 (0)

Density: 23.961

Routing Overflow: 0.00% H and 0.00% V

****optDesign ... cpu = 0:00:05, real = 0:00:06, mem = 1329.4M, totSessionCpu=0:00:49 ****

Clock Tree Synthesis (CTS)

```
Synthesizing clock trees done.
Connecting clock gate test enables...
Connecting clock gate test enables done.
**WARN: (IMPCCOPT-2015): Innovus will not update I/O latencies for the following reason(s):
* The following are in propagated mode:
- SDC clock func_clk in view func@BC_rcbest0.hold
- Root pin clk of SDC clock func_clk in view func@BC_rcbest0.hold

Resetting all latency settings from fanout cone of clock 'func_clk'
Clock DAG stats after update timingGraph:
cell counts      : b=0, i=0, icg=0, nicg=0, l=0, total=0
cell areas       : b=0.000um^2, i=0.000um^2, icg=0.000um^2, nicg=0.000um^2, l=0.000um^2, total=0.000um^2
cell capacitance : b=0.000pF, i=0.000pF, icg=0.000pF, nicg=0.000pF, l=0.000pF, total=0.000pF
sink capacitance : count=16, total=0.005pF, avg=0.000pF, sd=0.000pF, min=0.000pF, max=0.000pF
wire capacitance : top=0.000pF, trunk=0.000pF, leaf=0.004pF, total=0.004pF
wire lengths     : top=0.000um, trunk=0.000um, leaf=43.970um, total=43.970um
Clock DAG net violations after update timingGraph: none
Clock DAG transition distribution after update timingGraph:
Leaf : target=0.035ns count=1 avg=0.004ns sd=0.000ns min=0.004ns max=0.004ns {1 < 0.007ns}
Skew group summary after update timingGraph:
skew_group func_clk/func: insertion delay [min=0.000, max=0.000, avg=0.000, sd=0.000], skew [0.000 vs 0.026, 100% {0.000, 0.000, 0.000}] (wid=0.000 ws=0.000) (gid=0.00 gs=0.000)
Clock network insertion delays are now [0.000ns, 0.000ns] average 0.000ns std.dev 0.000ns
Logging CTS constraint violations...
No violations found.
Logging CTS constraint violations done.
Synthesizing clock trees with CCOpt done.

*** Summary of all messages that are not suppressed in this session:
Severity ID          Count Summary
WARNING IMPEXT-3530      5 The process node is not set. Use the com...
WARNING IMPCCOPT-1361      3 Routing configuration for %s nets in clo...
WARNING IMPCCOPT-5046      1 Net '%s' in clock tree '%s' has existing...
WARNING IMPCCOPT-5047      1 Found %d clock net(s) with existing rout...
WARNING IMPCCOPT-2015      2 %s will not update I/O latencies for the...

*** Message Summary: 12 warning(s), 0 error(s)
```



Timedesign Post CTS

timeDesign Summary

Setup views included:
func@BC_rcbest0.hold

Setup mode	all	reg2reg	default
WNS (ns):	8.451	N/A	8.451
TNS (ns):	0.000	N/A	0.000
Violating Paths:	0	N/A	0
All Paths:	17	N/A	17

DRVs	Real		Total
	Nr nets(terms)	Worst Vio	Nr nets(terms)
max_cap	0 (0)	0.000	0 (0)
max_tran	0 (0)	0.000	0 (0)
max_fanout	0 (0)	0	0 (0)
max_length	0 (0)	0	0 (0)

Density: 23.961%
Routing Overflow: 0.00% H and 0.00% V

Reported timing to dir ./timingReports
Total CPU time: 0.22 sec
Total Real time: 1.0 sec
Total Memory Usage: 1295.875 Mbytes

timeDesign Summary

Hold views included:
func@BC_rcbest0.hold

Hold mode	all	reg2reg	default
WNS (ns):	0.425	N/A	0.425
TNS (ns):	0.000	N/A	0.000
Violating Paths:	0	N/A	0
All Paths:	17	N/A	17

Density: 23.961%

Reported timing to dir ./timingReports
Total CPU time: 0.46 sec
Total Real time: 1.0 sec
Total Memory Usage: 1374.425781 Mbytes
Reset AAE Options

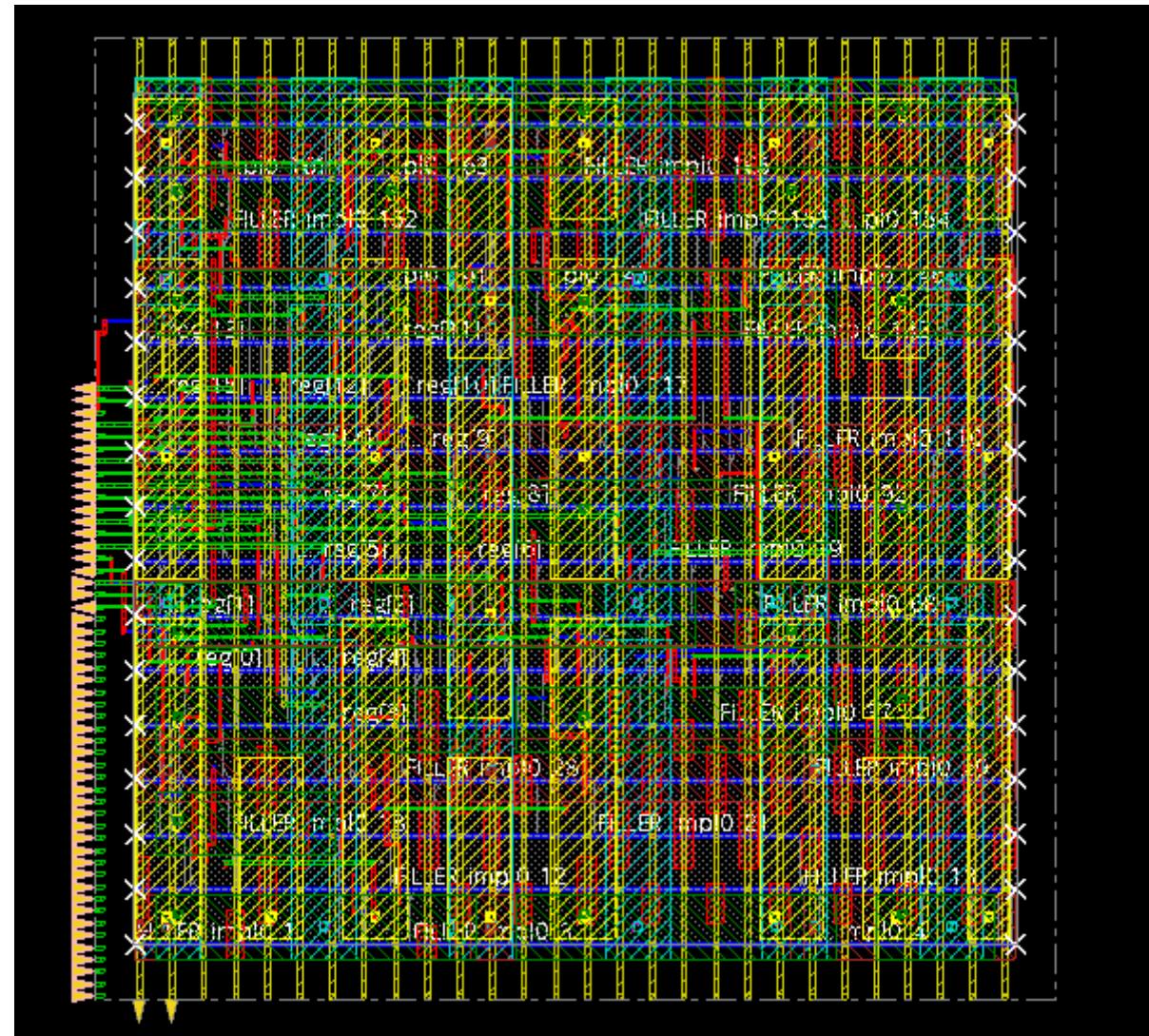


Post-Route timing and SI Optimization

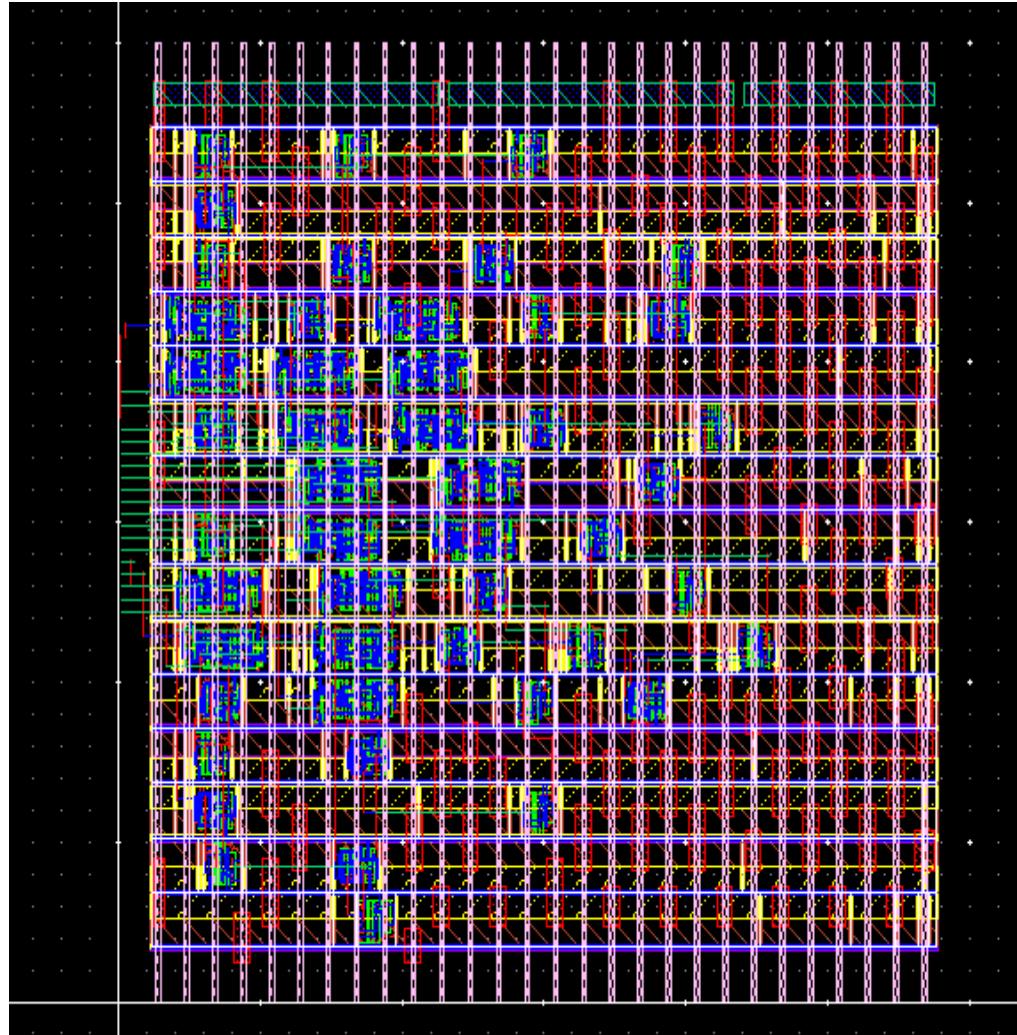
```
innovus 27> innovus 27> *** Starting Verify Geometry (MEM: 1494.2) ***  
  
**WARN: (IMPVFG-257): verifyGeometry command is replaced by verify_drc command. It still works in this release but will be removed in future release. Please update your script to use the new command.  
VERIFY GEOMETRY ..... Starting Verification  
VERIFY GEOMETRY ..... Initializing  
VERIFY GEOMETRY ..... Deleting Existing Violations  
VERIFY GEOMETRY ..... Creating Sub-Areas  
..... bin size: 1920  
VERIFY GEOMETRY ..... SubArea : 1 of 1  
VERIFY GEOMETRY ..... Cells : 0 Viols.  
VERIFY GEOMETRY ..... SameNet : 0 Viols.  
VERIFY GEOMETRY ..... Wiring : 0 Viols.  
VERIFY GEOMETRY ..... Antenna : 0 Viols.  
VERIFY GEOMETRY ..... Sub-Area : 1 complete 0 Viols. 0 Wrngs.  
VG: elapsed time: 0.00  
Begin Summary ...  
Cells : 0  
SameNet : 0  
Wiring : 0  
Antenna : 0  
Short : 0  
Overlap : 0  
End Summary  
Verification Complete : 0 Viols. 0 Wrngs.  
*****End: VERIFY GEOMETRY*****  
*** verify geometry (CPU: 0:00:00.1 MEM: 171.2M)
```



Adding filler cell and metal filling



DRC Check:



```
TWO LAYER BOOLEAN: Cumulative Time CPU = 0(s) REAL = 0(s)
POLYGON TOPOLOGICAL: Cumulative Time CPU = 0(s) REAL = 0(s)
POLYGON MEASUREMENT: Cumulative Time CPU = 0(s) REAL = 0(s)
SIZE: Cumulative Time CPU = 0(s) REAL = 0(s)
EDGE TOPOLOGICAL: Cumulative Time CPU = 0(s) REAL = 0(s)
EDGE MEASUREMENT: Cumulative Time CPU = 0(s) REAL = 0(s)
STAMP: Cumulative Time CPU = 0(s) REAL = 0(s)
ONE LAYER DRC: Cumulative Time CPU = 0(s) REAL = 0(s)
TWO LAYER DRC: Cumulative Time CPU = 0(s) REAL = 0(s)
    NET AREA: Cumulative Time CPU = 0(s) REAL = 0(s)
    DENSITY: Cumulative Time CPU = 0(s) REAL = 0(s)
MISCELLANEOUS: Cumulative Time CPU = 0(s) REAL = 0(s)
    CONNECT: Cumulative Time CPU = 0(s) REAL = 0(s)
    DEVICE: Cumulative Time CPU = 0(s) REAL = 0(s)
    ERC: Cumulative Time CPU = 0(s) REAL = 0(s)
PATTERN_MATCH: Cumulative Time CPU = 0(s) REAL = 0(s)
DFM FILL: Cumulative Time CPU = 0(s) REAL = 0(s)

Total CPU Time : 1(s)
Total Real Time : 1(s)
Peak Memory Used : 20(M)
Total Original Geometry : 1218(12825)
Total DRC RuleChecks : 562
Total DRC Results : 0 (0)
Summary can be found in file cla_top.sum
ASCII report database is /home/vlsi22/anila/akif/Project_CLA/cds_digital/cla_synth/newINNO/cla_top.drc_errors.ascii
Checking in all Softshare licenses.

Design Rule Check Finished Normally. Sat Dec 7 12:45:04 2024
```



Report Timing

```
#####
# Generated by: Cadence Innovus 16.10-p004_1
# OS: Linux x86_64 (Host ID CadenceServer3.localdomain)
# Generated on: Sat Dec 7 12:26:17 2024
# Design: cla_top
# Command: report_timing
#####
Path 1: MET Late External Delay Assertion
Endpoint: carry_out16 (^) checked with leading edge of 'func_clk'
Beginpoint: cin (^) triggered by leading edge of 'func_clk'
Path Groups: {func_clk}
Analysis View: func@BC_rcbest0.hold
Other End Arrival Time 0.000
- External Delay 0.600
+ Phase Shift 10.000
= Required Time 9.400
- Arrival Time 0.949
= Slack Time 8.451
    Clock Rise Edge 0.000
    + Input Delay 0.400
    = Beginpoint Arrival Time 0.400
+-----+
| Instance | Arc | Cell | Delay | Arrival | Required |
|          |     |      |       | Time   | Time   |
|-----+-----+-----+-----+-----+-----+
|          | cin ^ |       |       | 0.400 | 8.851 |
| carry_unit1/g62 | Al ^ -> Y ^ | AO21XL | 0.031 | 0.431 | 8.882 |
| carry_unit1/g61 | Al ^ -> Y ^ | AO21XL | 0.034 | 0.465 | 8.915 |
| carry_unit1/g60 | Al ^ -> Y ^ | AO21XL | 0.036 | 0.501 | 8.951 |
| carry_unit1/g59 | Al ^ -> Y ^ | AO21XL | 0.036 | 0.536 | 8.987 |
| carry_unit2/g62 | Al ^ -> Y ^ | AO21XL | 0.035 | 0.571 | 9.022 |
| carry_unit2/g61 | Al ^ -> Y ^ | AO21XL | 0.034 | 0.605 | 9.056 |
| carry_unit2/g60 | Al ^ -> Y ^ | AO21XL | 0.035 | 0.640 | 9.090 |
| carry_unit2/g59 | Al ^ -> Y ^ | AO21XL | 0.034 | 0.674 | 9.124 |
| carry_unit3/g62 | Al ^ -> Y ^ | AO21XL | 0.034 | 0.708 | 9.158 |
| carry_unit3/g61 | Al ^ -> Y ^ | AO21XL | 0.036 | 0.744 | 9.194 |
| carry_unit3/g60 | Al ^ -> Y ^ | AO21XL | 0.035 | 0.779 | 9.229 |
| carry_unit3/g59 | Al ^ -> Y ^ | AO21XL | 0.036 | 0.815 | 9.265 |
| carry_unit4/g62 | Al ^ -> Y ^ | AO21XL | 0.035 | 0.849 | 9.300 |
| carry_unit4/g61 | Al ^ -> Y ^ | AO21XL | 0.035 | 0.885 | 9.335 |
| carry_unit4/g60 | Al ^ -> Y ^ | AO21XL | 0.036 | 0.920 | 9.371 |
| carry_unit4/g59 | Al ^ -> Y ^ | AO21XL | 0.029 | 0.949 | 9.400 |
|          | carry_out16 ^ |       | 0.000 | 0.949 | 9.400 |
```



Report Area

innovus 20> report_area				
Depth	Name	#Inst	Area (um^2)	

0	cla_top	48	169.632	
1	gen_prop_inst	0	0.0	
1	carry_unit3	4	9.576	
1	carry_unit1	4	9.576	
1	sum_unit	32	131.328	
1	carry_unit4	4	9.576	
1	carry_unit2	4	9.576	
1				

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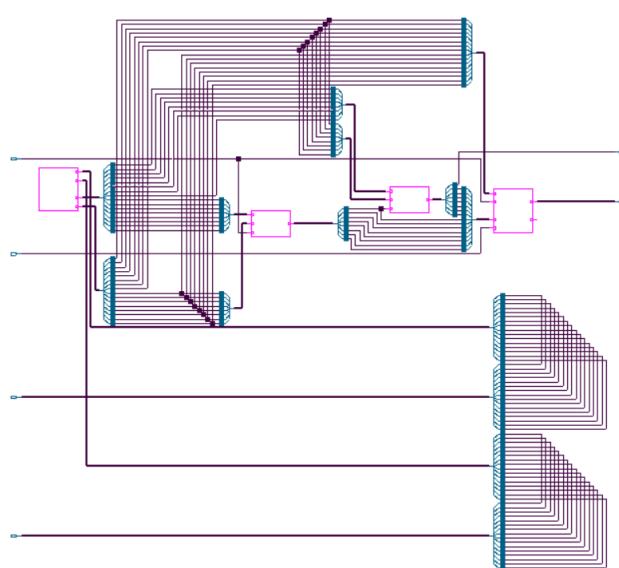
Optimization Summary

Acknowledgement and References

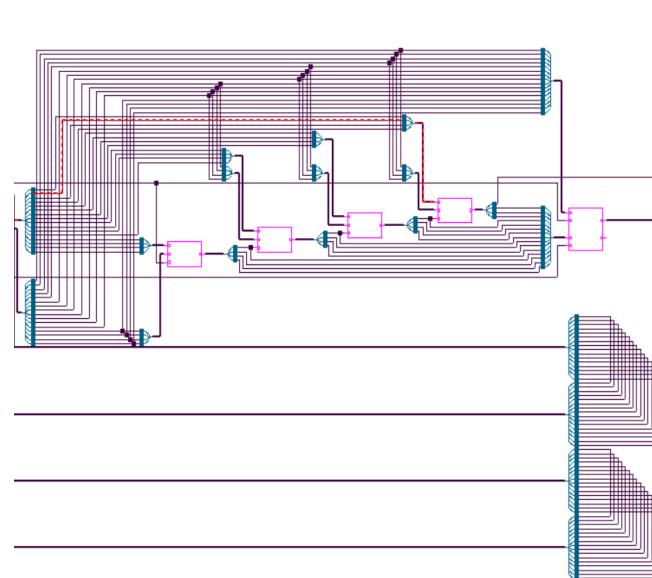


Design Consideration:

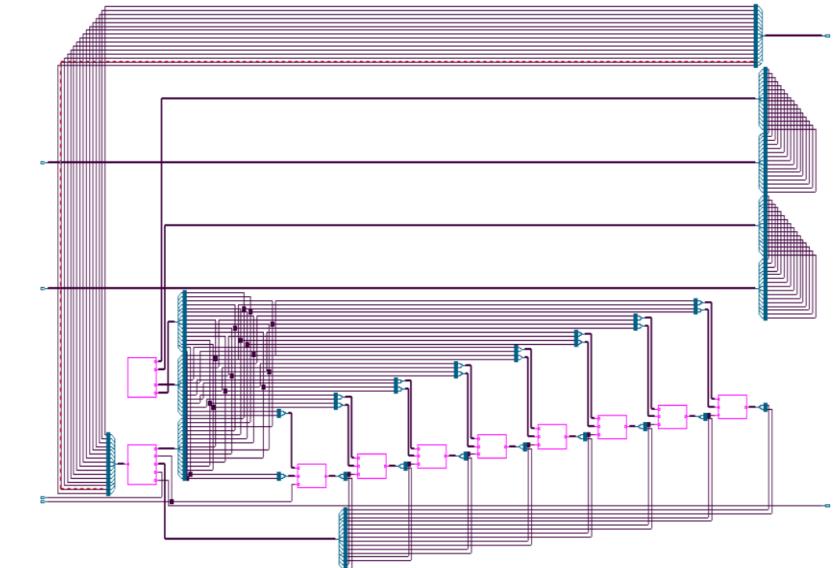
2 Carry Unit Blocks



4 Carry Unit Blocks



8 Carry Unit Blocks

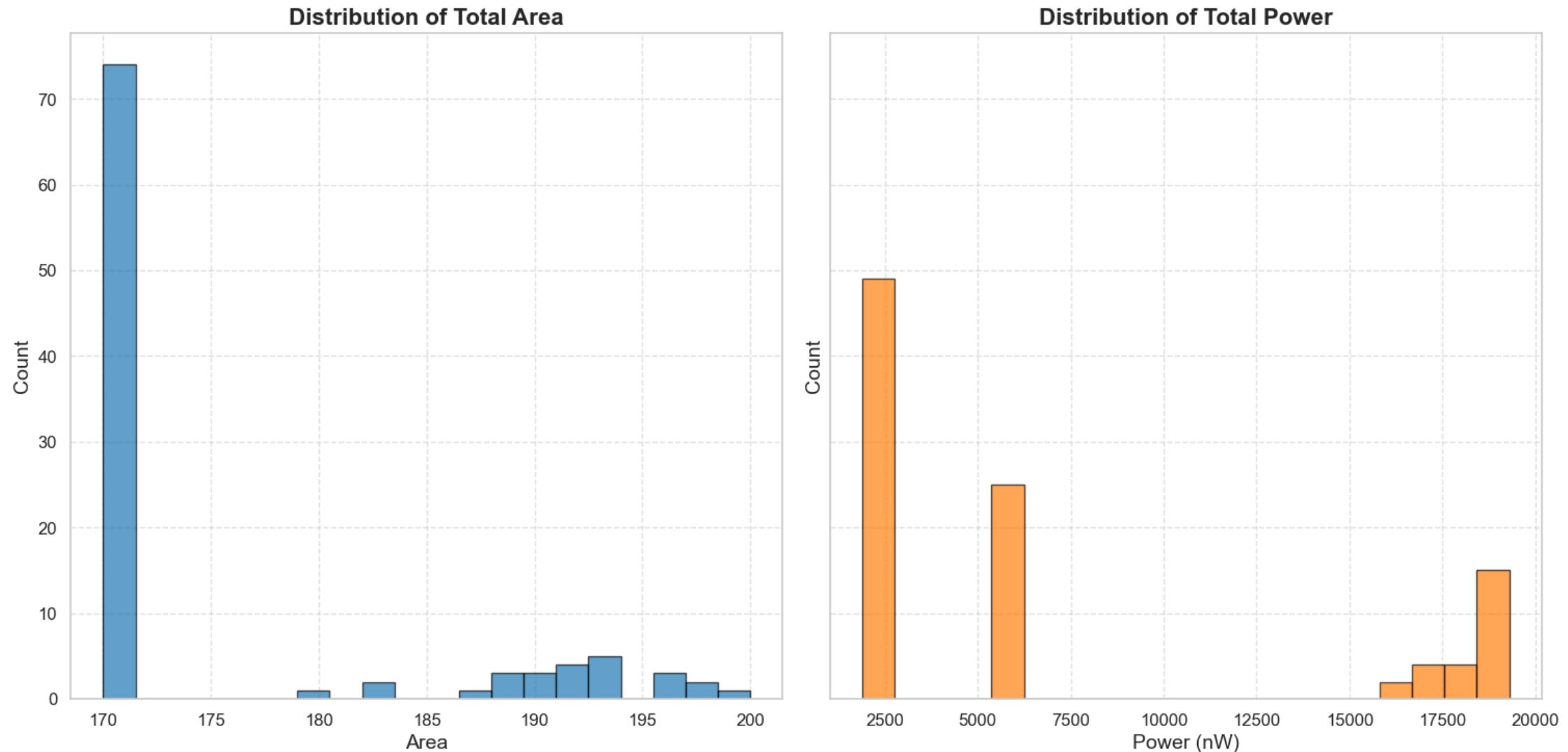


Design Consideration:

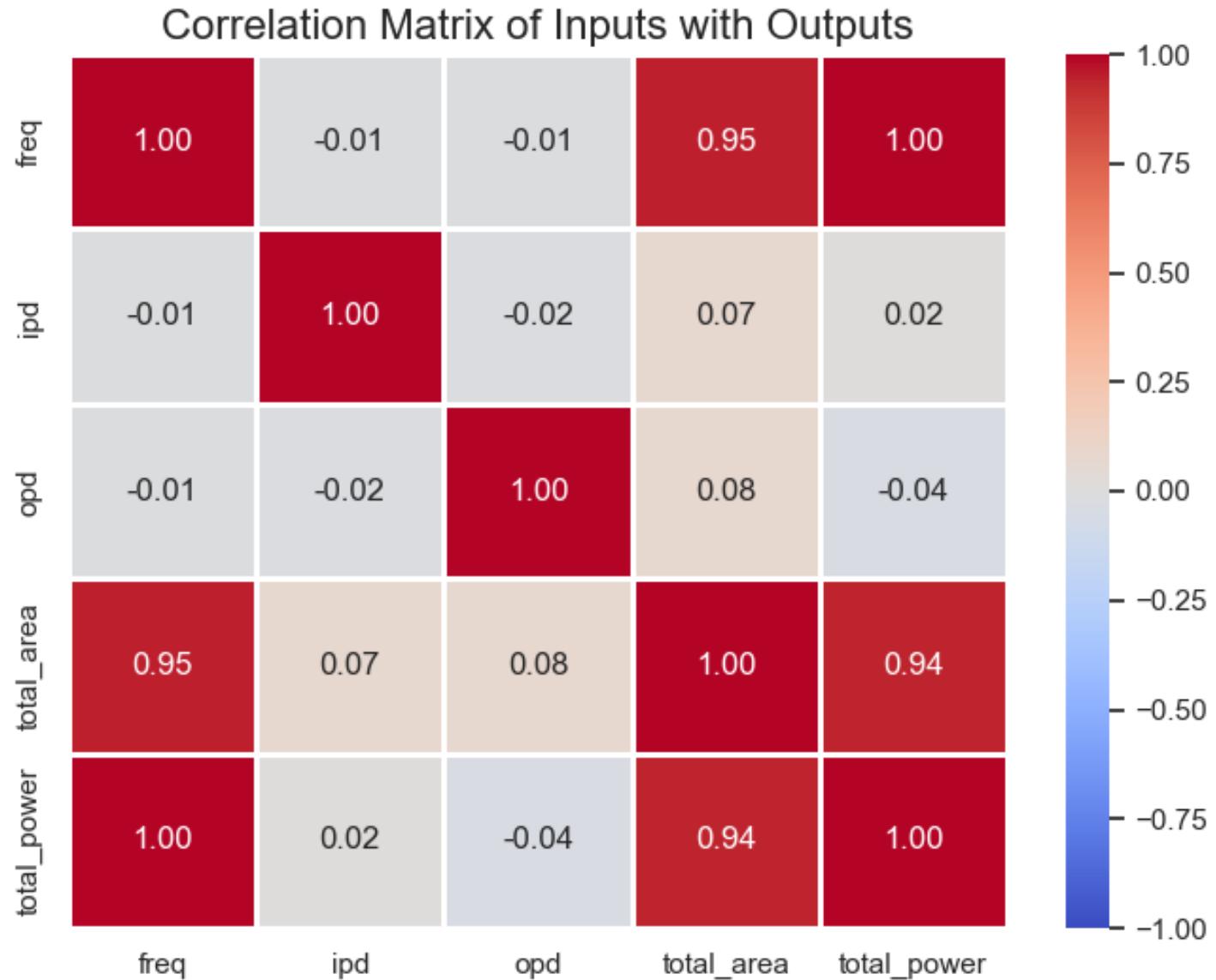
	2 Carry Unit Blocks	4 Carry Unit Blocks	8 Carry Unit Blocks
Power	5213 nW	5213 nW	1960 nW
Area	255	255	78
Slack Time	7004 ps	7004 ps	UNCONSTRAINED



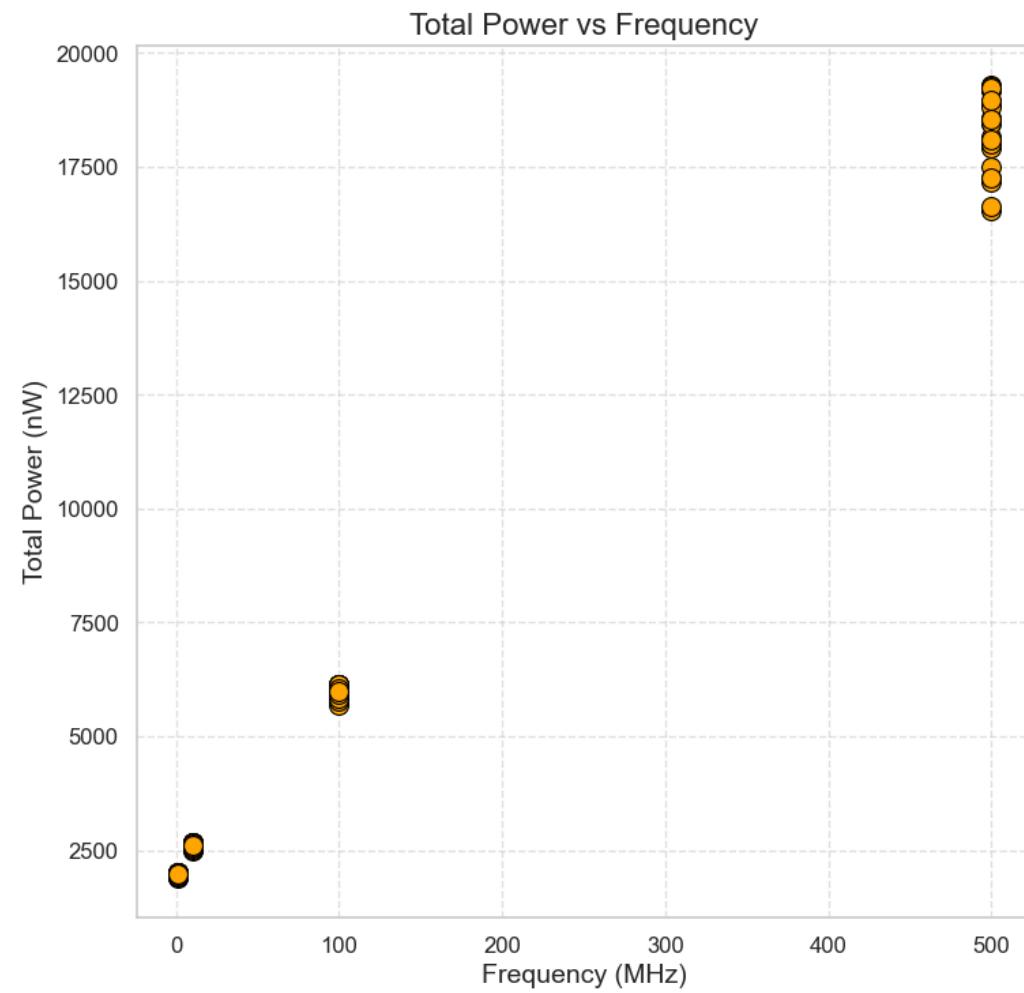
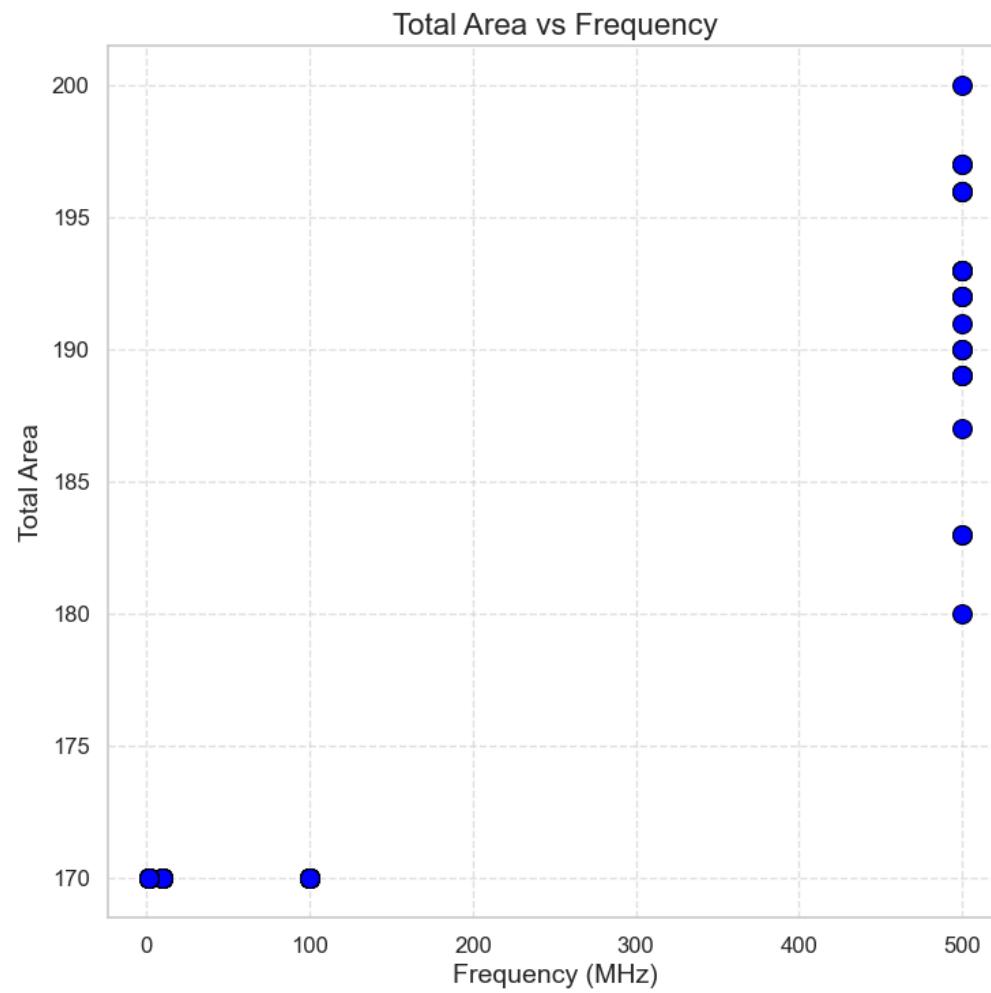
Genus Optimization:



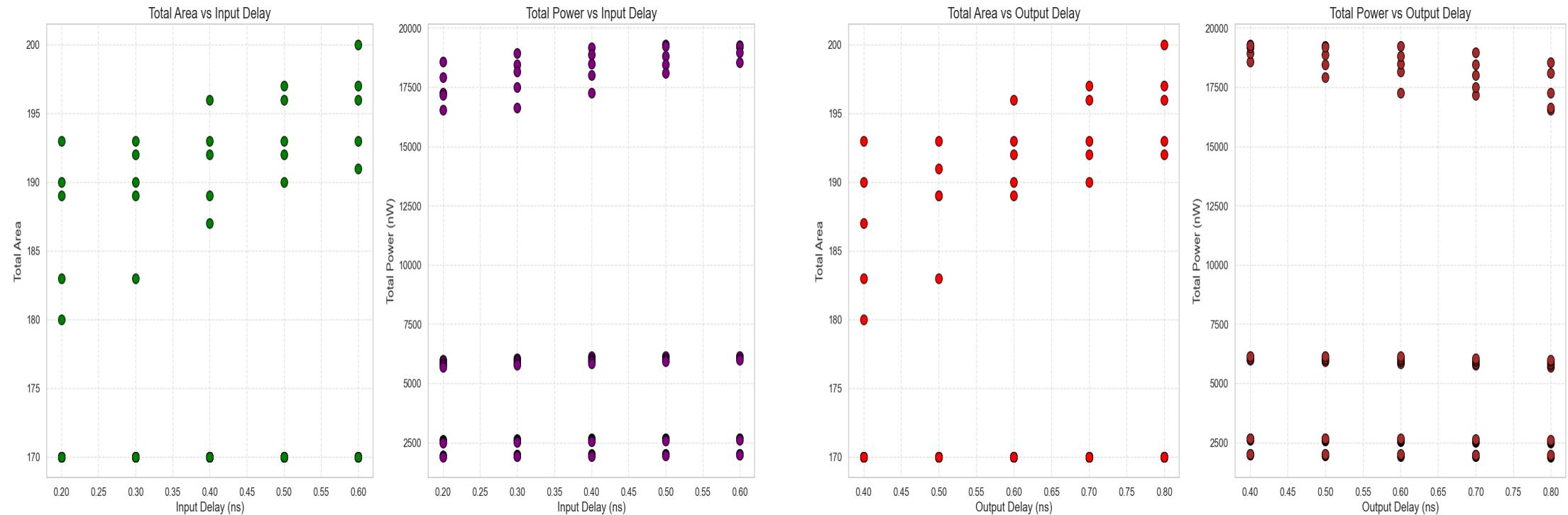
Genus Optimization:



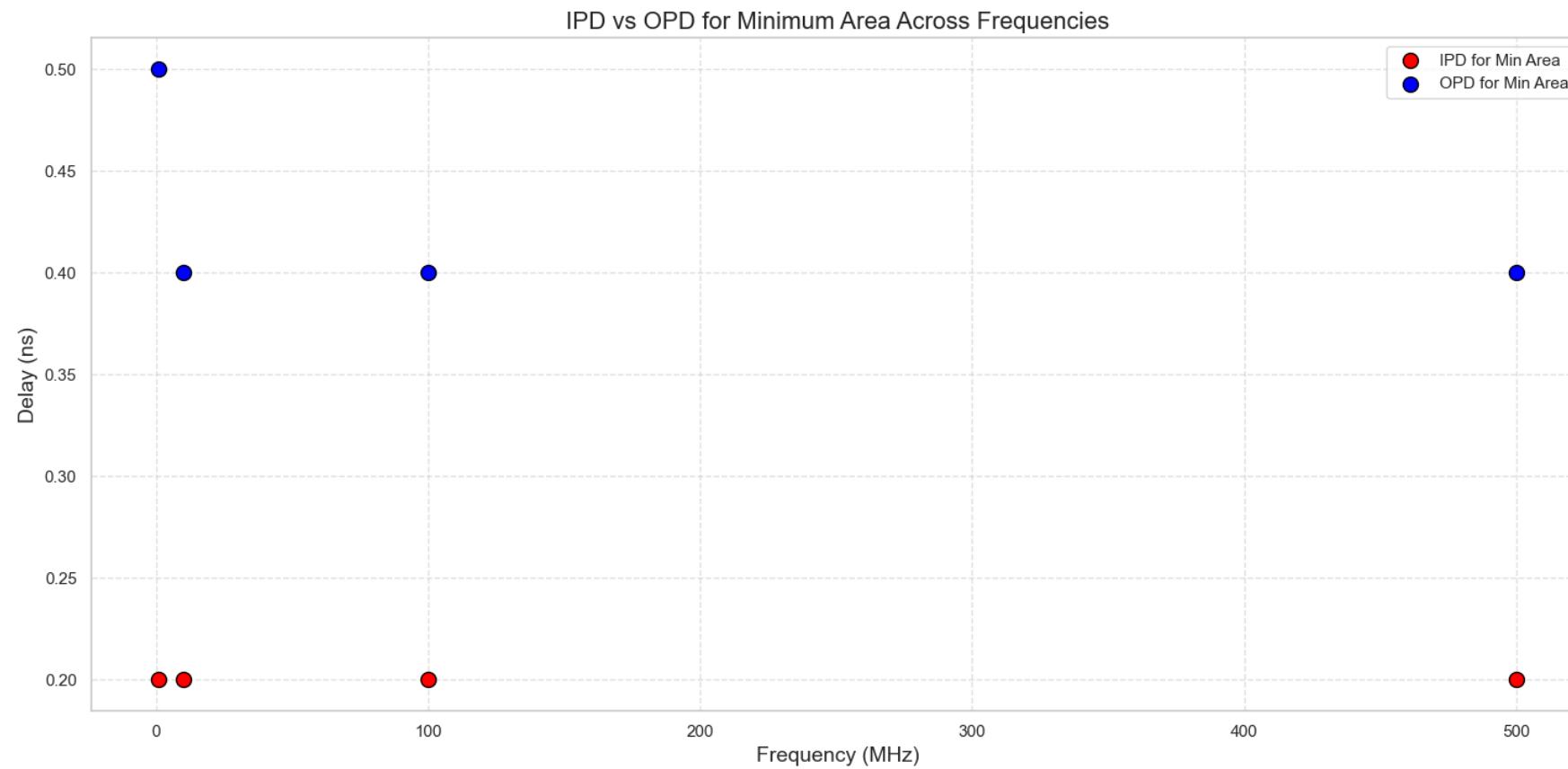
Genus Optimization:



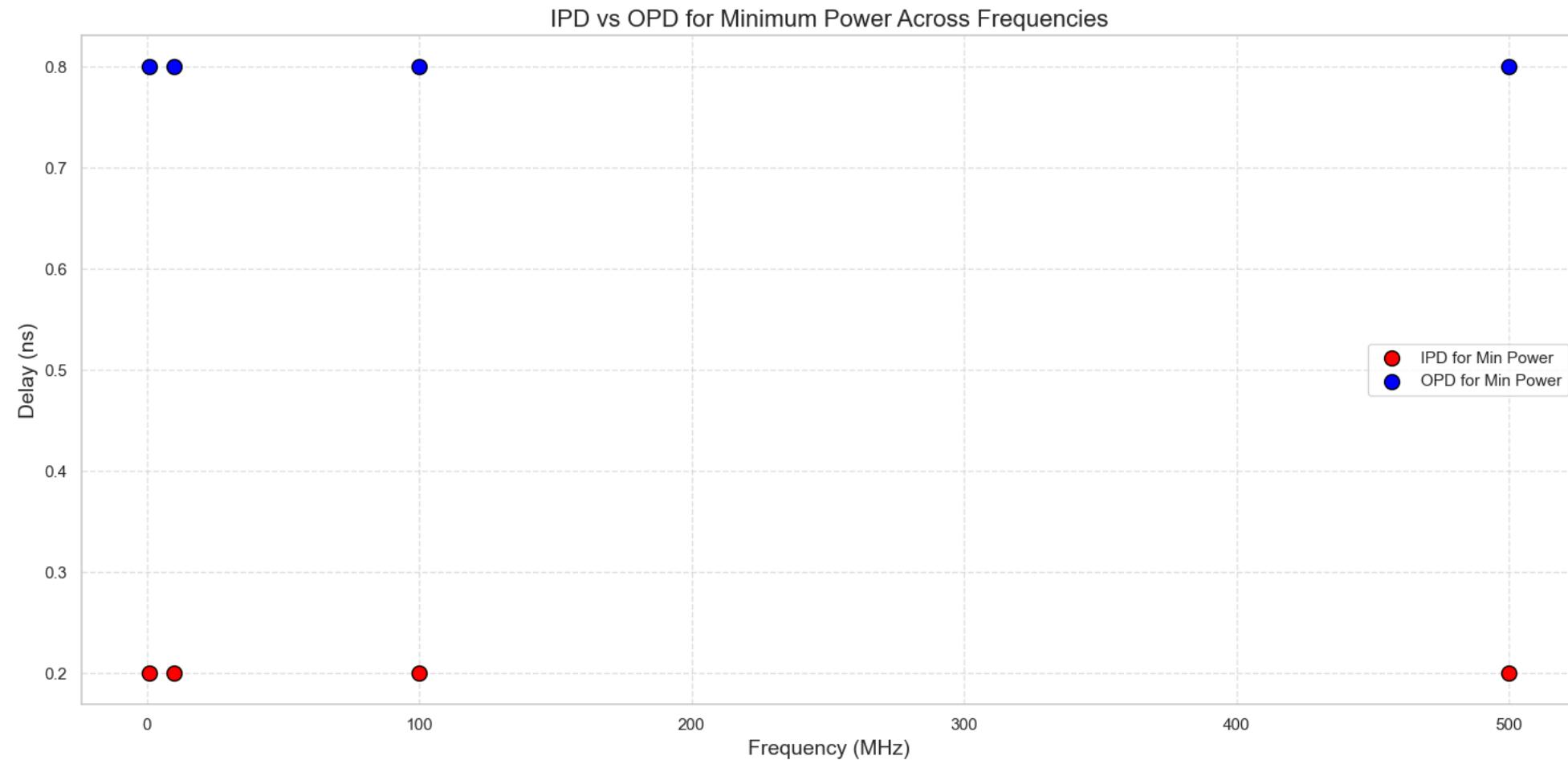
Genus Optimization:



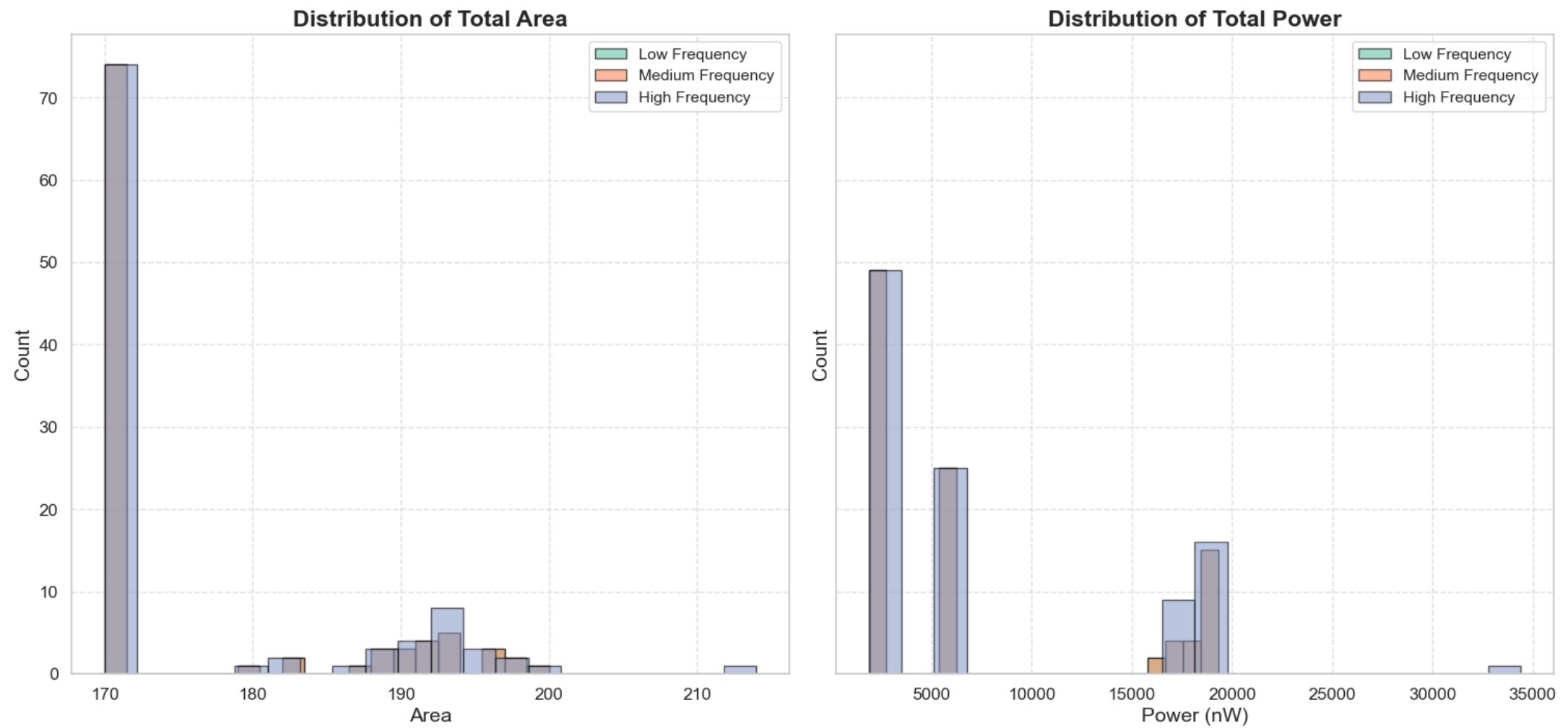
Genus Optimization:



Genus Optimization:



Genus Optimization:



Innovus Optimization:

The image shows two panels of the Innovus Optimization software interface.

Design Dimensions Panel (Left):

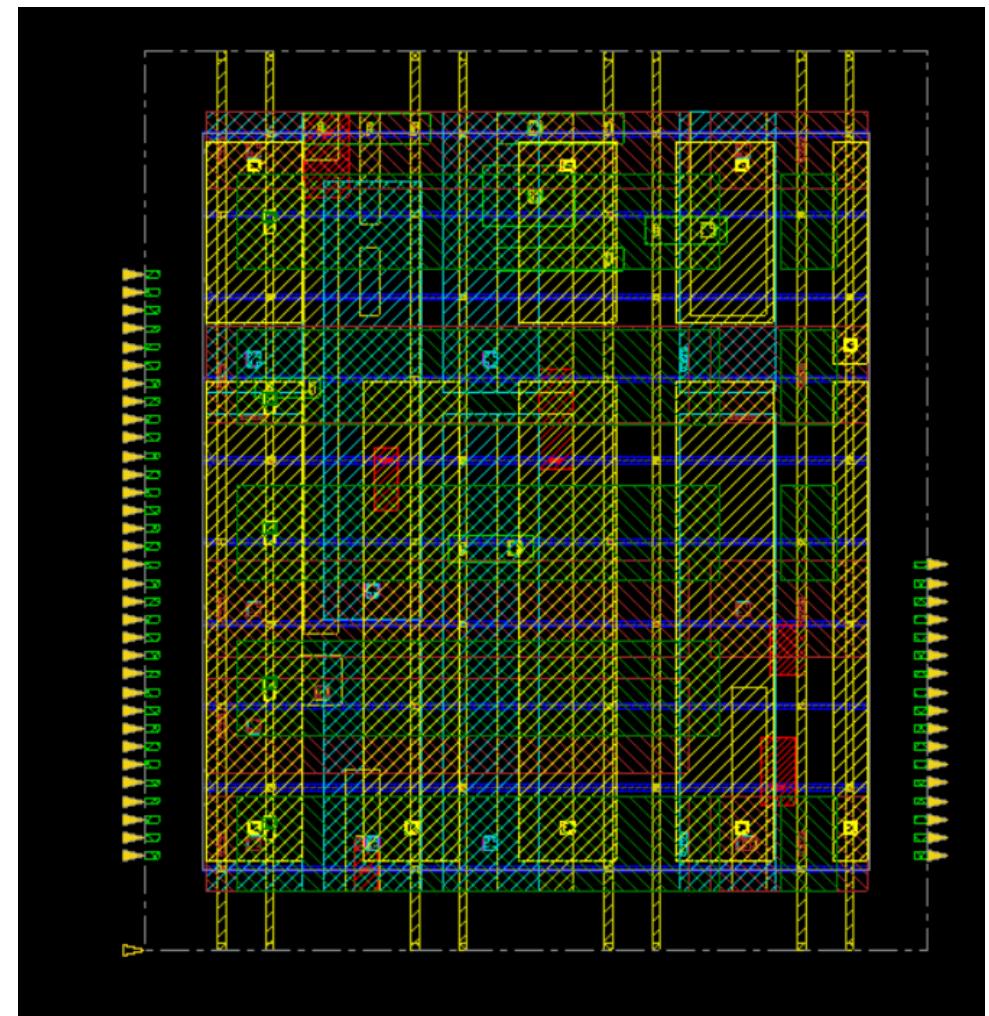
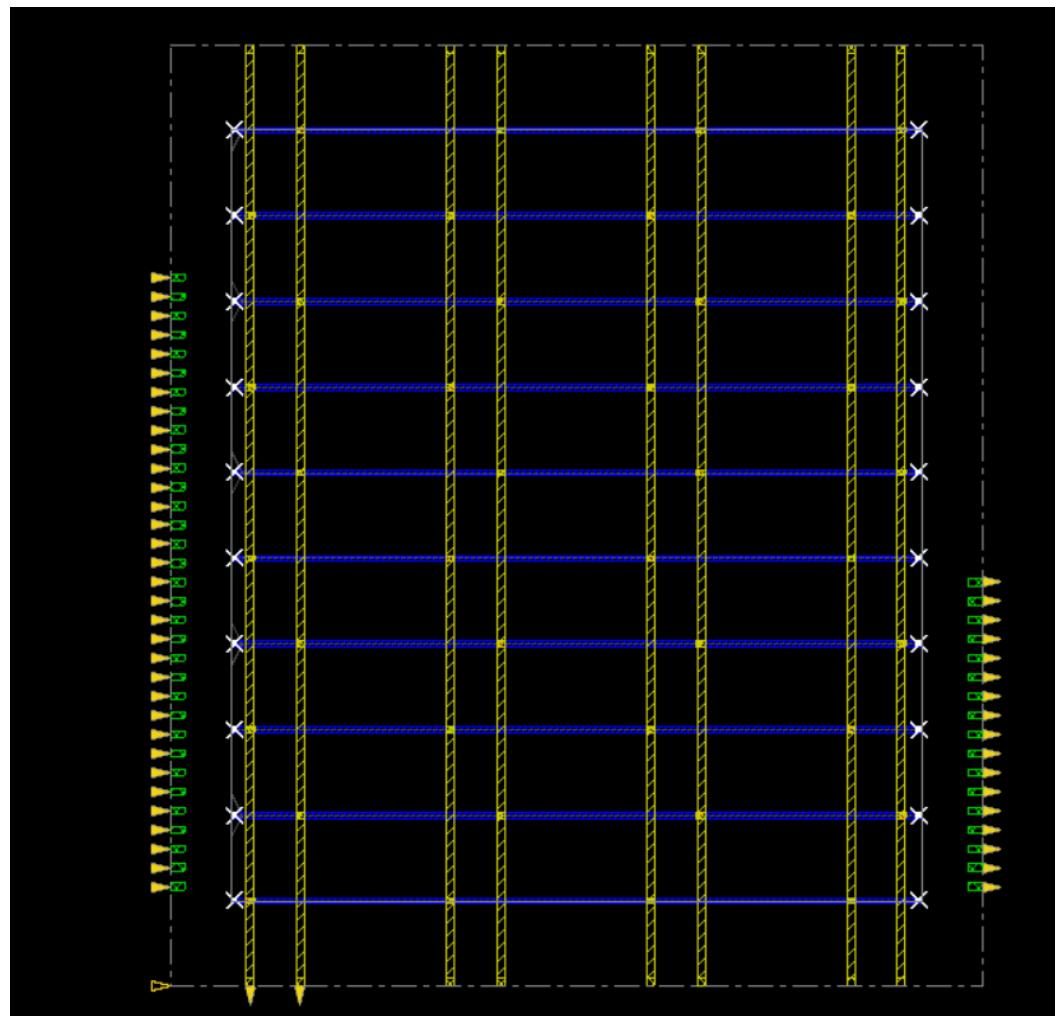
- Specify By:** Size Die/IO/Core Coordinates
- Core Size by:** Aspect Ratio Core Utilization Cell Utilization
- Ratio (H/W):** 1.2
Core Utilization: 0.8
Cell Utilization: 0.798712
- Dimension:** Width: 13.8, Height: 15.39, Width: 16.2, Height: 18.81
- Die Size by:** (disabled)
- Core Margins by:** Core to IO Boundary Core to Die Boundary
- Core to Left:** 1.2 **Core to Top:** 1.71
Core to Right: 1.2 **Core to Bottom:** 1.71
- IO Box Calculation Use:** Max IO Height Min IO Height
- Floorplan Origin at:** Lower Left Corner Center
- Unit:** Micron

Set Configuration Panel (Right):

- Basic** **Advanced** **Via Generation**
- Set Configuration:**
 - Net(s):** VDD VSS
 - Layer:** Metal4(4) **Direction:** Vertical Horizontal
 - Width:** 0.16 **Spacing:** 0.84
- Set Pattern:**
 - Set-to-set distance: 4
 - Number of sets: 1
 - Bumps
 - Over
 - Between
 - Over P/G pins
 - Pin layer:** Top pin layer
 - Max pin width: 0
 - Master name: []
 - Selected blocks
 - All blocks
- Stripe Boundary:**
 - Core ring
 - Pad ring Inner Outer
 - Design boundary Create pins
 - Each selected block/domain/fence
 - All domains
 - Specify rectangular area
 - Specify rectilinear area
- First/Last Stripe:**
 - Start from:** left right
 - Relative from core or selected area
 - X from left:** 0.3 **X from right:** 0
 - Absolute locations
- Option Set:** Edit Add Stripe Option



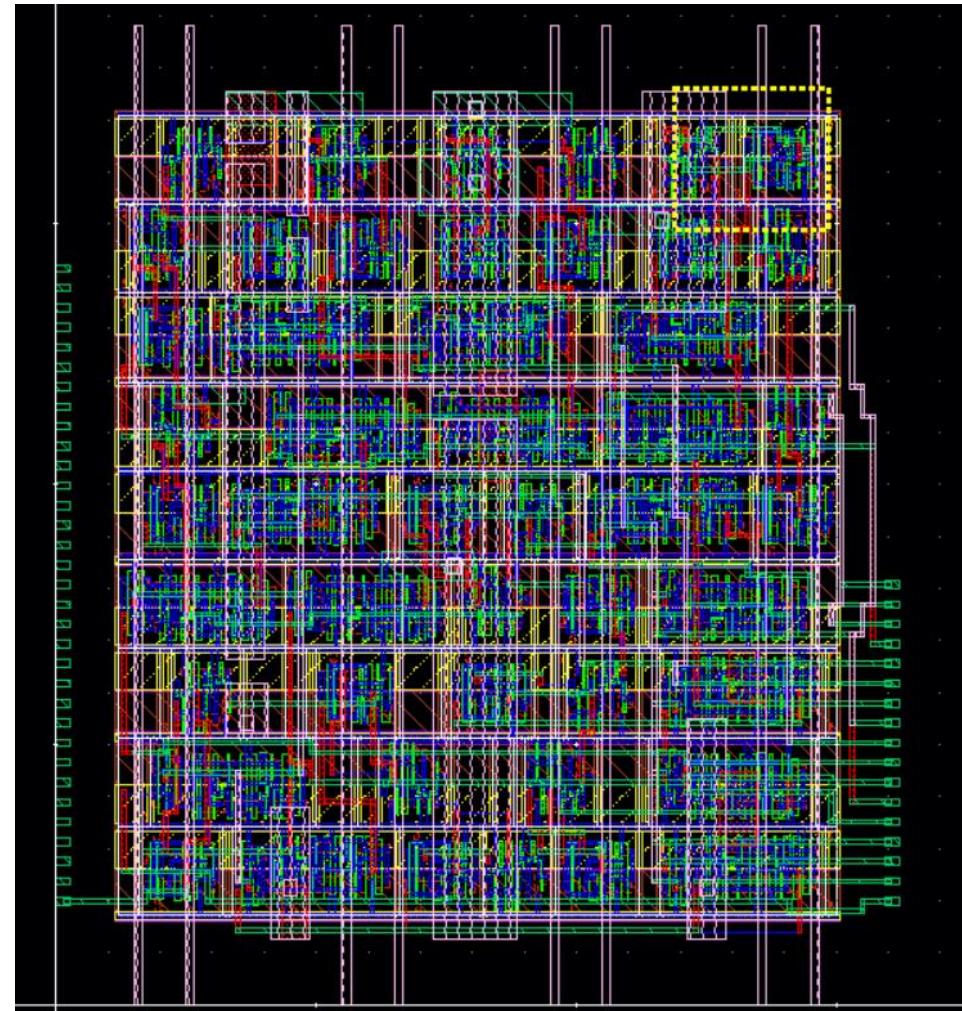
Innovus Optimization:



Innovus Optimization:

```
Total CPU Time          : 1(s)
Total Real Time         : 1(s)
Peak Memory Used        : 20(M)
Total Original Geometry : 828(6714)
Total DRC RuleChecks   : 562
Total DRC Results       : 0 (0)
Summary can be found in file cla_top.sum
ASCII report database is /home/vlsi37/CLA/Inno/cla_top.drc_errors.ascii
Checking in all Softshare licenses.
```

Design Rule Check Finished Normally. Sat Dec 7 15:35:28 2024



Innovus Optimization:

timeDesign Summary

Setup views included:
func@BC_rcbest0.hold

Setup mode	all	reg2reg	default
WNS (ns) :	8.477	N/A	8.477
TNS (ns) :	0.000	N/A	0.000
Violating Paths:	0	N/A	0
All Paths:	17	N/A	17

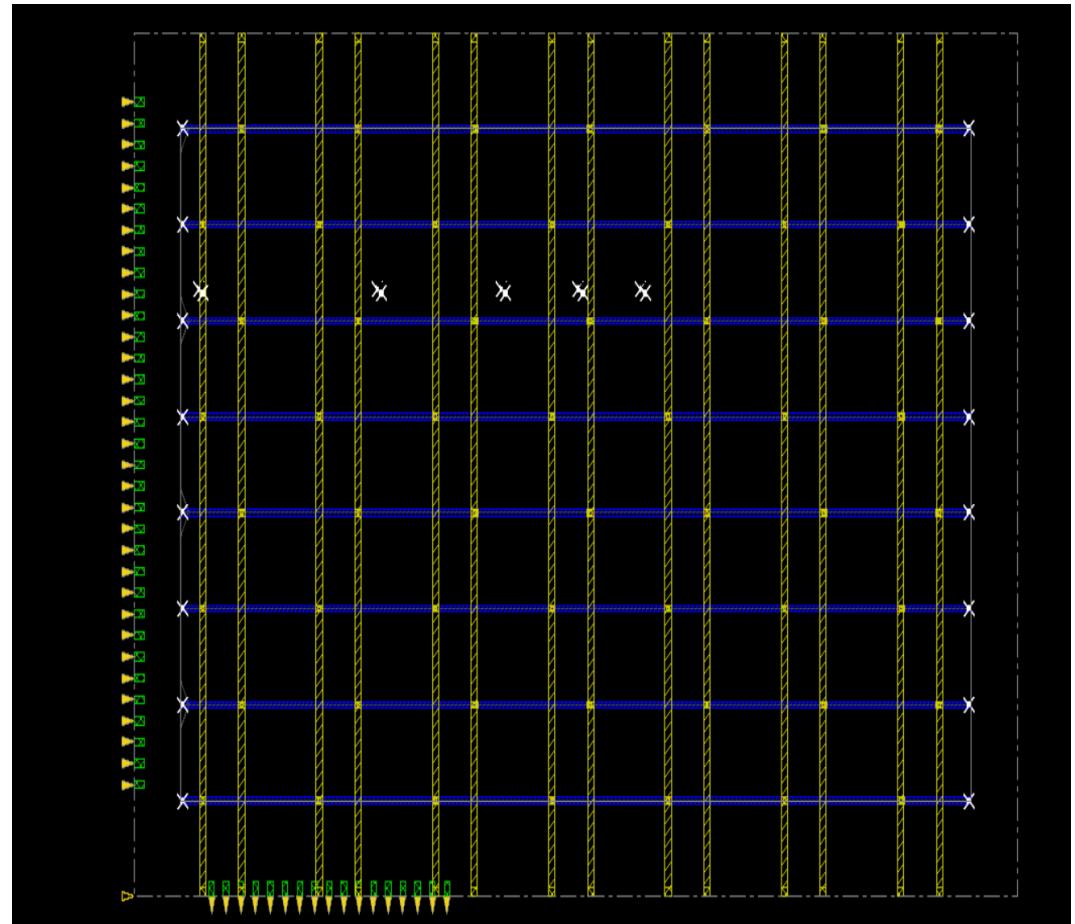
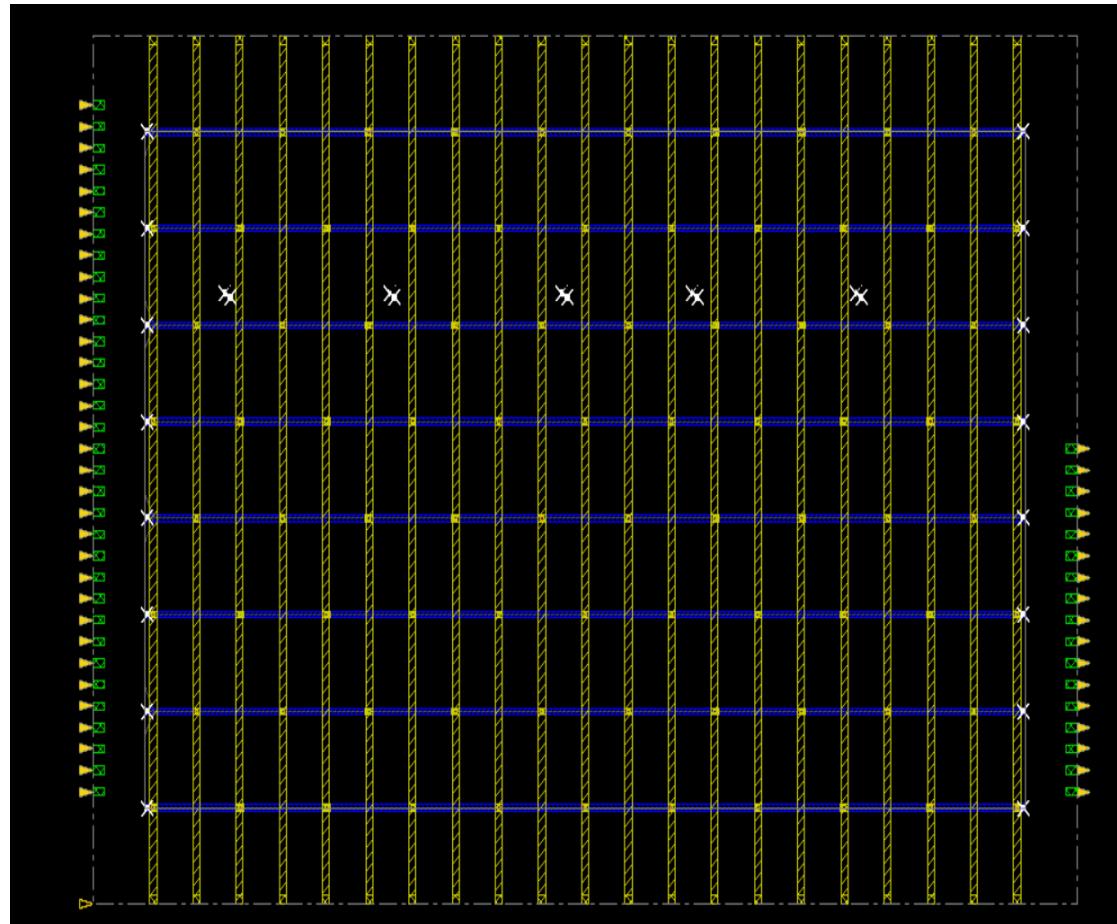
DRVs	Real		Total
	Nr nets(terms)	Worst Vio	Nr nets(terms)
max_cap	0 (0)	0.000	0 (0)
max_tran	0 (0)	0.000	0 (0)
max_fanout	0 (0)	0	0 (0)
max_length	0 (0)	0	0 (0)

Density: 79.871%

Routing Overflow: 0.00% H and 0.00% V



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Acknowledgement and References



References

Bibliography

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- [2] N. H. E. Weste and David Money Harris, *CMOS VLSI design : a circuits and systems perspective*. Noida: Pearson, 2015.
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- [4] "SystemVerilog TestBench," *ChipVerify*. <https://www.chipverify.com/systemverilog/systemverilog-simple-testbench>
- [5] P. Balasubramanian and D. L. Maskell, "A New Carry Look-Ahead Adder Architecture Optimized for Speed and Energy," *Electronics*, vol. 13, no. 18, pp. 3668–3668, Sep. 2024, doi: <https://doi.org/10.3390/electronics13183668>.



Thank You

Question and Answer Session

