BANGLADESH UNIVERSITY OF ENGINEERING AND TECHNOLOGY
DEPARTMENT ELECTRICAL AND ELECTRONIC ENGINEERING

EEE 304 – Digital Electronics Laboratory

Experiment 06

Introduction to SAP-1 (Simple as Possible) Computer

Evaluation Form:

IMPORTANT! You must complete this experiment during your scheduled lab period. All work for this experiment must be demonstrated to and verified by your lab instructor *before the end* of your scheduled lab period.

STEP	DESCRIPTION	MAX	SCORE
1	Identifying the basic timing states and dataflow of SAP-1	10	
2	Lab Tasks	10	
3	Report Tasks	10	
	TOTAL	30	

Signature of Evaluator: _____

Academic Honesty Statement

IMPORTANT! Please carefully read and sign the Academic Honesty Statement below. You will not receive credit for this lab experiment unless this statement is signed in the presence of your lab instructor.

"In signing this statement, I hereby certify that the work on this experiment is my own and that I have not copied the work of any other student (past or present) while completing this experiment. I understand that if I fail to honor this agreement, I will receive a score of ZERO for this experiment and be subject to possible disciplinary action."

Last Name (Printed): Choudhury **Lab Group:** B1 **Date:** 12/09/23

E-mail: 1906081@eee.buet.ac.bd **Signature:** Anin dya

Control Signal:

Control Signal	Description
CP ([controller12])	Enable Increment for PC
EP ([controller11])	Enable Output for PC
LM’ ([controller10])	Enable Load for MAR
CE’ ([controller9])	Enable Output for RAM
LI’ ([controller8])	Enable Load for IR
EI’ ([controller7])	Enable Output for ID
LA’ ([controller6])	Enable Load for Accumulator (Reg A)
EA ([controller5])	Enable Output for Accumulator (Reg A)
SU ([controller4])	Enable Subtraction operation for ALU
EU ([controller3])	Enable output for ALU
LB’ ([controller2])	Enable output for Reg B
LO’ ([controller1])	Enable load for Output Reg

Verilog Code:

```
module
sapcontroller(clock,reset,operation_code,controller);
    input [4:1] operation_code;
    input clock, reset;
    output reg [12:1] controller;
    reg [4:1]y;
    reg [4:1]Y;
    parameter [3:0] LDA= 4'b0000,ADD= 4'b0001, SUB=
4'b010, OUT= 4'b1110, HLT = 4'b1111;
    parameter [3:0] t1=1,t2=2,t3=3,t4=4,t5=5,t6=6;

    always@(operation_code,y)
    begin
        case(y)

        t1: begin
        controller=12'b010111100011;
        Y=t2;
        end

        t2: begin
        controller=12'b101111100011;
        Y=t3;
        end
```

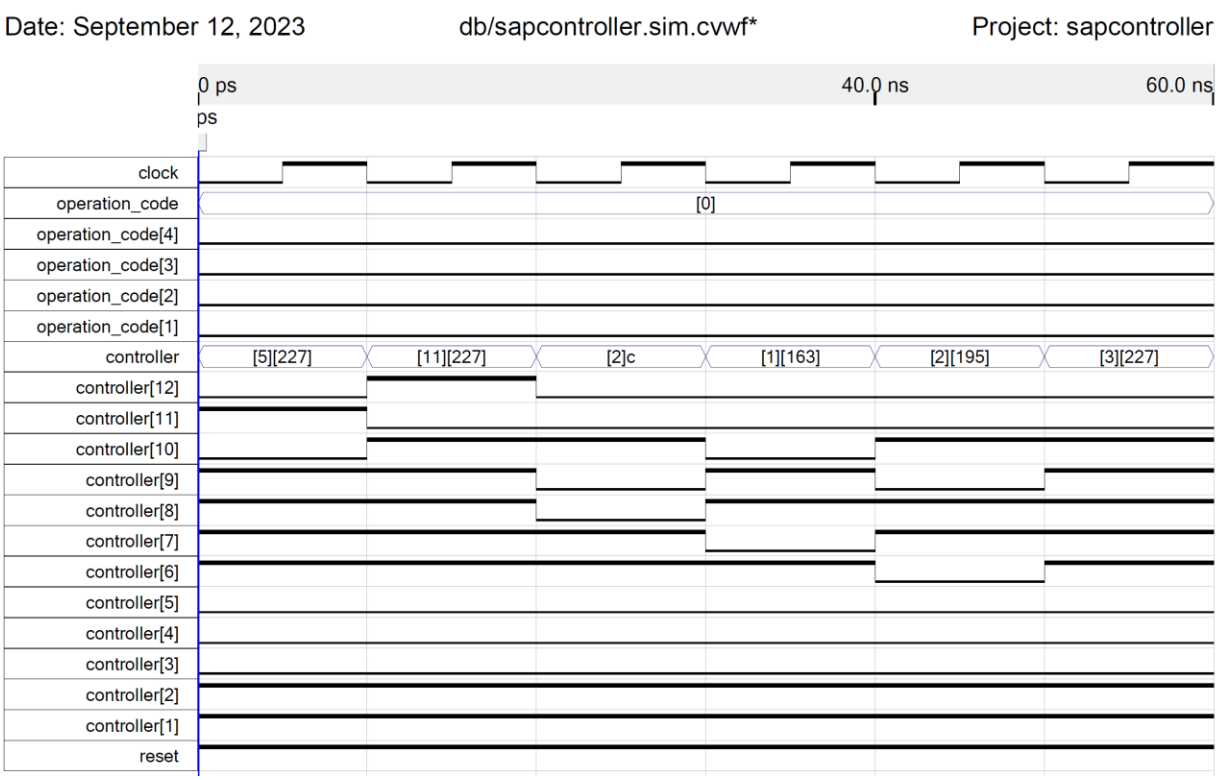
```
    t3: begin
    controller=12'b001001100011;
    if (operation_code==HLT)
        Y=t3;
    else
        Y=t4;
    end

    t4: begin
        case(operation_code)

            LDA: controller=12'b000110100011;
            ADD: controller=12'b000110100011;
            SUB: controller=12'b000110100011;
            OUT: controller=12'b001111110010;

        endcase
    Y=t5;
    end

t5: begin
    case(operation_code)

        LDA: controller=12'b001011000011;
        ADD: controller=12'b001011100001;
        SUB: controller=12'b001011100001;
```

```
        OUT: controller=12'b001111100011;

    endcase
Y=t6;
end

t6: begin
    case(operation_code)

        LDA: controller=12'b001111100011;
        ADD: controller=12'b001111000111;
        SUB: controller=12'b001111000111;
        OUT: controller=12'b001111000111;

    endcase
Y=t1;
end

default: Y=t1;
endcase
end

always @ (negedge clock or negedge reset)
begin
    if(reset==0) y<=t1;
    else y<=Y;
```

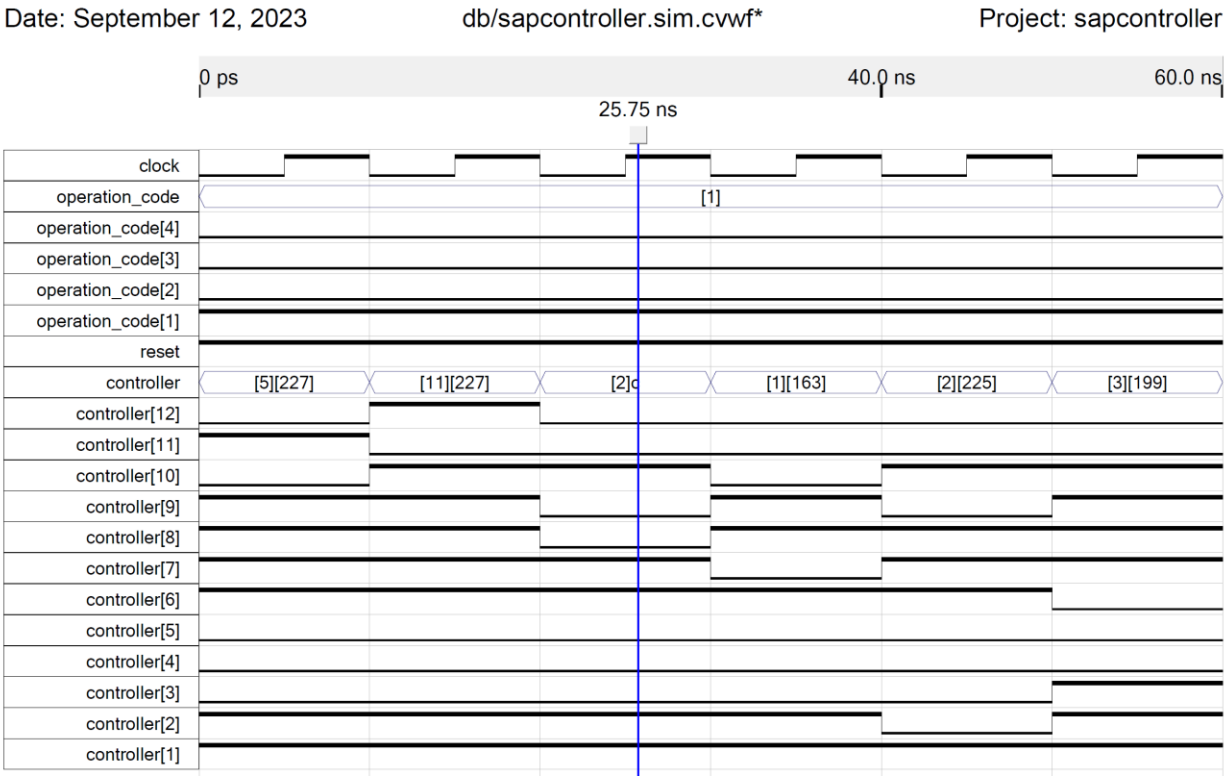
```
    end

endmodule
```

Outputs:

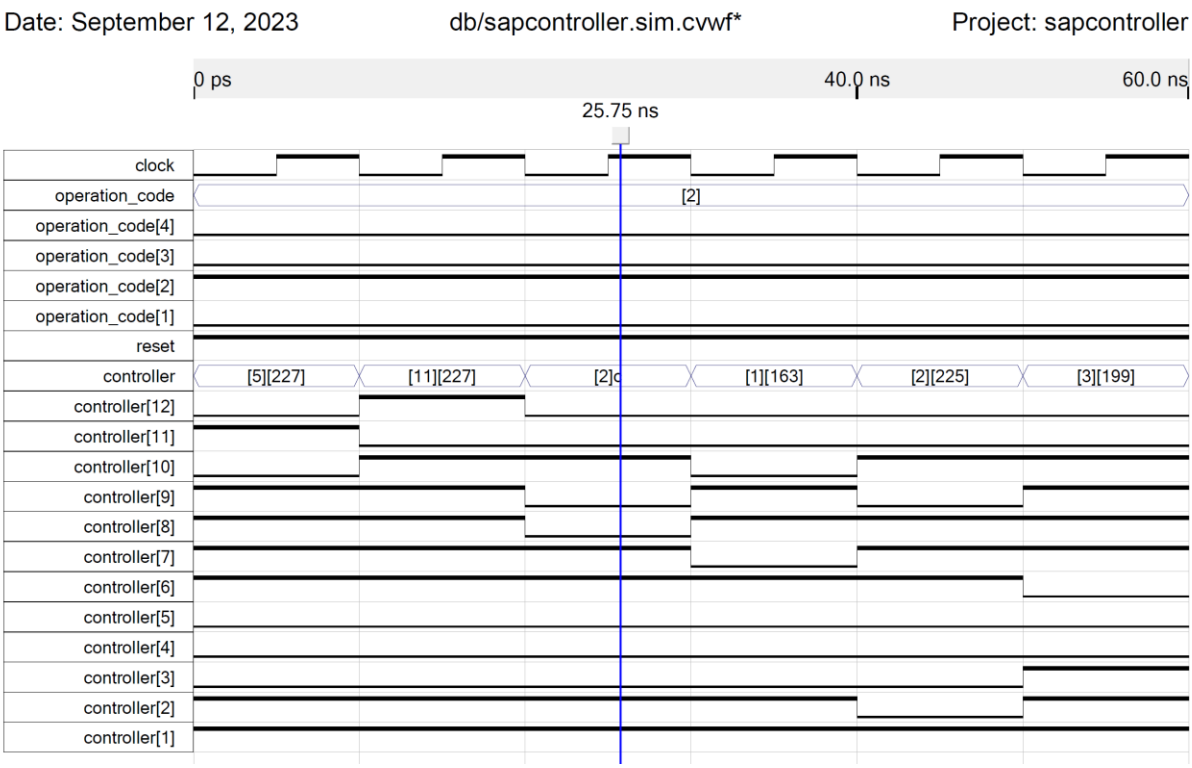
For Load Operation:



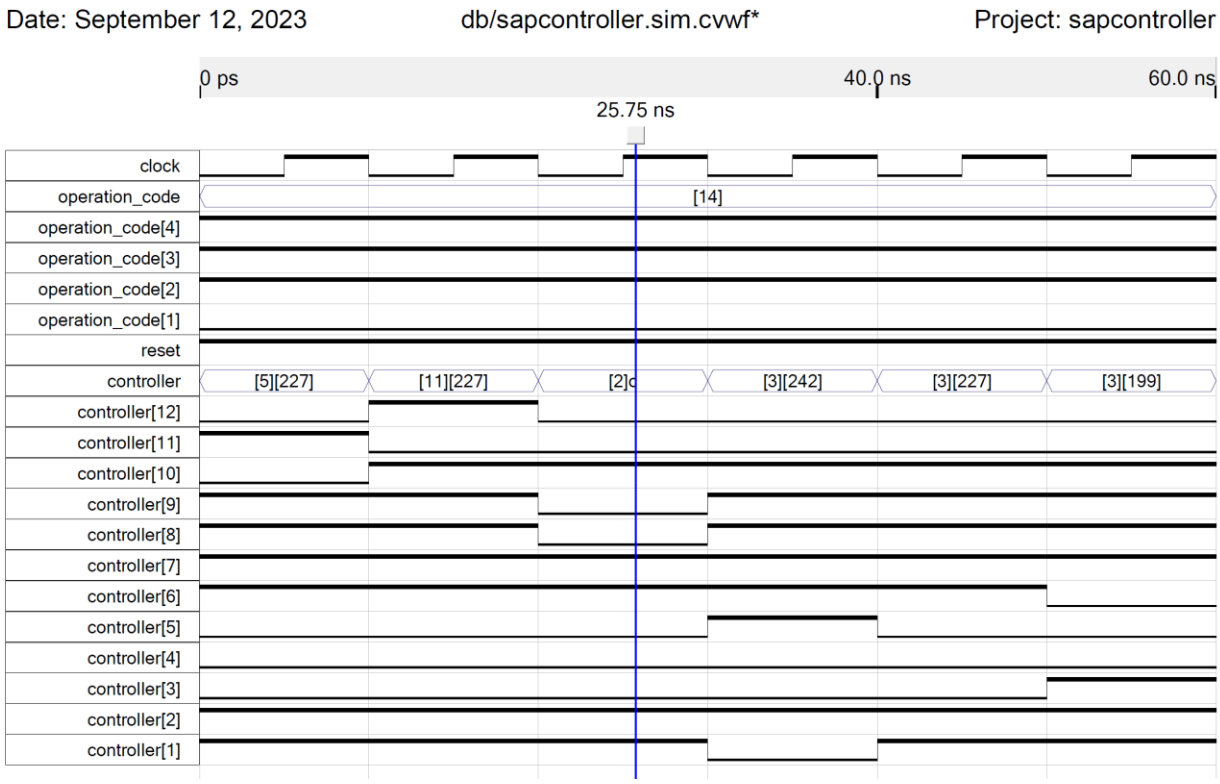
For ADD Operation:



For Sub operation:



For Out Operation:



For HLT Operation:

Date: September 12, 2023 db/sapcontroller.sim.cvwf* Project: sapcontroller