# Fall 2021 Computer Architecture

## Homework Assignment 4 **Due dates: Dec. 23**

**Problem 1.** This problem examines the accuracy of various branch predictors for the following repeating pattern (e.g., in a loop) of branch outcomes: NT, NT, T, NT, NT, T, T, T (Note: T represents Taken, and NT represents Not Taken). Assume the loop has n iterations, where n is a very large number (n ➔ ∞).

**(a)** Suppose we have a static branch predictor that predicts either always-taken or always-not-taken, what would be the accuracy of branch prediction in the two cases (i.e., the percentage of correct predictions in all predictions)?

**(b)** Suppose we have a 1-bit dynamic branch predictor, what would be the accuracy of branch prediction? If you think the answer may depend on the initial state of the branch predictor, please discuss all possibilities.

**(c)** Suppose we have a 2-bit dynamic branch predictor, what would be the accuracy of branch prediction? If you think the answer may depend on the initial state of the branch predictor, please discuss all possibilities.

**Problem 2.** Consider the following loop:

```
For I = 0 to 29
        C[i] = (A[i] + B[i]) / 2
```

**(a)** For the following scalar codes, how many dynamic instructions do we need? How many clock cycles are needed for 1-memory bank and 10-memory bank setting, respectively?

| | |
|---|---|
| MOVI R0 = 30 | 1 cycle |
| MOVA R1 = A | 1 cycle |
| MOVA R2 = B | 1 cycle |
| MOVA R3 = C | 1 cycle |
| X: LD R4 = MEM[R1++] | 8 cycles ; #autoincrement addressing |
| LD R5 = MEM[R2++] | 8 cycles |
| ADD R6 = R4 + R5 | 4 cycles |
| SHFR R7 = R6 >> 1 | 1 cycle |
| ST MEM[R3++] = R7 | 8 cycles |
| DECBNZ R0, X | 2 cycles # decrement and branch if NZ |

**b)** For the following vectorized codes, how many dynamic instructions do we need? How many clock cycles are needed for 10-memory bank setting?

| | |
|---|---|
| MOVI VLEN = 30 | 1 cycle |
| MOVI VSTR = 1 | 1 cycle |
| VLD V0 = A | 8 + VLEN – 1 cycles |
| VLD V1 = B | 8 + VLEN – 1 cycles |
| VADD V2 = V0 + V1 | 4 + VLEN – 1 cycles |
| VSHFR V3 = V2 >> 1 | 1 + VLEN – 1 cycles |
| VST C = V3 | 8 + VLEN – 1 cycles |