NATIONAL INSTITUTE OF TECHNOLOGY KARNATAKA

EC383 VLSI MINI PROJECT

EVALUATION 1 REPORT

MENTOR : MRS KALPANA BHAT

MENTEES : SHRIDEVI KUMAR 191EC150
KAVEEN SRIKANTHAN 191EC215
ANIRRVHINYAN K 191EC205

Introduction:

This report consists of our first progress towards 8-bit DAC using the R-2R Ladder method.

Objective:

We aim to build the Digital to Analog Convertor by first designing it and implementing it on LTSpice and later simulating it on Proteus software.

Methodology/Work done:

How a DAC works?

Lets take 3 – bit DAC and Inputs as $D_2\, D_1\, D_0$

For example

$D_2\, D_1\, D_0 = 001$

At D_0 = Vref = 10 V

Vth $= [\frac{2R}{2R+2R}]$ Vref = $\mathbf{\frac{Vref}{2}}$

Rth = R

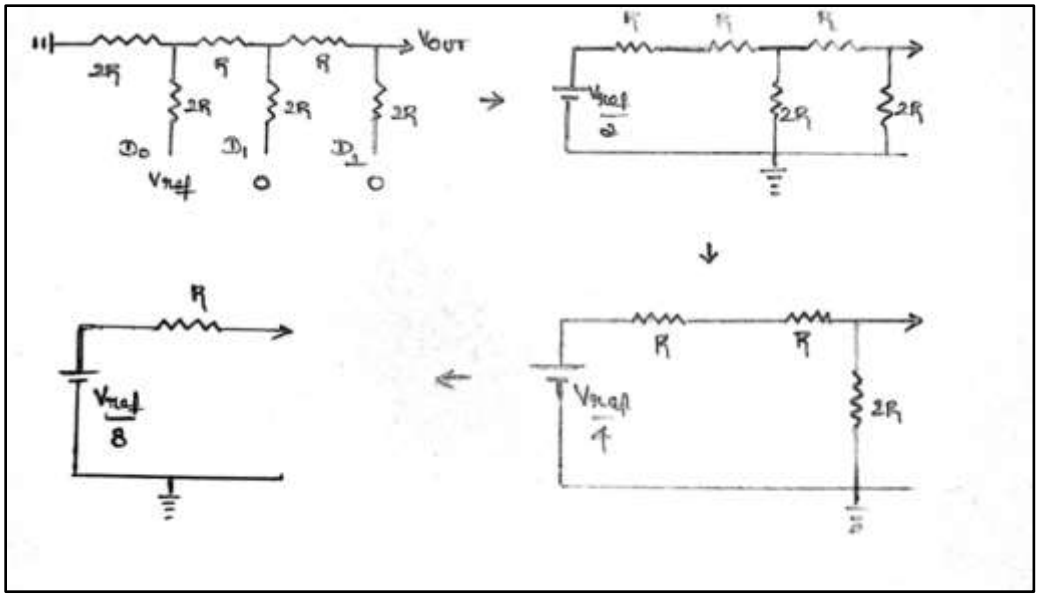
Again for resullt circuit Vth = $\mathbf{\frac{\frac{Vref}{2}}{2} = \frac{Vref}{4}}$

Rth remains R

In the final circuit Vth = $\mathbf{\frac{\frac{Vref}{4}}{2} = \frac{Vref}{8}}$ and Rth is R

Vout = $\mathbf{\frac{Vref}{8}}$

Circuital representation:



This technique is followed for all values which gives **Vout = Vref** $\mathbf{[\frac{D2}{2} + \frac{D1}{4} + \frac{D0}{8}]}$

Similarly for 8 bit DAC:

The Vout calculation depending on Input:
Lets consider all Inputs ie. V_0, V_1, V_2 …. $V_7 = 0$
Then Node A = Node B = ….. = Node G = Vout = 0V as all are connected to ground

If all inputs are 10 V, we get Vout as 10V because all nodes are in 10V
All values from 0 – 255 will have values output between 0 – 10V

The equation of Vout for different binary inputs is:

$$\textbf{Vout = Vref } \left[\frac{D7}{2} + \frac{D6}{4} + \frac{D5}{8} + \frac{D4}{16} + \frac{D3}{32} + \frac{D2}{64} + \frac{D1}{128} + \frac{D0}{256}\right]$$

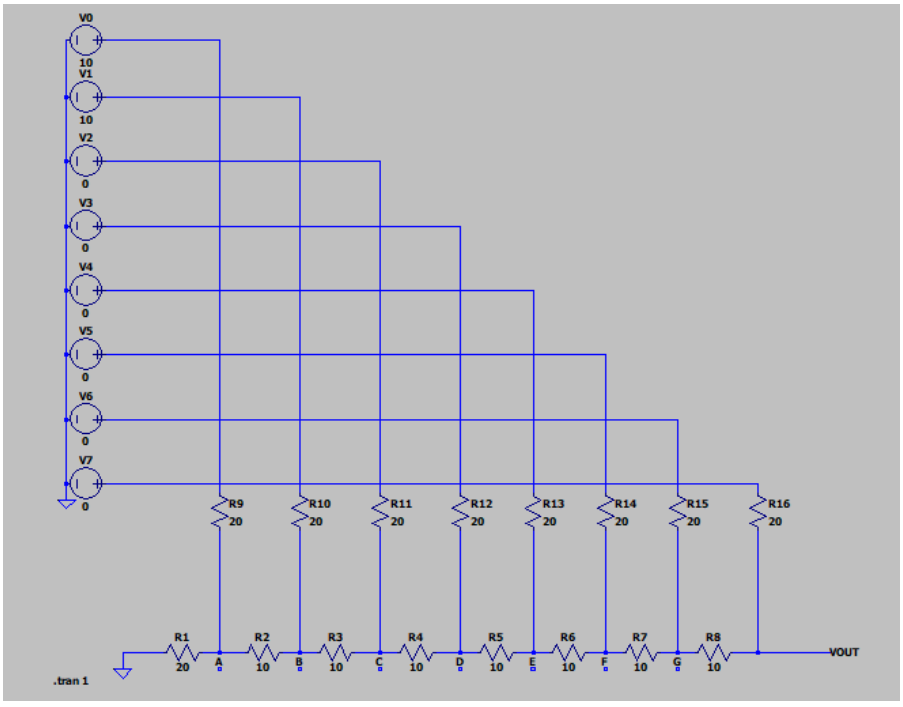
Here V_0, V_1, V_2 …. V_7 are 0 if 0V and 1 if 10V.

Example:
If $V_0 = V_1$ = High are rest are Low

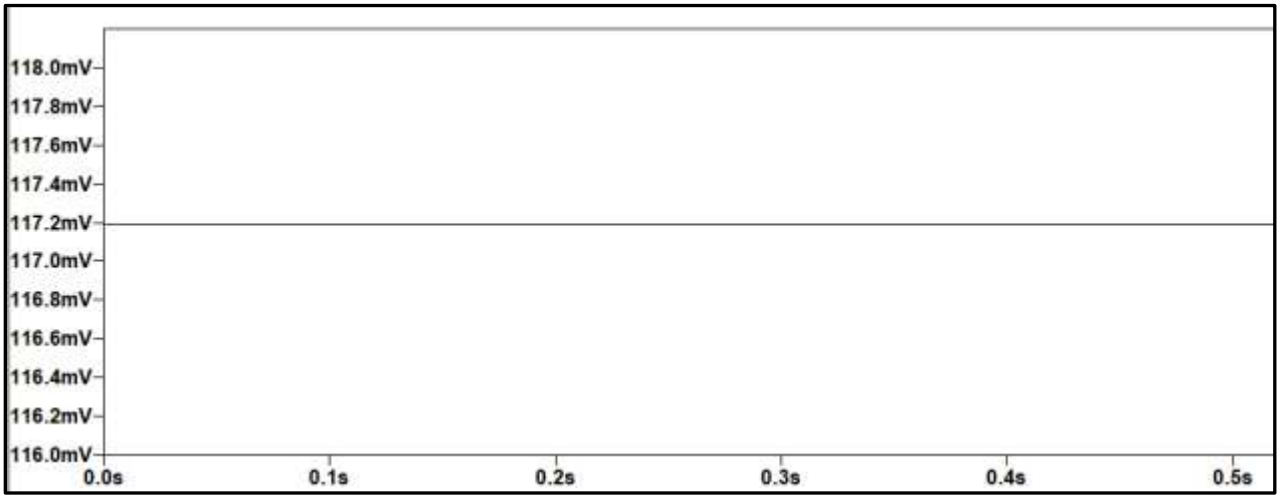
$$\textbf{Vout = 10 } \left[\frac{1}{128} + \frac{1}{256}\right] \textbf{ = 0.1172 V}$$

Simulation in LT Spice:

Circuit:



Output:



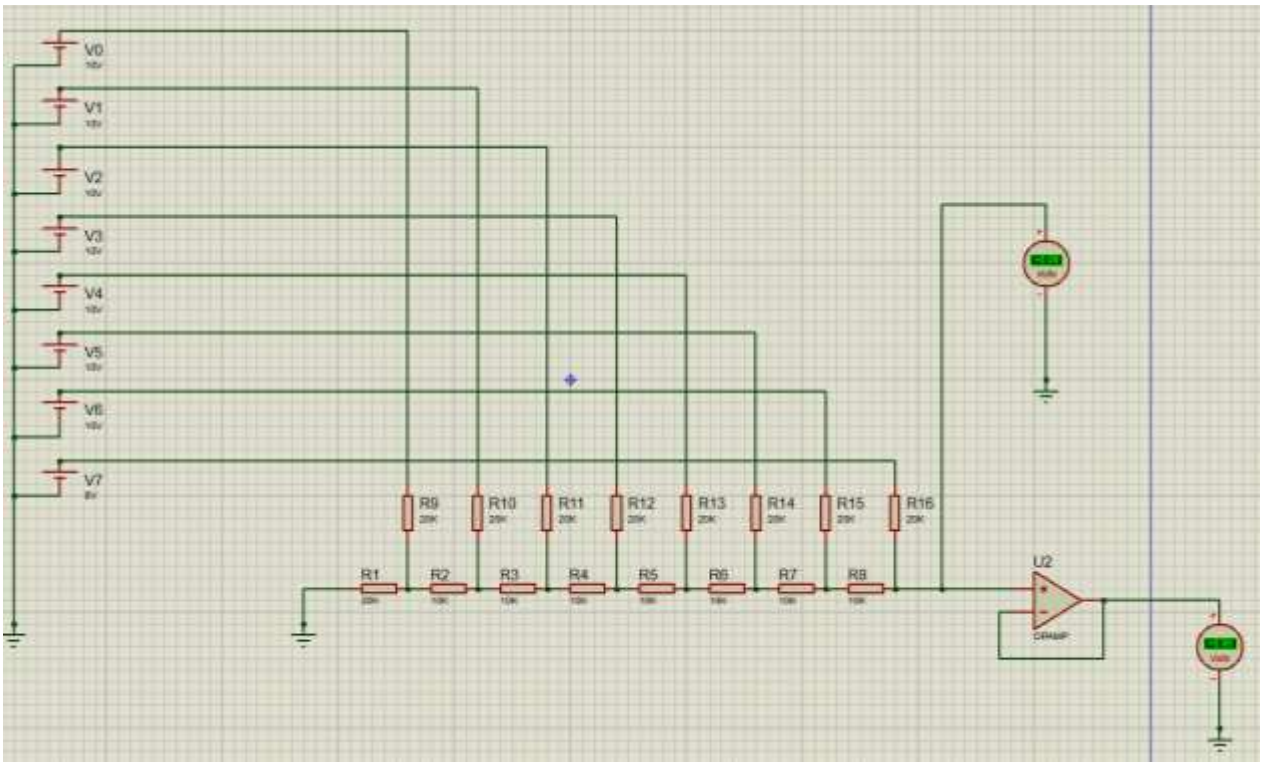
Vout = 117.2 mV

- Now that this is a resistor network, if we apply any load on the output of the first stage, this load will be considered as an additional resistor in the network, and thus will disturb the network which will no longer provide the correct & desired output voltage.
- Therefore, to overcome this problem, we need a voltage buffer, here is where the next stage comes.

Simulation in Proteus

Circuit:

Output is also shown in DC Voltmeter



With voltage buffer:

This stage will isolate the point V1 from the final output V2, while always keeping the voltage V2 at the exact same value as V1. This is what we call a voltage buffer. For the voltage buffer, we use an opamp with the output connected to the inverting input (this special configuration of the Op Amp is also called Voltage Follower). The most important things to note are:

1. No current (almost 0A) will flow from the point V1 into the OpAmp, so we won't be disturbing the resistor network configuration.
2. V2 will always equal V1 (theoretically, as shown in the rest of this document).
3. The current going out from the point V2 to any other stage is sourced from the power supply of the OpAmp.

Conclusion

The first phase of our project has been completed successfully. We were able to develop the right circuit model both on LTSpice and Proteus. Results were obtained as expected and hence phase 1 of our project has been simulated successfully.

Future Work

We are currently in the process of designing our own opamp which will be added to the end of the circuit. We will also be simulating our circuit using an ideal and practical Opamp. Further, depending on the output values of our circuit we will be designing an application using the DAC.

References

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