EC302 VLSI DESIGN LAB

PROJECT REPORT

1. 4 BIT ADDER
2. 2×2 MULTIPLIER
3. 2×4 DECODER

DOCUMENTED BY:

KAVEEN SRIKANTHAN	191EC215
ANIRRVHINYAN K	191EC205
SHRIDEVI KUMAR	191EC150

UNDER THE SUPERVISION OF
DR . RAMESH KINI

TABLE OF CONTENTS

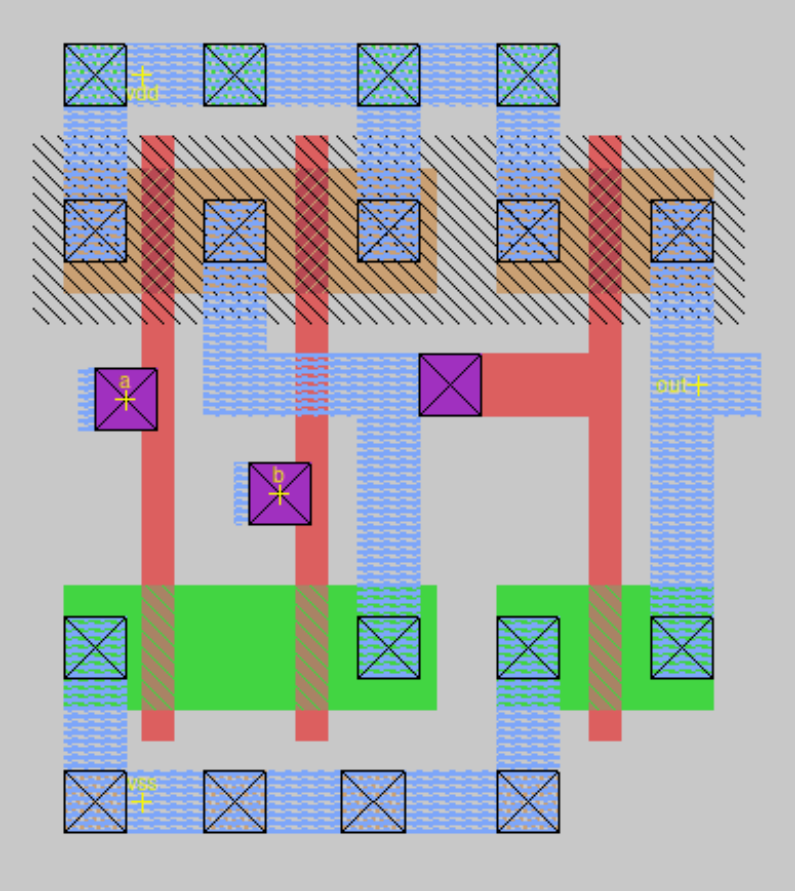
GATES USED IN THIS PROJECT

1. **AND Gate**

A two input gate that is high when both of its inputs are high.

A	B	Output
0	0	0
0	1	0
1	0	0
1	1	1

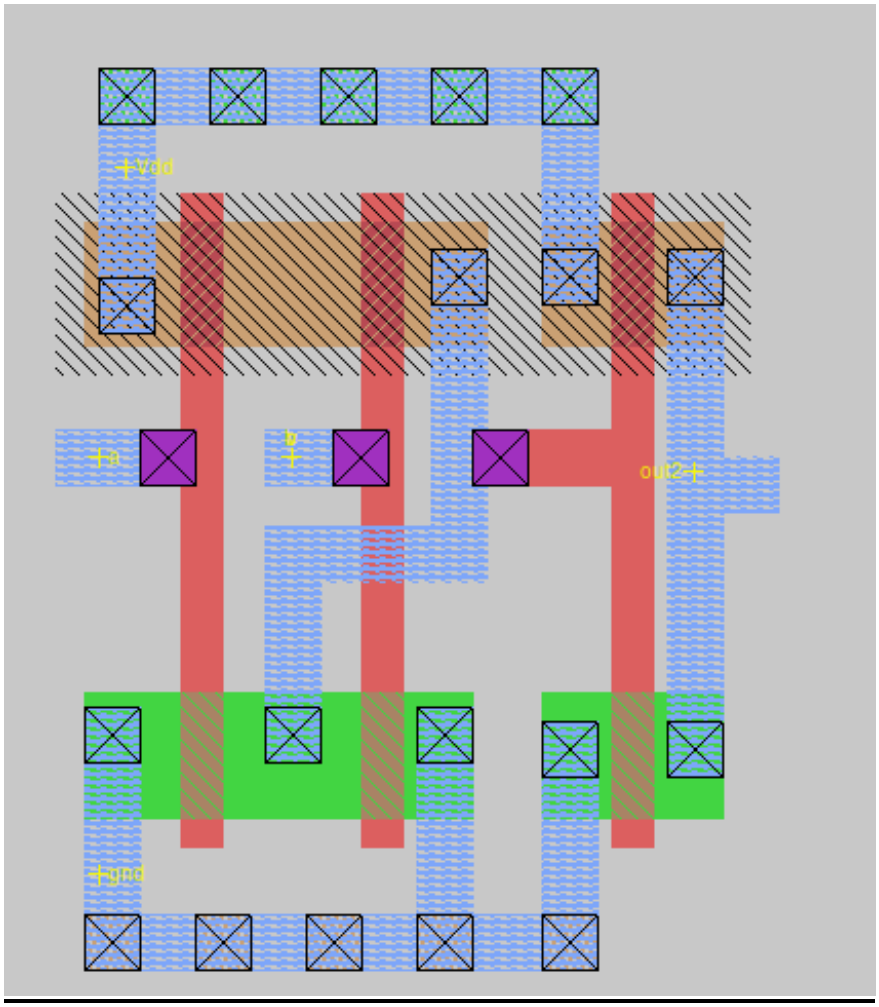
Table 1: AND gate Truth Table



2.**OR Gate-**

A two input gate that is high when any of its inputs are high.

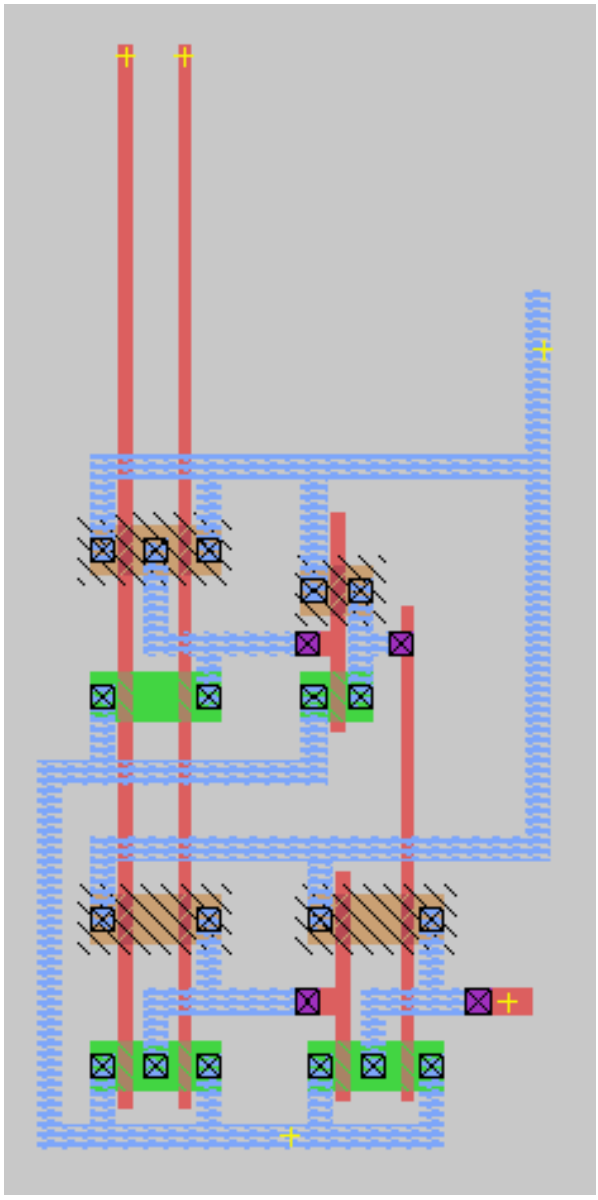
A	B	Output
0	0	0
0	1	1
1	0	1
1	1	1



3.XOR Gate

A two-input gate that is high when any either one of its inputs is high.

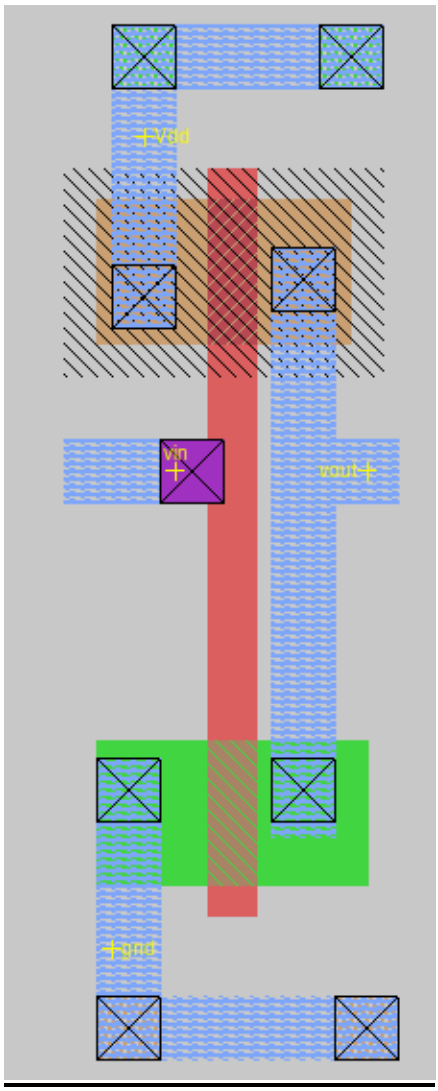
A	B	Output
0	0	0
0	1	1
1	0	1
1	1	0



4.**NOT Gate-**

The value of the input is inverted at the output

Input	Output
0	1
1	0



IMPLEMENTATION OF ARITHMETIC OPERATIONS AND DECODER

Objective:

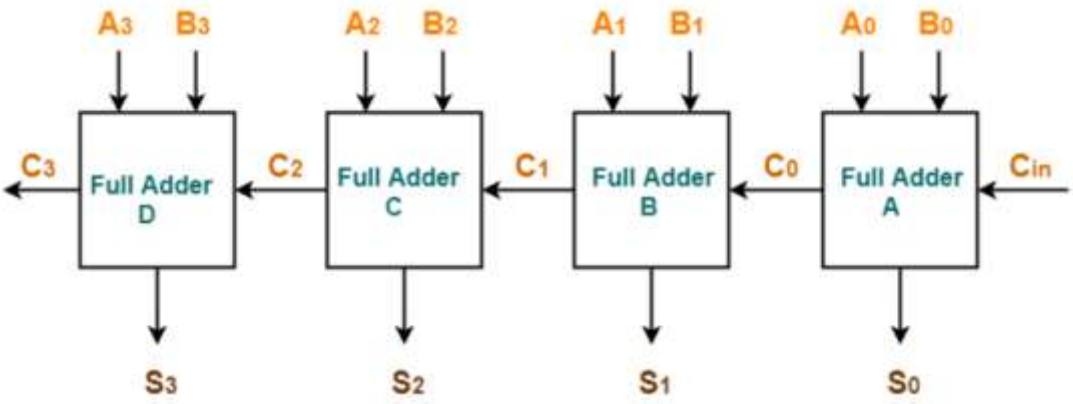
To design a layout which consists of arithmetic operations ie. addition and multiplication on 4-bit numbers and 2 * 4 decoder.

We are doing this project in 3 phases

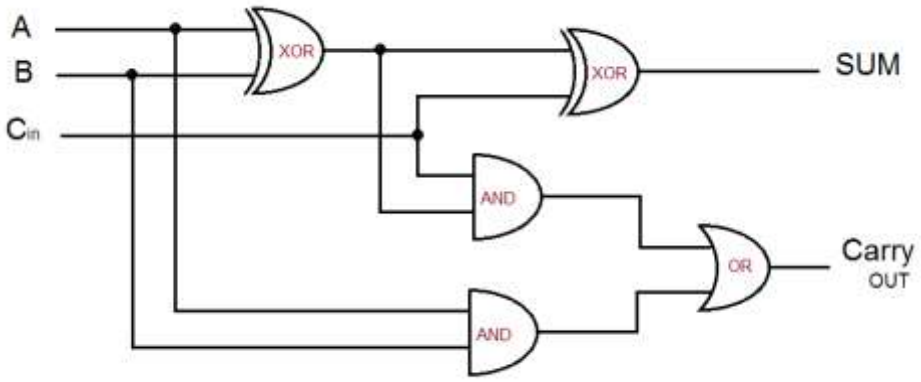
1. 4 Bit Adder
2. 2x2 Multiplier
3. 2x4 Decoder

Phase 1: 4 Bit Adder

Block circuit of the design:



Circuit design of 4 Bit Adder



Circuit design of each Full Adder

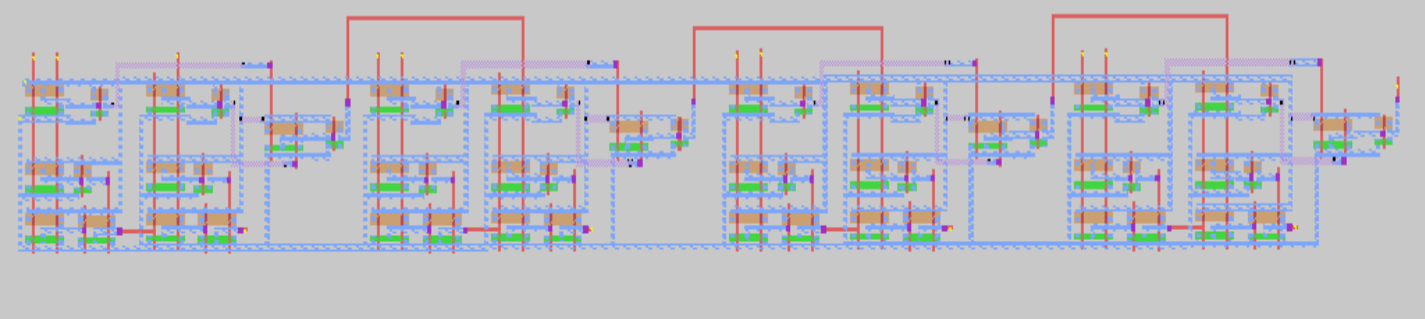
Brief description of the design:
The 4 bit adder is designed by combining 4 one bit adders with carry given in each stage.
The table shows truth table of 1 bit adder:

A	B	Carry-In	Sum	Carry-Out
0	0	0	0	0
0	0	1	1	0
0	1	0	1	0
0	1	1	0	1
1	0	0	1	0
1	0	1	0	1
1	1	0	0	1
1	1	1	1	1

Implementation details:

Layout Design : Magic
Testing Layout : IRSIM

Screen capture of the layout of the top level:

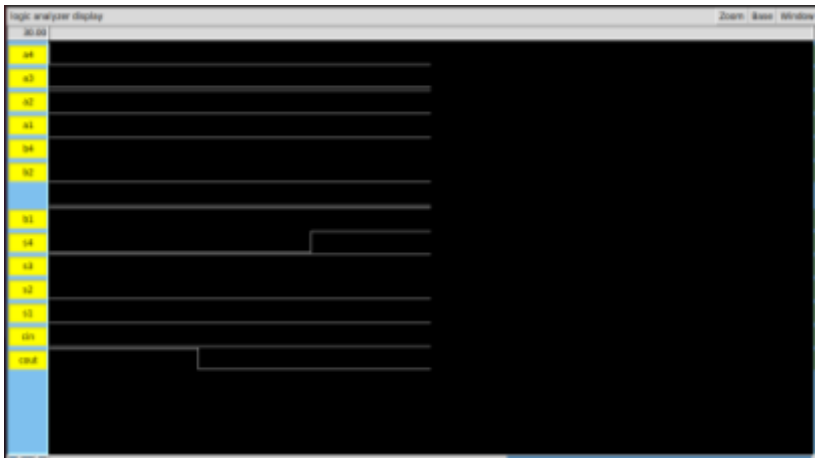


Test strategy: We used irsim to test the layout with various input and output values

Commands Used:

```
% h vdd
% l gnd
% w a1 b1 s1 cin
%
% w a1 b1 s1 cin a2 b2 s2 a3 b3 s3 a4 b4 s4 cout
% d
cout=X s4=X b4=X a4=X s3=X b3=X a3=X s2=X b2=X a2=X cin=X s1=X b1=X a1=X
time=0.000000ns

% h a4
% l a3
% h a2
% h a1
% h b4
% l b3
% l b2
% h b1
% l cin
% s
cout=1 s4=X b4=1 a4=1 s3=X b3=0 a3=0 s2=X b2=0 a2=1 cin=0 s1=X b1=1 a1=1
time=10.000000ns

% s
cout=1 s4=X b4=1 a4=1 s3=X b3=0 a3=0 s2=0 b2=0 a2=1 cin=0 s1=0 b1=1 a1=1
time=20.000000ns

% s
cout=1 s4=0 b4=1 a4=1 s3=1 b3=0 a3=0 s2=0 b2=0 a2=1 cin=0 s1=0 b1=1 a1=1
time=30.000000ns

% l a4
% l a3
% h a2
% h a1
% h b4
% l b3
% l b2
% h b1
% l cin
% s
cout=0 s4=0 b4=1 a4=0 s3=1 b3=0 a3=0 s2=0 b2=0 a2=1 cin=0 s1=0 b1=1 a1=1
time=40.000000ns

% s
cout=0 s4=1 b4=1 a4=0 s3=1 b3=0 a3=0 s2=0 b2=0 a2=1 cin=0 s1=0 b1=1 a1=1
time=50.000000ns

% ana a4 a3 a2 a1 b4 b2 b2 b1 s4 s3 s2 s1 cin cout
```

Results obtained:

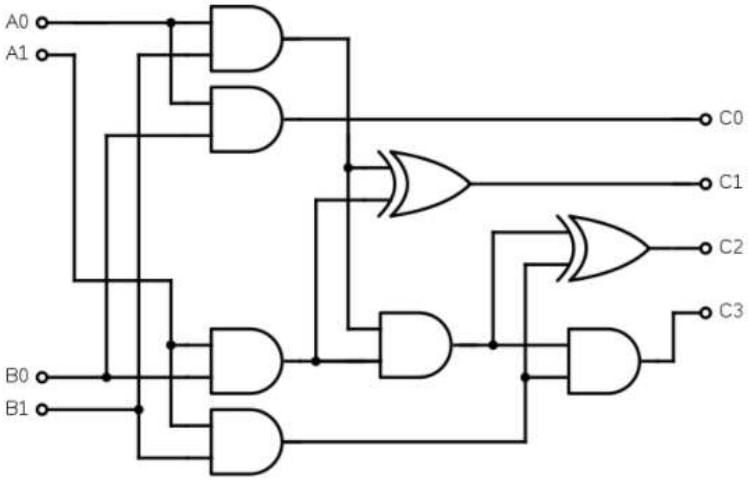


Conclusion:

The layout of the 4-bit adder is obtained and its timing graph has been verified using IRSIM.

Phase 2:
2x2 Multiplier

Block circuit of the design:

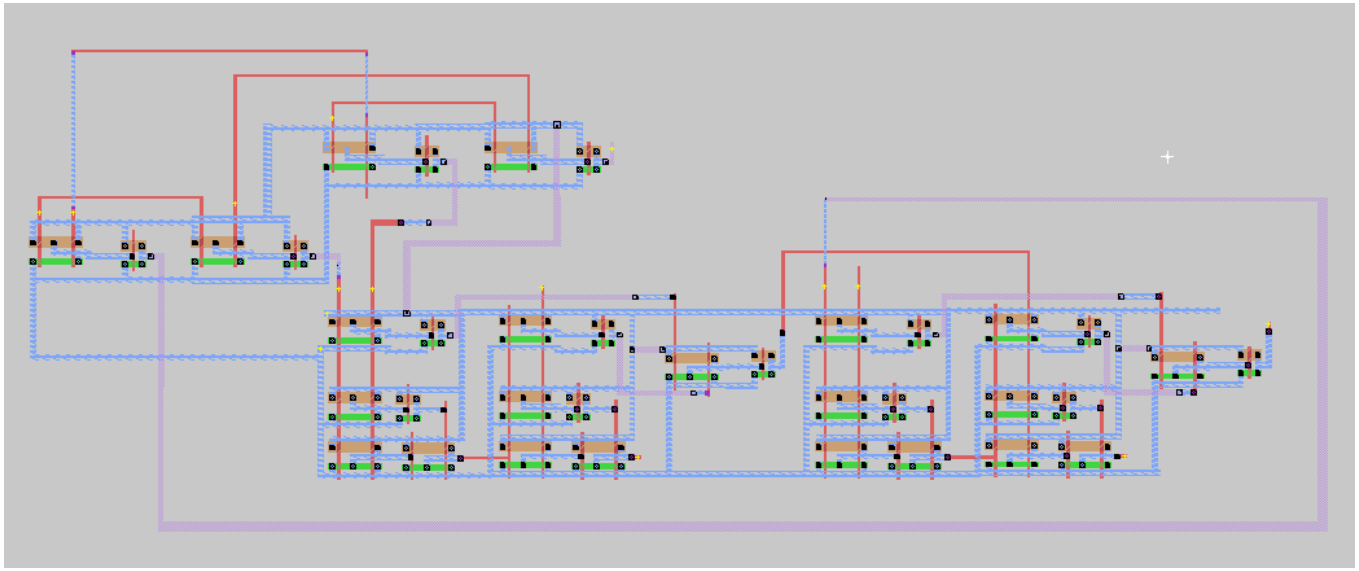


Brief description of the design:
The circuit implements a two-bit-by-two-bit multiplier by multiplying each bit of the multiplicand by each bit of the multiplier to form the partial products. The partial products are then weighted and summed to get the overall product.

Implementation details:

Layout Design	**:**	Magic
Testing Layout	**:**	IRSIM

Screen capture of the layout of the top level:

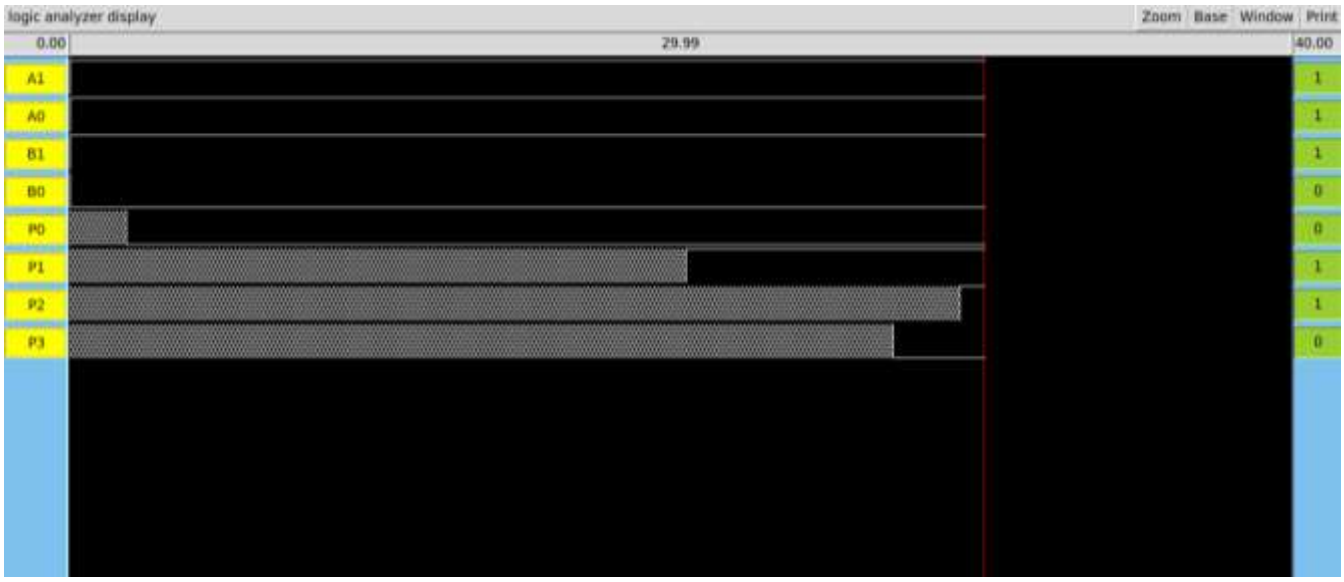


Test strategy : We used IRSIM to test the layout with various input and output values

Commands Used

```
% h vdd
% l gnd
% w A1 A0 B1 B0 b2 cin P0 P1 P2 P3
% d
P3=X P2=X P1=X P0=X cin=X b2=X B0=X B1=X A0=X A1=X time=0.000000ns

% l b2
% l cin
% h A1
% h B1
% h A0
% l B0
% s
P3=X P2=X P1=X P0=0 cin=0 b2=0 B0=0 B1=1 A0=1 A1=1 time=10.000000ns

% s
P3=X P2=X P1=X P0=0 cin=0 b2=0 B0=0 B1=1 A0=1 A1=1 time=20.000000ns

% s
P3=0 P2=1 P1=1 P0=0 cin=0 b2=0 B0=0 B1=1 A0=1 A1=1 time=30.000000ns

% ana A1 A0 B1 B0 P0 P1 P2 P3
```

Results obtained:

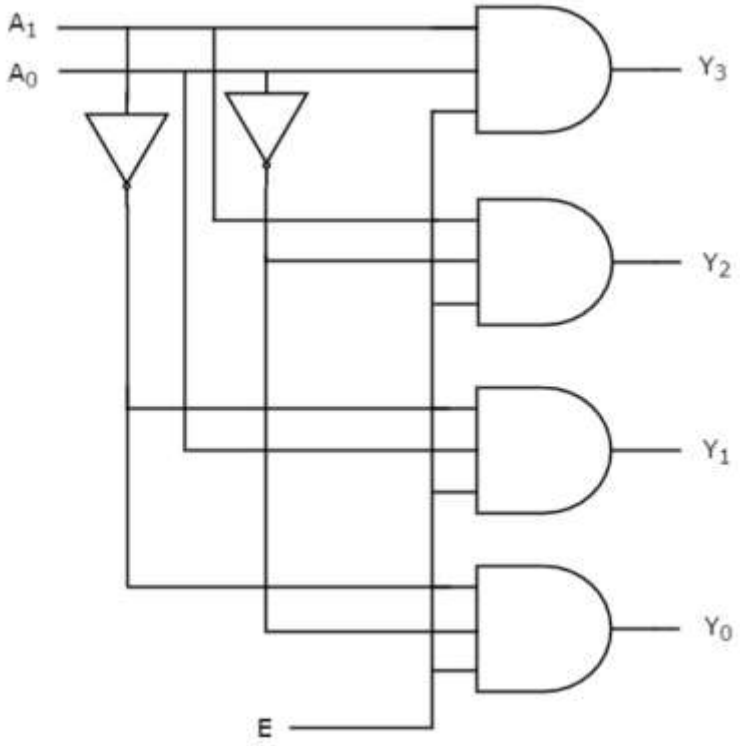


Conclusion:

The layout of the 2*2 Multiplier is obtained and its timing graph has been verified using IRSIM.

Phase 3:
2x4 Decoder

Block circuit of the design:



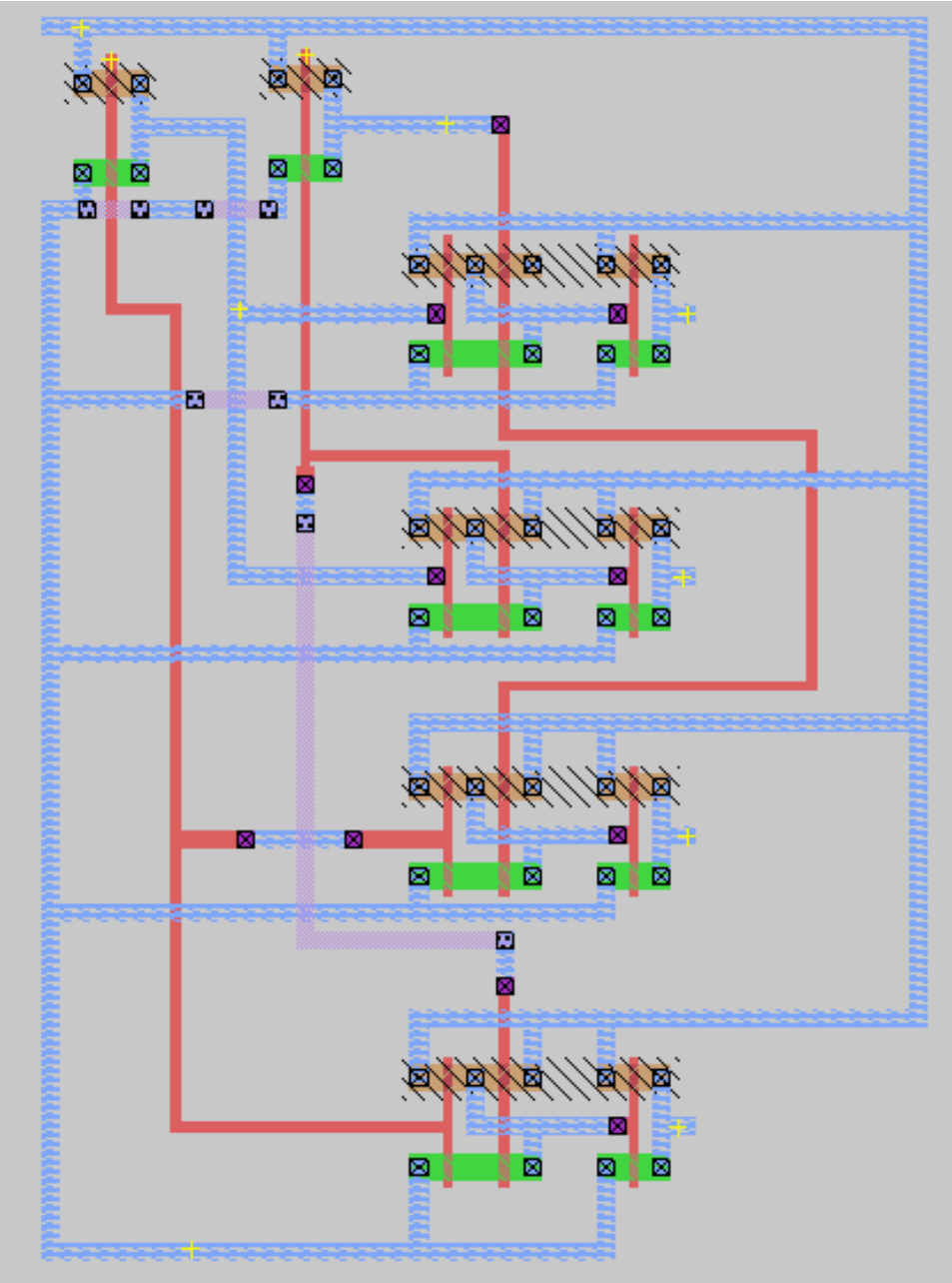
Brief description of the design:

First Enable ensures that it should be on to make the whole circuit work, A1A0 takes value from 00,01,10,11 which maps to Y0,Y1,Y2,Y3 respectively. In magic by cmos level design, each gate is interconnected in the way shown in block diagram.

Implementation details:

Layout Design	**:**	Magic
Testing Layout	**:**	IRSIM

Screen capture of the layout of the top level:

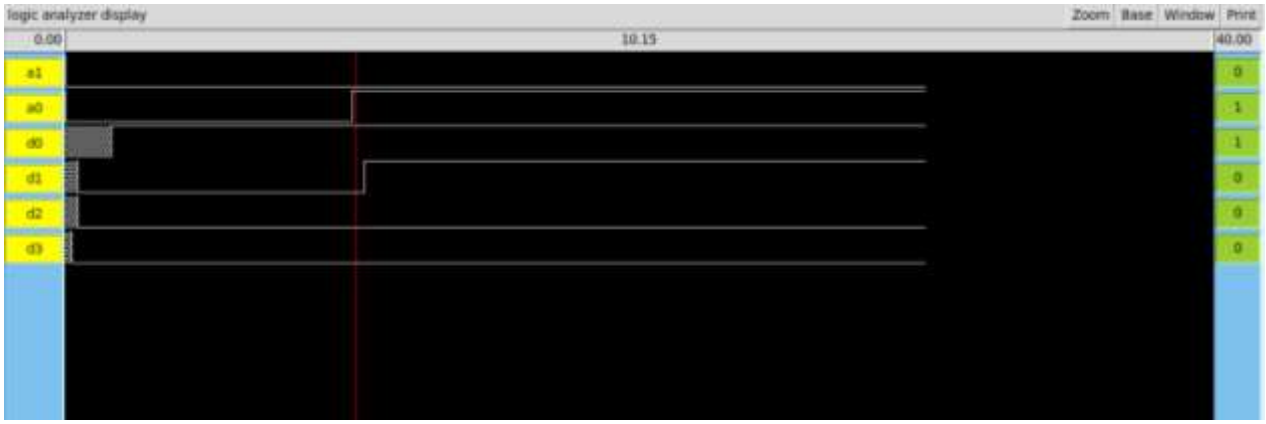


Test strategy : We used IRSIM to test the layout with various input and output values

Commands Used:

```
% h vdd
% l gnd
% w a1 a0 d0 d1 d2 d3
% d
d3=X d2=X d1=X d0=X a0=X a1=X time=0.000000ns

% l a1
% l a0
% s
d3=0 d2=0 d1=0 d0=1 a0=0 a1=0 time=10.000000ns

% l a1
% h a0
% s
d3=0 d2=0 d1=1 d0=1 a0=1 a1=0 time=20.000000ns

% s
d3=0 d2=0 d1=1 d0=1 a0=1 a1=0 time=30.000000ns

% ana a1 a0 d0 d1 d2 d3
```

Results obtained:



Conclusion:

The layout of the 2*4 decoder is obtained and its timing graph has been verified using IRSIM.