

## UNIT - I

# 1

# P - N Junction Diode and Special Purpose Diodes

### Part A : Introduction to Electronics

#### 1.1 : Evolution of Electronics and Its Impact In Industry and Society

**Q.1 Write a note on history of electronics and its evolution.**

EEP [SPPU : Marks 5]

**Ans. :** The history can be divided in two parts,

1. The beginning of electronics and
2. Solid state electronics

#### **1. The beginning of electronics**

- In 18th century many electrical experiments were conducted by many scientists. This research and the information obtained from it is the base of modern electronics.
- The beginning of electronics starts with the invention of electric currents in vacuum tubes. Scientist William Crookes proposed a theory about the current in vacuum tube consists of some particles. Sir Joseph Thompson measured the properties of the particles which are called electrons.
- But the actual history of electronics began with the invention of vacuum diode which allowed the flow of current in one direction. It was invented by J.A. Fleming, in 1904 called Fleming valve. After that, in 1907, a vacuum triode was implemented by Lee De Forest by adding a grid to basic vacuum diode, to amplify electrical signals. Due to this device, the transcontinental telephone service and radios were possible

- In 1923, Valdimir Zworykin invented the first television picture tube. It was revolution in both communication technology and also for the world media.
- During world war II, there was rapid development from the point of view which helped a lot in the development of electronic communication. Due to the development of magnetron and klystron, radar and very high frequency communication was made possible.

## 2. Solid state electronics

- In 1947, Walter Brattain, John Bardeen and William Shockley invented the famous device called the transistor. Subsequently, the transistor era began. The use of germanium and silicon semiconductor materials made these transistors gain popularity and wide-acceptance usage in different electronic circuits.
- The modern electronics what it is called today was actually started after the discovery of the transistor. Transistor opened the road for the electronics and thereafter electronics got an independent identity.
- Though the transistors were developed, some problems were there like assembling of many electronic components on a single mother board. The most important invention from this point of view was in 1950s. Jack Kilby in Texas Instruments found a very nice solution to such problems, by making first Integrated Circuit (IC). This invention started the modern computer age and brought the revolutionary changes in the fields of communication, medicine, manufacturing of electronic circuits and entertainment. Robert Noyce also did many contributions to the IC technology by joining the Fairchild Company.
- And the trend further carried forward with the JFETs and MOSFETs that were developed during 1951 to 1958 by improving the device designing process and by making more reliable and powerful transistors.

- The first operational amplifier (op-amp) was designed by Bob Widlar in 1965. Due to some problems associated with it, most popular IC op-amp 741 was designed which became the industry standard and the base for the design of many more versions of op-amp.
- In 1968, Rob Noyce and Moore left Fairchild to start new company named Intel. In 1971 their company invented the first microprocessor well known as 4004 having 2300 transistors on one silicon chip. In the same year, the company announced the first 8-bit processor called 8008. That microprocessor led the way to the successors like the 8080, 8085, 80486, Pentium series and the most modern processors like the Xeon too.
- The computer became an important tool for automated testing and virtual instrumentation in 1980s. The developments in 1980s led to reliable, fast and miniature electronic circuits.
- The various research oriented companies thought of the interconnection of the computers to form a common network. This resulted into development of an internet technology and a new framework which is now popularly known as WWW or the World Wide Web. The whole knowledge and information regarding anything is now, just clicks away.

## 1.2 : Introduction to Active and Passive Components

### Important Points to Remember

**Active components :** The components which supply energy in the circuit in the form of voltage or current, produce amplification and behave actively in the circuit are called active components.

**Passive components :** The components which consume energy in the circuit or store energy without producing any amplification are called passive components.

**Q.2 Differentiate between active and passive components.** Ques. No. 2  
EB- (SPPU : Marks 1)

Ans. :

No.	Active component	Passive component
1.	Deliver power or energy to the circuit.	Consume power or energy in the circuit.
2.	Produce energy in the form of voltage or current.	Store energy in the form of voltage or current.
3.	Can control the flow of current.	Can not control the flow of current.
4.	Capable of providing power gain.	Can not provide the power gain.
5.	These are energy donor.	These are energy acceptor.
6.	Mostly behaviour is nonlinear in nature.	Mostly behaviour is linear in nature.
7.	External source is required for the operation.	External source is not required for the operation.
8.	Examples are transistors, op-amps, diodes, voltage sources etc.	Examples are resistors, inductors, capacitors, potentiometers, switches etc.

### 1.3 : Resistors

#### Important Points to Remember

- A two terminal circuit element which introduces opposition to the flow of electric current in a circuit is called a resistor.
- The Fig. 1.1 shows the symbols of resistor.



Fig. 1.1 Symbols of resistor

- The property of resistor to oppose the flow of current is called resistance which is measured in ohms ( $\Omega$ ).

The resistors are classified as,

- Fixed resistors
- Variable resistors

**Q.3 Explain the three types of fixed resistors with neat diagrams.** Ques. No. 3  
EB- (SPPU : Marks 8)

Ans. : If the resistance value of the component used in the circuit is always constant, it is called fixed resistor. The three types of fixed resistors are,

#### 1. Carbon composition resistors

- The resistive element of carbon composition resistor is manufactured from finely ground mixture of carbon or graphite and silica. The silica acts as an inert nonconducting filler used to bind the resistor all together.
- The mixture of carbon is adjusted to obtain different ohmic values of a resistor.
- This mixture, lead and insulating material is compressed and bonded under pressure. After that it is cured in a controlling baking cycle.
- The Q.3.1 shows the construction of a carbon composition resistor.

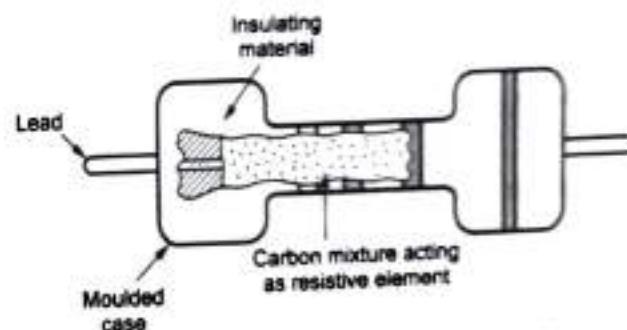


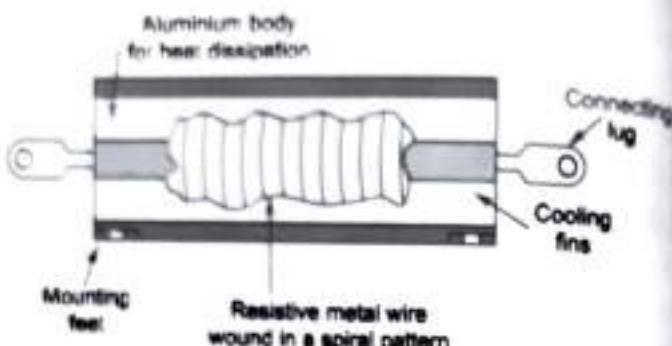
Fig. Q.3.1 Construction of carbon composition resistor

#### 2. Wire wound resistors

- The wire wound resistor is manufactured by winding a thin metal alloy wire such as nichrome onto an insulating ceramic former.



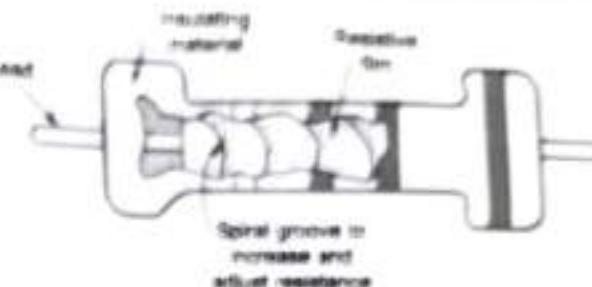
- The wire is wound in a spiral helical pattern.
- The wire is welded to end caps and then leads are welded to end caps.
- These resistors have connecting lugs instead of leads.
- By controlling the gauge of the wire and the number of turns, value of the resistance is adjusted.
- The Fig. Q.3.2 shows the construction of wire wound resistor.



**Fig. Q.3.2 Construction of wire wound resistor**

### 3. Metal film resistors

- The film resistors consist of metal film, carbon film or m-oxide film.
- The resistors are manufactured by depositing a film of resistive element on a ceramic or glass rod.
- Depending on the material used and the thickness of the film, value of the resistor can be controlled.
- Once deposited, a helical groove is cut into the film with the help of a laser beam. This helical pattern gives the effect of increasing the resistive path between the end terminals.
- The Fig. Q.3.3 shows the construction of a film resistor.



**Fig. Q.3.3 Construction of film resistor**

### Important Points to Remember

- If the resistance value of the component used in the circuit is adjustable then it is called variable resistor. It is three terminal device. Its two terminals are fixed and one is connected to a movable cap which slides along the element to vary the resistance. Its symbol is shown in the Fig. 1.2.



**Fig. 1.2 Variable resistors**

- The variable resistors are called potentiometers.

**Q.4 Explain any three types of variable resistors(potentiometers)**  
[SPPU : Marks 6]

**Ans. :** The three types of variable resistors are,

#### 1. Wire wound potentiometers

These are further classified as rotary and rheostats.

i) **Rotary** : The construction is shown in the Fig. Q.4.1.



Fig. Q.4.1 Rotary wirewound potentiometers

In this type, the former or flat strip is bent into circular form after winding. By moving the wiper, the resistance value can be changed.

ii) **Rheostat** : These have large power rating and generally used for laboratory and industry purposes. The Fig. Q.4.2 shows its construction.

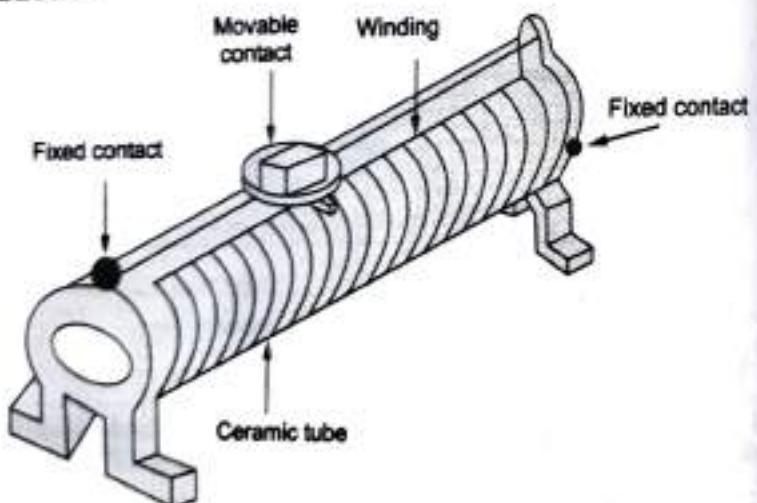


Fig. Q.4.2 Rheostats

By using movable contact, the variable resistance can be obtained. These are heavy, bulky and having large weight.

**2. Cermet potentiometers** : • In these potentiometers, a glass and cermet layer is screened on a ceramic substrate.

- Cermet is a hybrid mixture of ceramic and metal or metal oxide. They have hard but abrasive film.
- They provide better temperature coefficients and immunity towards humidity.

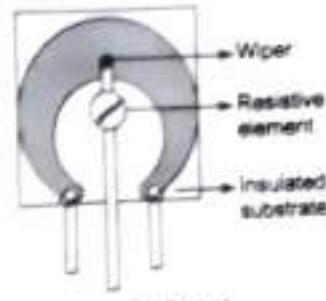
### 3. Trimmer or Preset potentiometers

- For correct adjustment of the resistance value and to compensate for tolerance build-ups and aging, trimmer potentiometers are used.

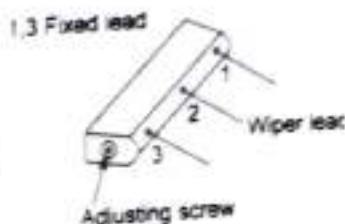
- There are two types trimmers :

- 1) Single turn - Also known as preset and
- 2) Multiturn - Known as trimpot.

- The Fig. Q.4.3 shows these two types.
- The spring loaded wiper arm moves over the carbon block to provide the necessary resistance variation.



(a) Preset



(b) Trimpot

Fig. Q.4.3 Types of trimmers

## 1.4 : Capacitors

### Important Points to Remember

- Capacitor is made up of two parallel conducting plates separated by insulating material called as dielectric. The plates can be square, circular, rectangular or spherical in shape.
- When a voltage source is connected across the plates, a momentary charging current deposits charge on the plates which establishes an electric field. This is shown in the Fig. 1.3.

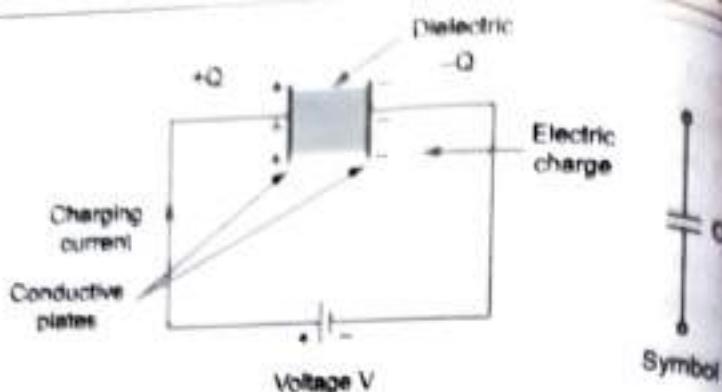


Fig. 1.3

- Capacitor when charged fully can act as a voltage source. It can discharge through a load. Thus a capacitor has got ability to store electrical energy.
- The capacitors are classified as fixed capacitors and variable capacitors.

#### Q.5 Explain the three types of fixed capacitors with neat diagrams

IITP [SPPU : Marks 5]

Ans. : The various types of fixed capacitors are,

##### 1. Paper capacitors

- Paper and metal foil are alternately wound into a tight roll. Metal used may be tin or copper.
- After winding, the extruded foils are crushed over the paper and leads in order to reduce inductance without affecting the capacitance. This roll is vacuum impregnated with wax, plastic resin, or a synthetic or mineral oil.
- To protect against moisture, this roll is encapsulated. The construction is shown in the Fig. Q.5.1

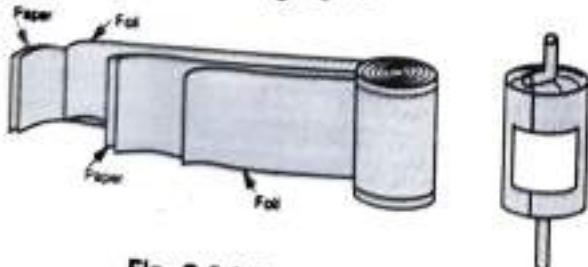


Fig. Q.5.1 Paper capacitor

These are used for high voltage and high current applications.

##### Mica capacitors

It is constructed by assembling alternately the thin mica sheets and metal foils. The foils are connected in two sets as shown in the Fig. Q.5.2 One set acts as one plate while other acts as second plate. This assembly is either encapsulated or dipped in phenolic resin following with epoxy impregnation.

These are available in the range of 50 to 500 pF

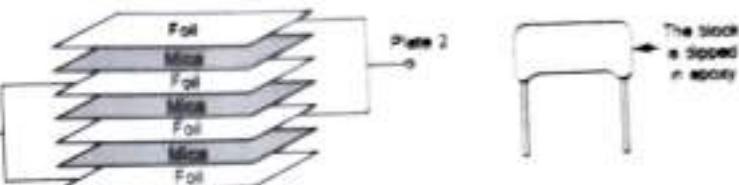


Fig. Q.5.2 Mica capacitor

- It is mainly used in high frequency circuits and as coupling and blocking capacitors.

##### 3. Ceramic capacitors

- A disc of ceramic material is taken. On each surface a metallized electrode is plated. For electrodes, mainly silver compound is used. Leads are attached by soldering.
- After this a conformal coating of a suitable resin is applied for protection against moisture.
- Construction of disc type is shown in the Fig. Q.5.3.

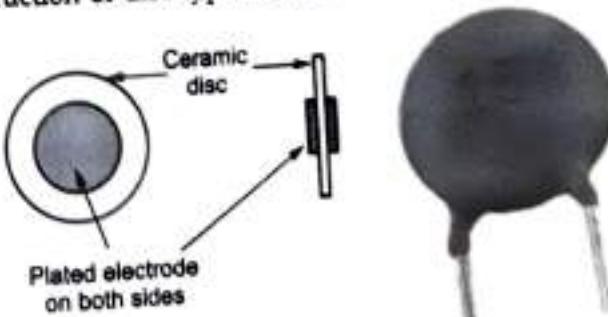


Fig. Q.5.3 Ceramic disc capacitor

- Practically ceramic capacitors are manufactured in various shapes other than disc such as tubular type, flat type and pearl type ceramic capacitors.

#### Q.6 Write a note on variable capacitors.

EE [SPPU : Marks 6]

**Ans. :** In variable capacitors, capacitance is varied using a shaft.

There are two basic types of variable capacitors,

##### 1. Ganged capacitors

- Construction of ganged capacitor is shown in the Fig. Q.6.1. They are also called as air cored capacitor as the dielectric used is air.

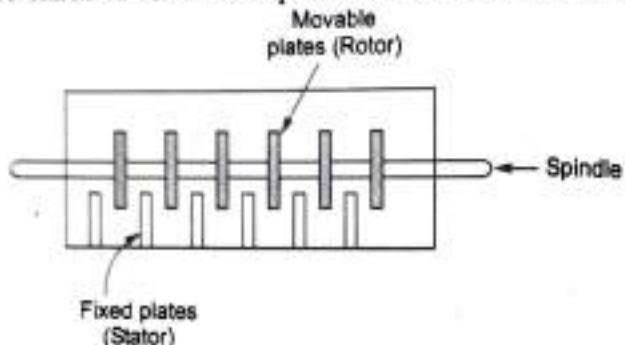


Fig. Q.6.1 Ganged capacitor

- In this type fixed air gap is there but plate area is variable.
- There are two sets of metal plates separated by air. One is stationary called stator while secondary set is connected to shaft and can be rotated. This is called rotor.
- They are used in broadcast receivers and in oscillator resonating circuits.

##### 2. Trimmer capacitors

- In this type of capacitor there is fixed plate area but gap between the plates is variable.
- Two flexible metal plates are separated by air or mica or plastic (PVC) film as the dielectric.
- The gap between the plates can be changed by means of a screw adjustment.

- The construction of plastic film trimmer capacitor is shown in the Fig. Q.6.2. These are also called plastic cored capacitors.

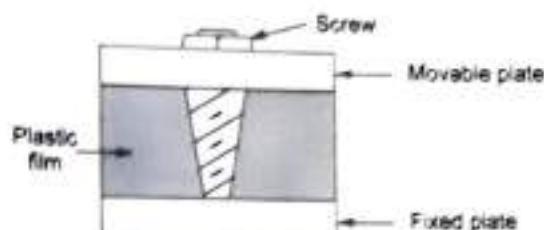


Fig. Q.6.2 Trimmer capacitor

#### 1.5 : Inductors

##### Important Points to Remember

- A coil of a wire having  $N$  turns, which is wound on a core or former of some suitable material is called an inductor or a choke. It is another passive type of electric component. It stores the electrical energy in the form of magnetic field and delivers it whenever required.
- When a current passes through such an inductor then the flux is produced. And as the current changes, e.m.f. is induced in an inductor. This property of an inductor is called its inductance.
- Unit for inductance is Henry (H).
- The schematic symbol for an inductor is shown in the Fig. 1.4.

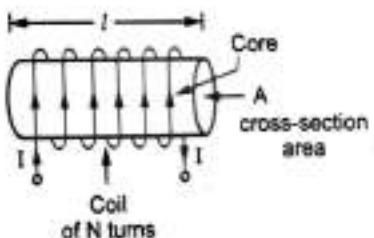


Fig. 1.4 Inductor

**Q.7 Explain the various types of inductors. State its applications.**  
SPPU : Marks 6]

**Ans. :** The three types of inductors used in electronic circuits are,

#### 1. Air-core Inductor

- Symbol for this type is shown in the Fig. Q.7.1
- Former made up of insulating material like ceramic, plastic or cardboard is used to wind the coil on it. In the air core type, air is there inside the former.



Fig. Q.7.1 Symbol

#### 2. Iron-core Inductor

- The space inside the former of coil is filled with solid iron or laminated iron core in iron core inductor.
- To reduce eddy current loss, iron is laminated. The symbol and construction is shown in Fig. Q.7.2.

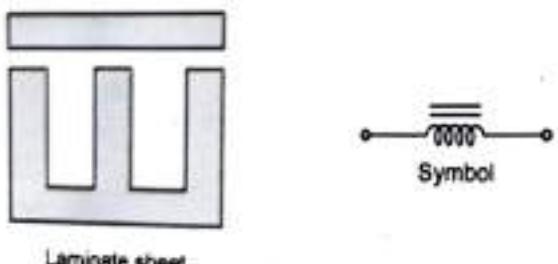
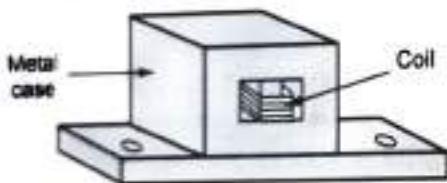


Fig. Q.7.2 Iron core inductor

- Iron-core inductor is also known as choke. It is mainly useful at low frequencies. Therefore used as filter choke and A.F. choke.

#### 3. Ferrite-core inductor

- When iron oxide is sintered with other metal oxides to control magnetic properties, ferrite is prepared.
- When the coil of wire is wound on a solid core made up of ferrites, it exhibits minimum eddy current loss. High magnetic permeability is the advantage of ferrite.



Fig. Q.7.3 Symbol

#### The applications of inductors are,

- In analog circuits and signal processing circuits.
- In filter circuits to remove the ripple contents.
- In tuned circuits used in radio reception and broadcasting circuits.
- Used around the cables to prevent radio frequency interference.
- Used as the energy storage device in switched mode power supplies.
- Used as chokes in fluorescent tubes.

#### 1.6 : Switches

**Q.8 Define switch and explain various types of switches.**

SPPU : Marks 6]

**Ans. :** • The switch is a device which is used to make or break the electrical circuit.

#### • The various types of switches are :

- 1) **S.P.S.T. (Single pole single throw switch)** : It consists of only one pole and it can be thrown only on one side for make and breaking of the circuit. This switch is connected in series with the device whose on-off action is to be controlled. This is also called one way switch with two terminals which can be seen from backside of switch.

2) S.P.D.T. (Single pole double throw switch) : This is further classified as two way switch.

- In case of a two way switch, it always makes contact with one of the two poles and in two way with centre off, it can be switched off and can be kept open from the two poles, in its central position. Two way switch is used in staircase wiring. Two way with centre off switch is used when two lamps are to be operated alternately.

- The Fig. Q.8.1 (a) shows various types of single pole switches.

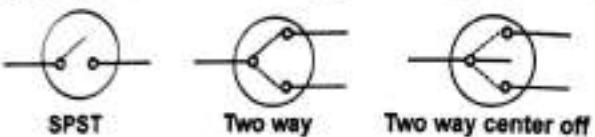


Fig. Q.8.1 (a) Types of single pole switches

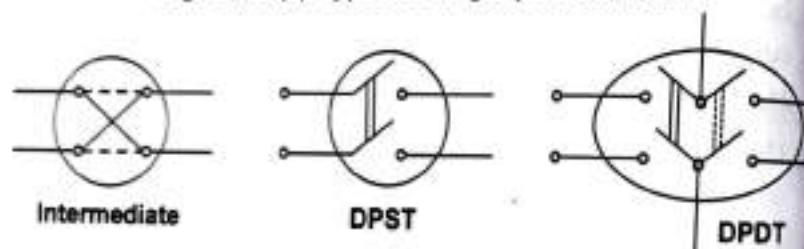


Fig. Q.8.1 (b) Types of double pole switches

3) D.P.S.T. (Double pole single throw switch) : For instantaneous and simultaneous action of both poles, a spring is provided connecting two movable blades. The double pole switch is a combination of two one way switches which are operated simultaneously.

4) D.P.D.T. (Double pole double throw switch) : This is also available in the form of intermediate switch. This type of switch is used as changeover switch.

5) T.P.S.T. (Triple pole single throw switch) : This is used for three phase supply.

6) T.P.D.T. (Triple pole double throw switch) : This switch has three poles and it can be thrown in two directions as shown in the Fig. Q.8.1 (c).

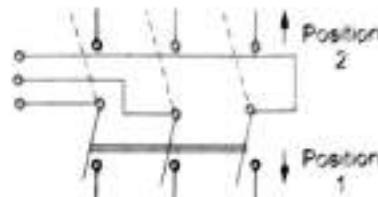


Fig. Q.8.1 (c) TPDT switch

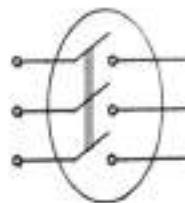


Fig. Q.8.1 (d) TPST

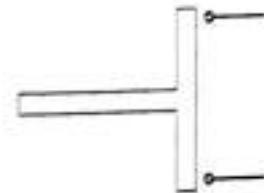


Fig. Q.8.1 (e) Push button type

- Other variety of switches are push button switch, rotary snap switch, flush switch, bed switch etc.
- Flush switches are fixed in the wall and do not project out. When high quality performance and appearance is required, it is used.
- Push button switch is normally used in controlling action of an electric bell. When knob is pressed, circuit is completed and bell rings. Similarly if knob is released, due to disconnection of circuit, bell stops ringing.
- Toggle switch : Toggle switch is manually operated (or pushed up or down) by a mechanical handle, lever or rocking mechanism. These are commonly used as light control switches.

### 1.7 : Relay

Q.9 Define relay and explain the working principle of a relay  
[SPPU : Marks 5]

Ans. : • A relay is an electrically operated switch.

- A relay is a circuit which is used to completely separate and isolate a circuit from the supply under unfavourable conditions in the circuit.

- The relays are mainly used as protective device in the circuits.
- Many relays use an electromagnet to operate a switch mechanism mechanically which are called electromagnetic relays.
- There is no electrical connection inside such relay and the control link is magnetic or mechanical.
- Many relays use an electromagnet to operate a switch mechanism mechanically which are called electromagnetic relays.
- There is no electrical connection inside such relay and the control link is magnetic or mechanical.

#### Working Principle of a Relay Circuit

- The Fig. 1.14.1 shows the simplified circuit of an electromagnetic relay circuit.
- A relay has a coil and contacts.
- Under normal operation, relay coil current produces the magnetic field which is not sufficient to attract the relay contacts.
- Under fault conditions, relay coil current increases to very high value.
- Thus relay coil produces high magnetic field due to which the contacts get closed mechanically.
- This completes the trip circuit and current flows through the trip coil.
- This further energises the protective device which disconnects the circuit to be protected from the supply.

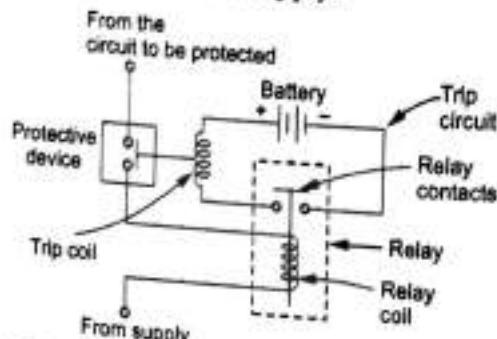


Fig. Q.9.1 Working of an relay

#### Part B : P - N Junction Diode

##### 1.8 : Intrinsic Semiconductor

**Q.10 What is Intrinsic semiconductor ? Explain its crystalline structure.** [SPPU : Marks 4]

Ans. : • A sample of semiconductor in its purest form is called an **intrinsic semiconductor**. The conductivity of such intrinsic semiconductor is very poor and practically can not be used for manufacturing of the semiconductor devices.

- In the outermost shell of intrinsic semiconductor, there are 4 electrons.
- Such atoms have a crystalline structure in which 4 electrons of one atom share the 4 electrons of an adjacent atom, forming covalent bonds. This is shown in the Fig. Q.10.1.
- Hence the outermost shells of all the atoms are completely filled with 8 electrons and are very stable.

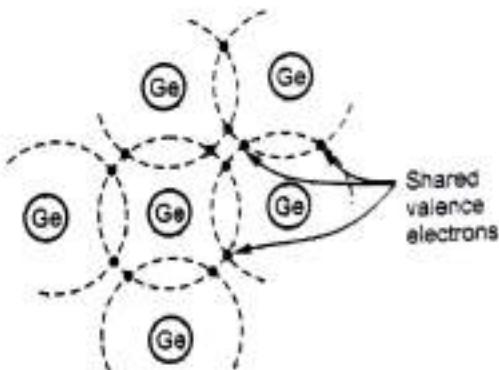


Fig. Q.10.1 Crystalline structure of germanium

## Important Points to Remember

- At room temperature, intrinsic semiconductor absorbs thermal energy which is sufficient for few valence electrons to break covalent bonds.
- Such electrons jump to conduction band and become free electrons. While moving from valence band to conduction band, they produce vacancies in valence band. These vacancies are called holes. The holes are treated as positively charged carriers.
- Thus due to thermal energy, electron-hole pairs are generated which is called **thermal generation**.
- When a battery is connected to an intrinsic semiconductor, the electrons move towards positive of battery causing an **electron current**. At the same time positively charged holes move towards negative of battery constituting **hole current**.
- Thus in semiconductors, the total current is combined effect of electron current and hole current.

### 1.9 : Extrinsic Semiconductors

**Q.11 What is extrinsic semiconductor ? What is doping ? What are the two types of extrinsic semiconductors ?**

[SPPU : Marks 4]

**Ans. :** As pure intrinsic semiconductor has poor conductivity, some impurity is added to it to increase the conductivity. This impurity is purposely added to make the material suitable for manufacturing of the semiconductor devices. Such impure semiconductor is called an **extrinsic semiconductor**.

- The process of adding other material to an intrinsic semiconductor, to improve its conductivity is called **doping**.
- The impurity added is called **dopant** and the resulting doped semiconductor material is called **extrinsic semiconductor**.

- There are two types of impurities used to obtain two different types of extrinsic semiconductors called p type and n type.
- The impurity having five valence electrons is called **pentavalent impurity**. When this is added, its each atom donates one free electron and such doping is called **donor doping**. The examples of pentavalent impurity are arsenic, bismuth, phosphorous etc. This creates n type extrinsic semiconductor.
- The impurity which has three valence electrons is called **trivalent impurity**. When this is added, its each atom creates one hole which is ready to accept an electron. Hence this is called **acceptor doping**. The examples of trivalent impurity are gallium, indium and boron. This creates p type extrinsic semiconductor.

**Q.12 Explain the formation of n-type semiconductor.**

[SPPU : Marks 5]

**Ans. :** Consider a pentavalent impurity like Arsenic (As) is added to Silicon (Si). It is a donor impurity with five valence electrons.

- The arsenic atom fits in the silicon crystal in such a way that its four valence electrons form covalent bonds with four adjacent silicon atoms. Remember that both germanium and silicon have four electrons in the valence shell.
- The fifth electron of arsenic has no chance to form covalent bond hence this electron enters in conduction band as a free electron. Thus each As atom added to Si atom donates one free electron. This is shown in the Fig. Q.12.1
- The number of free electrons can be controlled by the amount of impurity added.
- Since the free electrons have negative charges, the material obtained is called **n-type extrinsic semiconductor**.

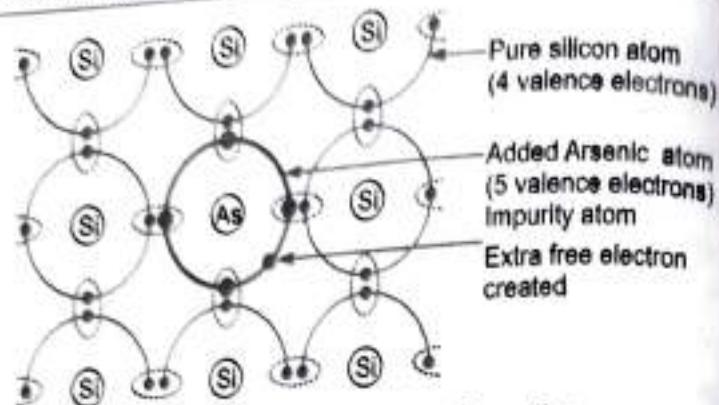


Fig. Q.12.1 n-type material formation

## Q.13 Explain the formation of p-type semiconductor.

ECE [SPPU : Marks 5]

Ans. : • Consider a trivalent impurity like Gallium (Ga) is added to Silicon (Si). It is an acceptor impurity with three valence electrons.  
 • The gallium atom fits into the silicon crystal in such a way that its three valence electrons form covalent bonds with the three adjacent silicon atoms. There is shortage of one electron to form a covalent bond. This creates a vacancy in the fourth covalent bond which is nothing but a hole. Thus each Ga atom added into Si atom creates one hole which is ready to accept an electron. This is shown in the Fig. Q.13.1

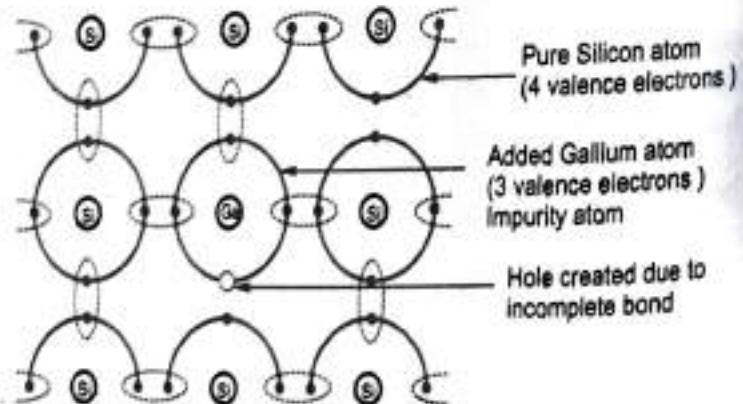


Fig. Q.13.1 p-type material formation

- The number of such holes can be controlled by the amount of impurity added to the silicon.
- As the holes are treated as positively charged, the material obtained is called **p-type extrinsic semiconductor**.

## Q.14 Compare Intrinsic and extrinsic semiconductors.

ECE [SPPU : Marks 4]

Ans. : • The following table gives the comparison of intrinsic and extrinsic semiconductor materials.

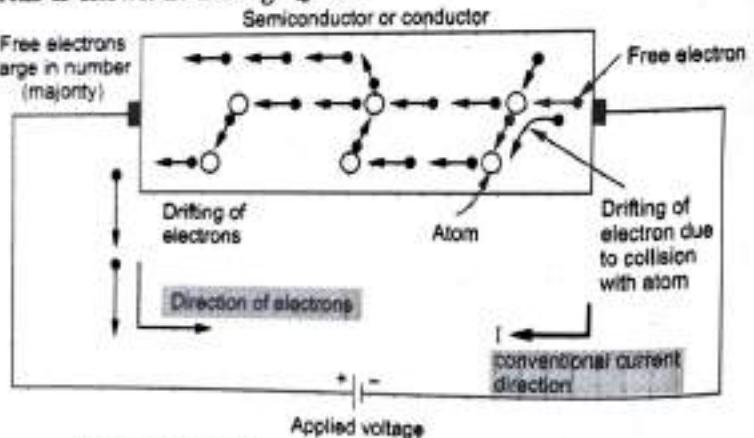
Sr. No.	Intrinsic	Extrinsic
1.	Purest in form without any impurity.	Impurity is added hence not pure.
2.	Naturally available.	Obtained by the process called doping.
3.	Number of electrons and holes is always same.	Either electrons are more or holes are more depending on the type of the material.
4.	Conductivity is very poor.	Conductivity is high and can be controlled by doping level.
5.	Current flow is equal by electrons and holes.	Current flow is mainly because of majority carriers (electrons or holes) depending on the type n or p.
6.	Not used practically for manufacturing the devices.	Used for manufacturing of electronic devices.

## 1.10 : Drift and Diffusion Currents

**Q.15 What is drift current ? State its expression.** ESE [SPPU : Marks 4]

**Ans. :**

- When a voltage is applied to a semiconductor, the free electrons try to move in a straight line towards the positive terminal of the battery.
- The electrons, moving towards positive terminal collide with the atoms of semiconductor and connecting wires, along its way. Each time the electron strikes an atom, it rebounds in a random direction.
- But still the applied voltage make the electrons drift towards the positive terminal. This drift causes current to flow in a semiconductor, under the influence of the applied voltage.
- This current produced due to drifting of free electrons is called drift current.
- Thus drift current means the flow of current due to bouncing of electrons from one atom to another, travelling from negative terminal to positive terminal of the applied voltage.
- This is shown in the Fig. Q.15.1.



**Fig. Q.15.1 Drift mechanism causing drift current**

The drift current density for electrons and holes is given by:

$$J_n = nq\mu_n E \text{ and } J_p = pq\mu_p E A/m^2$$

Where

$n$  = Concentration of electrons/m<sup>3</sup>

$p$  = Concentration of holes/m<sup>3</sup>

$q$  = Charge on each electron =  $1.6 \times 10^{-19} C$

$\mu_n, \mu_p$  = Mobility of electrons and holes respectively in m<sup>2</sup>/V-sec

$E$  = Applied field intensity in V/m

$$E = \frac{V}{L} \text{ where}$$

$V$  = Applied voltage

$L$  = Length of semiconductor in m

**Q.16 What is diffusion current ? State its equation.**

ESE [SPPU : Marks 4]

**Ans. :** • Consider a piece of semiconductor which is nonuniformly doped. Due to such nonuniform doping, one type of charge carriers occur at one end of a piece of semiconductor.

- The charge carriers are either electrons or holes, of one type depending upon the impurity used.
- They have the same polarity and hence experience a force of repulsion between them.
- The result is that there is a tendency of the charge carriers to move gradually i.e. to diffuse from the region of high carrier density to the low carrier density. This process is called diffusion.
- This movement of charge carriers under the process of diffusion constitutes a current called diffusion current. This is shown in the Fig. Q.16.1.
- The diffusion current continues till all the carriers are evenly distributed throughout the material.

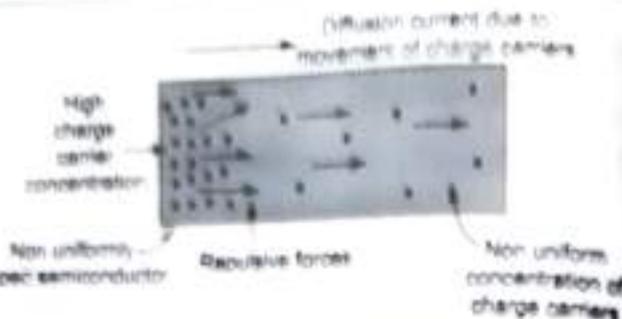


Fig. Q.16.1 Diffusion Current

- The expression for diffusion current density is,

$$J_p = -q D_p \frac{dp}{dx} \quad \text{or} \quad J_n = +q D_n \frac{dn}{dx}$$

Where  $D_p$  and  $D_n$  are diffusion constants of holes and electrons respectively.

$q$  = Charge on each electron  $\frac{dp}{dx}$  and  $\frac{dn}{dx}$  is concentration gradient of holes and electrons respectively.

**Q.17** A bar of n-type silicon has a length of 4 cm and cross-section of  $10 \text{ mm}^2$ . It is subjected to a voltage of 1 V across its length. Find the drift current if mobility of free electrons is  $1300 \text{ cm}^2/\text{V-sec}$  and charge on each electron is  $1.6 \times 10^{-19} \text{ C}$ . The concentration of free electrons is  $0.9615 \times 10^{21}/\text{m}^3$

**Ans.:** Given

$$n = 0.9615 \times 10^{21}/\text{m}^3, q = 1.6 \times 10^{-19} \text{ C}$$

$$\mu_n = 1300 \text{ cm}^2/\text{V-sec} = 1300 \times 10^{-4} \text{ m}^2/\text{V-sec}$$

$$L = 4 \text{ cm}, a = 10 \text{ mm}^2 = 10 \times 10^{-6} \text{ m}^2, V = 1 \text{ V}$$

$$E = \frac{V}{L} = \frac{1}{4 \times 10^{-2}} = 25 \text{ V/m}$$

$$J = \text{Drift current density} = n q \mu_n E$$

$$= 0.9615 \times 10^{21} \times 1.6 \times 10^{-19} \times 1300 \times 10^{-4} \times 25$$

$$= 500 \text{ A/m}^2$$

$$I_n = \text{Drift current} = J \times a$$

$$= 500 \times 10 \times 10^{-6} = 5 \text{ mA}$$

### 1.11 P-N Junction Diode

#### Important Points to Remember

- The p-type and n-type materials are chemically combined with a special fabrication technique to form a p-n junction.
- On p-side, there are large number of holes while on n-side there are large number of free electrons.
- Such a p-n junction acts as a famous device called p-n junction diode.

**Q.18** Write a note on p-n junction diode. Draw its symbol.

EF (SPPU : Marks 4)

**Ans.:** • The p-n junction forms a popular semiconductor device called **p-n junction diode**.

- Its two terminals are called electrodes, one each from p-region and n-region.
- It can conduct current only in one direction.
- The p-region is anode and n-region is cathode.
- Its symbol is shown in the Fig. Q.18.1. The arrowhead in the symbol indicates the direction of the conventional current which can flow when an external voltage is applied in a specific manner across the diode.

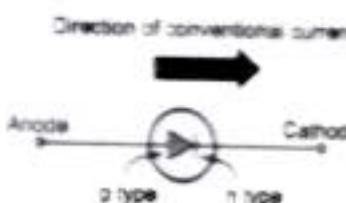


Fig. Q.18.1 Symbol of a diode

- Applying external voltage to p-n junction diode is called biasing.
- Depending upon the polarity of external d.c. voltage applied to diode, the biasing is classified as,

1. Forward biasing
2. Reverse biasing

**Q.19** Explain the formation of depletion region in unbiased p-n junction diode.

EF (SPPU : Marks 5)

**Ans.:** • In a p-n junction, on p-side there are large number of holes while on n-side there are large number of free electrons.

Hence there is nonuniform distribution of charge carriers due to which diffusion of charge carriers from one side to another starts.

- The majority holes on p side start diffusing into n side while the majority free electrons on n side start diffusing into p side.
- In n region, the holes diffusing from n-side, recombine with the electrons. Thus due to additional positively charged holes, these atoms on n-side become positive immobile ions, just near the junction in n region.
- In p region, the free electrons diffusing from n-side, recombine with the holes of the atoms. Thus due to gain of additional negatively charged free electrons, these atoms become negative immobile ions, just near the junction in p-region.
- As more holes diffuse on n side, large immobile positive charge accumulates near the junction on n side. This positive charge repels the positively charged holes and the diffusion of holes stops.
- Similarly large negative charge accumulates near the junction on p side. This negative charge repels the negatively charged electrons and the diffusion of electrons stops.
- Thus there exists a wall near the junction with negative immobile charge on p side and positive immobile charge on n side. There are no charge carriers in this region. The region is depleted of the charge carriers hence called depletion region, depletion layer or space charge region. The depletion region is shown in the Fig. Q.19.1 (Refer Fig. Q.19.1 on next page).

#### Important Point to Remember

- Due to positive and negative immobile ions on either sides of depletion region, there exists a voltage across the depletion region which is called barrier potential, junction potential or cut-in voltage of diode.
- It is denoted as  $V_b$  and it is about 0.7 V for Silicon and 0.3 V for Germanium diode.

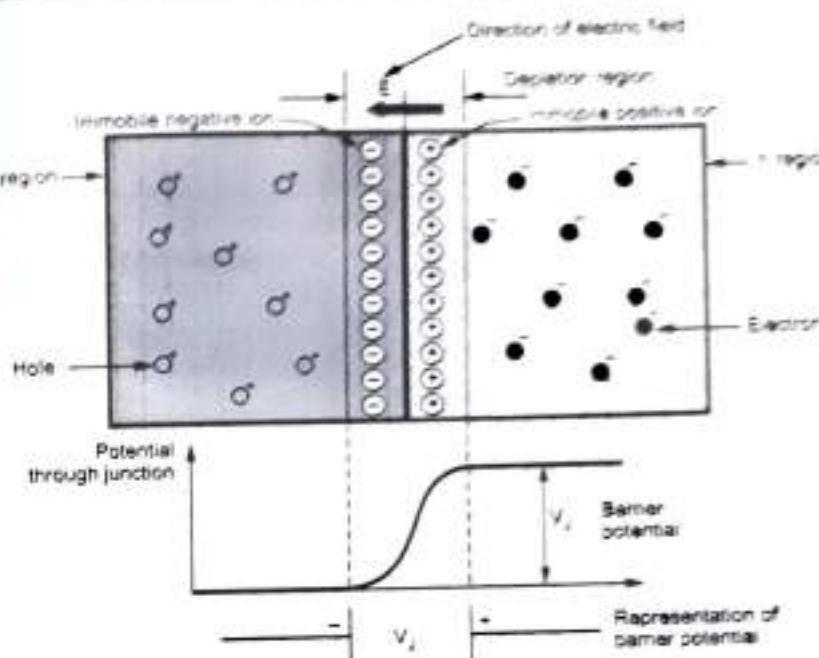


Fig. Q.19.1 Formation of depletion region in a p-n junction

#### 1.12 : Forward Biasing of Diode

Q.20 Explain the forward biasing of a diode.

ESE (SPPU : Marks 6)

Ans. : • When an external d.c. voltage is connected in such a way that p region is connected to positive and n region to negative of the d.c. voltage then the biasing is called forward biasing. It is shown in the Fig. Q.20.1

- As long as applied voltage V is less than barrier potential there is no conduction.
- When applied voltage V is more than barrier potential, it overcomes the barrier potential and reduces the width of depletion region. This is because the negative of battery pushes the free electrons against the barrier from n to p region while

positive of battery pushes holes against barrier from p to n region.

- As applied voltage is increased, at a particular value, the depletion region becomes very narrow and majority charge carriers can easily cross the junction.
- This large number of majority charge carriers constitute a current called forward current.
- The current in the p region is due to movement of holes so it is hole current. The current in the n region is due to movement of electrons so it is electron current. The holes in p region and electrons in n region are majority charge carriers. Hence the forward current is due to majority charge carriers.
- The forward current in a diode is shown in the Fig. Q.20.2.

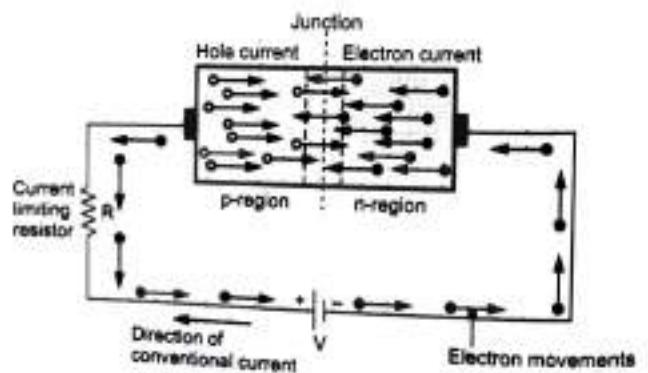
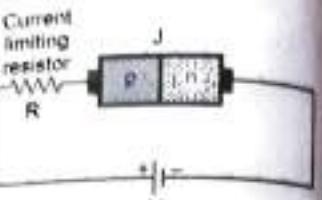
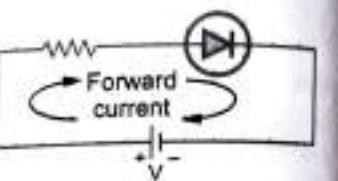


Fig. Q.20.2 Forward current in a diode



(a) Forward biasing



(b) Symbolic representation

Fig. Q.20.1

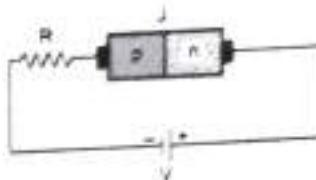
### 1.13 : Reverse Biasing of Diode

SPPU : Marks 6

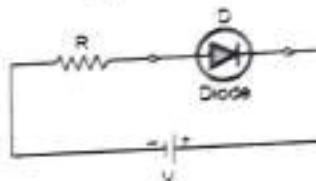
- Q.21 Explain the reverse biasing of a diode.

Ans. : \* When an external d.c. voltage is connected in such a way that p region is connected to negative and n region to positive terminal of the d.c. voltage then the biasing is called reverse biasing. It is shown in the Fig. Q.21.1.

- In reverse biasing, negative of battery attracts the holes in p region and positive of battery attracts the electrons in n region away from the junction.
- This widens the depletion region and barrier potential increases. No majority charge carrier can cross the junction.
- The resistance of the reverse biased diode is very high and the diode is said to be nonoperative in the reverse biased.
- However due to increased barrier potential, the free electrons on p side are dragged towards positive while holes on n side are dragged towards negative of the battery.
- This constitutes a current called reverse current. It flows due to minority charge carriers and hence its magnitude is very very small.
- For constant temperature, the reverse current is almost constant though applied reverse voltage is increased upto certain limit. Hence it is called reverse saturation current denoted as  $I_0$ . This is shown in the Fig. Q.21.2.



(a) Reverse biasing



(b) Symbolic representation

Fig. Q.21.1

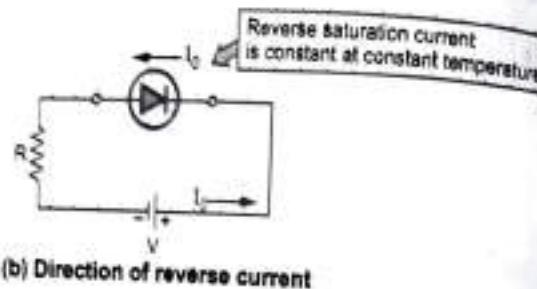
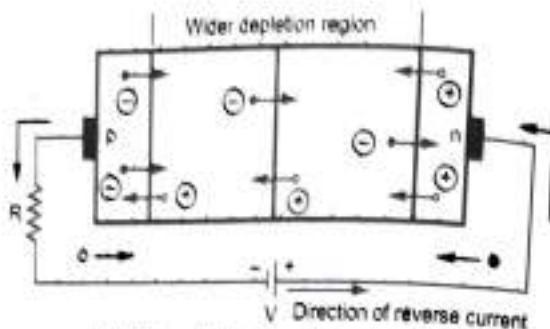


Fig. Q.21.2 Reverse biased diode

- The reverse current  $I_0$  is of the order of few microamperes for Ge and few nanoamperes for Si diodes.

#### 1.14 : V-I Characteristics of Diode

**Q.22 Explain V-I characteristics of p-n junction diode.**

BBP [SPPU : Marks 6]

**Ans. :** In forward biasing  $V_f$  is the voltage across the p-n junction and  $I_f$  is the forward current hence graph of  $I_f$  against  $V_f$  is called forward characteristics of p-n junction.

- The forward characteristics of a diode is shown in the Fig. Q.22.1
- It is divided into two regions :

- Region O to P : As long as  $V_f$  is less than cut-in voltage ( $V_c$ ) the current flowing is very small.

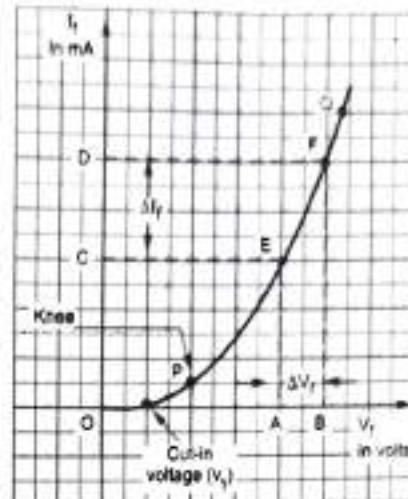


Fig. Q.22.1 Forward characteristics of a diode

- Region P to Q and onwards : When  $V_f$  exceeds  $V_c$  i.e. cut-in voltage, the depletion region becomes very thin and current  $I_f$  increases suddenly. This increase in the current is exponential as shown in the Fig. Q.22.1 by the region P to Q.
- The point P, after which the forward current starts increasing exponentially is called knee of the curve and the corresponding voltage is called knee voltage.
- The reverse voltage across the diode is  $V_R$  and reverse current through the diode is  $I_R$  hence graph of  $I_R$  against  $V_R$  is called reverse V-I characteristics of p-n junction.
- As the reverse voltage is increased, reverse current increases initially but after a small voltage becomes constant equal to reverse saturation current  $I_0$ . This point is shown as P, in the Fig. Q.22.2.
- After this, though reverse voltage is increased, the reverse current remains constant till point A where diode breakdown occurs.

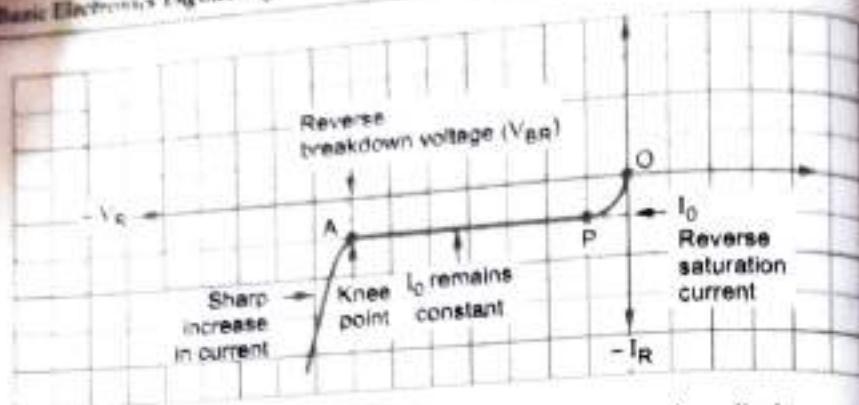


Fig. Q.22.2 Reverse characteristics of p-n junction diode

- The point A is called knee point and the corresponding voltage is called **reverse breakdown voltage** of diode.
- The complete V-I characteristics of p-n junction diode is the combination of its forward as well as reverse characteristics. This is shown in the Fig. Q.22.3.

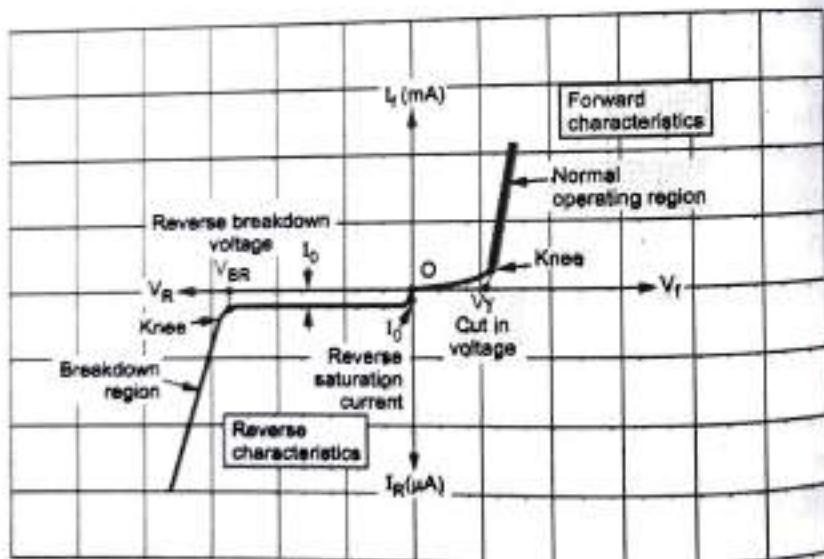


Fig. Q.22.3 Complete V-I characteristics of a diode

**Important Points to Remember**

- The diode current equation is:

$$I = I_0 [e^{V/\eta V_T} - 1]$$

where  $I_0$  = Reverse saturation current in A

$V$  = Applied voltage (positive for forward bias and negative for reverse bias)

$\eta = 1$  for Ge and  $\eta = 2$  for Si diode

$V_T$  = Voltage equivalent of temperature

$V_T = kT$ ,  $k = 8.62 \times 10^{-5}$  eV/K,  $T$  in °K

**1.15 : Diode as a Switch**

**Q.23 Explain how diode can be used as a switch.** SPPU : Marks 4

**Ans. :** In forward biased condition, the forward resistance of a diode is very small and ideally it can be treated to be zero. Thus ideally forward biased diode acts as a zero resistance device which is a **closed switch**. Hence ideal model of a diode in forward biased condition is a closed switch as shown in the Fig. Q.23.1.

In reverse biased condition, the reverse resistance is very very large and it can be treated to be infinite. Thus ideally the reverse biased diode can be treated as infinite resistance device which does not allow the flow of current. Such a device is nothing but an **open switch**. Hence ideal model of a diode in reverse biased condition is an open switch as shown in the Fig. Q.23.1.

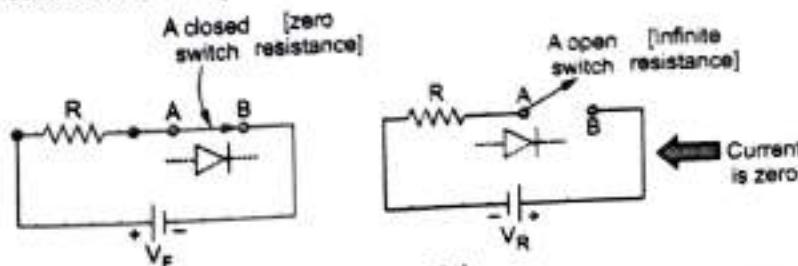


Fig. Q.23.1

- For an ideal diode in forward biased condition, the barrier potential and the forward resistance of a diode is neglected. It is assumed that it conducts instantly when the forward voltage is applied to it.

- For an ideal diode in reverse biased condition, the reverse resistance of a diode is infinite and the current is zero.

- Thus the diode can be used as a switch in the circuit to control the flow of current only in one direction and blocks the current in other direction.

- As ideal diode conducts instantly in forward biased condition and does not conduct at all in reverse biased condition. The ideal characteristics for a diode as a switch are as shown in the Fig. Q.23.2

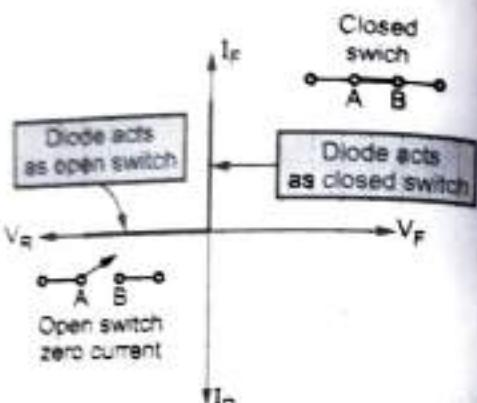


Fig. Q.23.2

#### Q.24 What is rectifier ? What are its types ?

**EF [SPPU : May-18, Marks 2]**

**Ans. :** • A rectifier is a device which converts a.c. voltage to pulsating d.c. voltage, using one or more p-n junction diodes.

- The three types of rectifiers using diodes are,

- Half wave rectifier
- Full wave rectifier with center tap
- Bridge rectifier

#### 1.16 : Rectifier

#### 1.17 : Half Wave Rectifier

**Q.25 Draw the circuit and explain the operation of a half wave rectifier alongwith the waveforms.**  
**EF [SPPU : May-18, Marks 4]**

**Ans. :** • The circuit diagram is shown in the Fig. Q.25.1

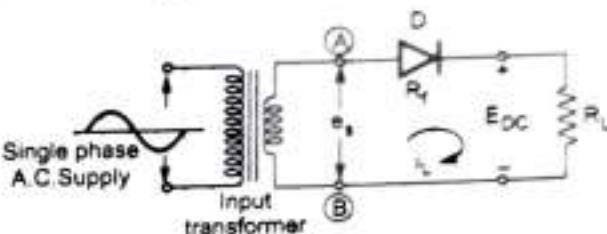


Fig. Q.25.1 Halfwave rectifier

- A sinusoidal a.c. voltage, having frequency of 50 Hz is applied to rectifier circuit using suitable step-down transformer, with necessary turns ratio.

- The transformer secondary voltage  $e_s$  is mathematically given by,

$$e_s = E_{\text{sm}} \sin \omega t \quad \text{with } \omega = 2\pi f \text{ and } f = \text{Supply frequency}$$

- The turns ratio of transformer decides the secondary voltage  $e_s$ , which is applied to rectifier.

#### Operation of the Circuit :

- During the positive half cycle of input a.c. voltage, terminal (A) becomes positive with respect to terminal (B). The diode is forward biased and the current flows in the circuit in the clockwise direction, as shown in the Fig. Q.25.2 (a). This current is also flowing through the load resistance  $R_L$  hence denoted as  $i_L$  (load current).

- During negative half cycle when terminal (A) is negative with respect to terminal (B), diode becomes reverse biased. Thus it acts as an open circuit. Hence no current flows in the circuit as shown in the Fig. Q.25.2 (b).

- Thus the circuit current, which is also the load current, is in the form of half sinusoidal pulses.

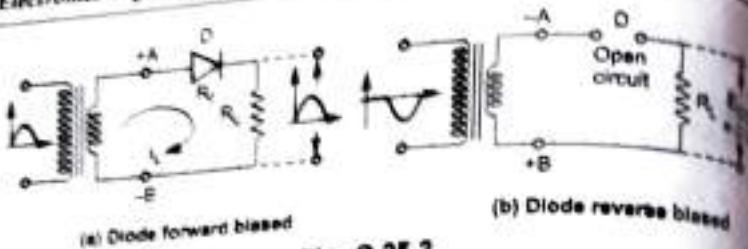


Fig. Q.25.2

- The load voltage, being the product of load current and resistance, will also be in the form of half sinusoidal pulses, different waveforms are illustrated in Fig. Q.25.3.

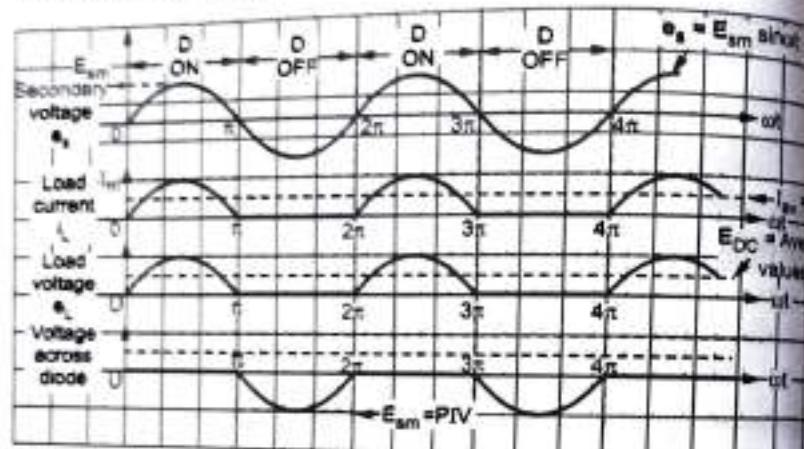


Fig. Q.25.3 Load current and load voltage waveforms for half wave rectifier

#### Important Points to Remember

- The peak value of the load current is given by,  

$$\therefore I_m = \frac{E_{sm}}{R_f + R_L + R_s} \text{ where } R_s = \text{Resistance of second}$$

$$R_f = \text{Forward resistance of diode}$$
- If  $R_s$  and  $R_f$  are not given they should be neglected while calculating  $I_m$ .

ESE (SPPU : May-11, Marks 2)

#### Q.26 Define ripple factor. State its expression.

Ans. : • The measure of ripples present in the output is with the help of a factor called **ripple factor** denoted by  $\gamma$ . It tells how smooth is the output.

- Mathematically **ripple factor** is defined as the ratio of R.M.S. value of the a.c. component in the output to the average or d.c. component present in the output.

$$\therefore \text{Ripple factor } \gamma = \frac{\text{R. M. S. value of a.c. component of output}}{\text{Average or d.c. component of output}}$$

- The output current is composed of a.c. component as well as d.c. component.

Let  $I_{ac} = \text{R.M.S. value of a.c. component present in output}$

$I_{DC} = \text{D.C. component present in output}$

- $I_{RMS} = \text{R.M.S. value of total output current} = \sqrt{I_{ac}^2 + I_{DC}^2}$   
 $\text{i.e. } I_{ac} = \sqrt{I_{RMS}^2 - I_{DC}^2}$

$$\text{Ripple factor} = \frac{I_{ac}}{I_{DC}} = \frac{\sqrt{I_{RMS}^2 - I_{DC}^2}}{I_{DC}} = \sqrt{\left(\frac{I_{RMS}}{I_{DC}}\right)^2 - 1} \quad \dots \text{As per definition}$$

#### Important Points to Remember

- The various parameters and their expressions for half wave rectifier are,

$I_{DC} = \text{Average or d.c. load current} = \frac{I_m}{\pi}$

$I_{RMS} = \text{RMS value of load current} = \frac{I_m}{2}$

$E_{DC} = \text{Average or d.c. load voltage} = \frac{E_{sm}}{\pi}$

$P_{DC} = \text{D.C. power output} = I_{DC}^2 R_L$

$P_{DC} = \frac{E_{sm}^2 R_L}{\pi^2 [R_f + R_L + R_s]^2}$

$P_{AC} = \text{A.C. power input}$ 

$$= I_{\text{RMS}}^2 (R_L + R_f + R_s)$$

$$\% \eta = \text{Rectifier efficiency} = \frac{P_{DC}}{P_{AC}} \times 100$$

$$\% \eta_{\text{max}} = \text{Maximum rectifier efficiency}$$

$$= 40.6 \%$$

Ripple factor = 1.21

PIV = Peak Inverse Voltage =  $E_{\text{sm}}$ 

TUF = Transformer Utilization Factor = 0.28

### 1.18 : Full Wave Rectifier

**Q.27** Draw the full wave rectifier circuit and explain its operation along with the waveforms.

[SPPU I May-16, Marks]

**Ans. :** The full wave rectifier circuit is shown in the Fig. Q.27.1

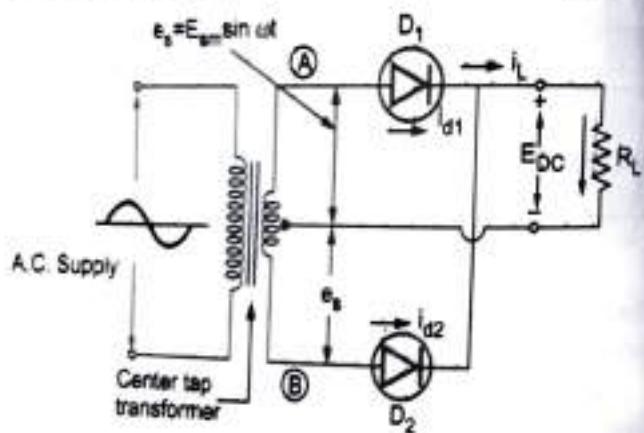


Fig. Q.27.1 Full wave rectifier

- It uses a center tap transformer.
- It uses two diodes which feed a common load resistance  $R_L$ .
- The a.c. voltage is applied through a suitable power transformer with proper turns ratio.

### Operation of the Circuit :

Consider the positive half cycle of ac input voltage in which terminal (A) is positive and terminal (B) is negative due to center tap transformer.

The diode  $D_1$  will be forward biased and hence will conduct, while diode  $D_2$  will be reverse biased and will act as an open circuit and will not conduct. The diode  $D_1$  supplies the load current, i.e.  $i_L = i_{d1}$ .

In the next half cycle of ac voltage, polarity reverses and terminal (A) becomes negative and (B) positive. The diode  $D_1$  conducts, being forward biased, while  $D_2$  does not, being reverse biased. The diode  $D_2$  supplies the load current, i.e.  $i_L = i_{d2}$ .

The load current flows in both the half cycles of ac voltage and in the same direction through the load resistance. Hence we get rectified output across the load.

The load current is sum of individual diode currents flowing in corresponding half cycles.

The waveforms of secondary voltage (one half), load current and load voltage are shown in the Fig. Q.27.2.

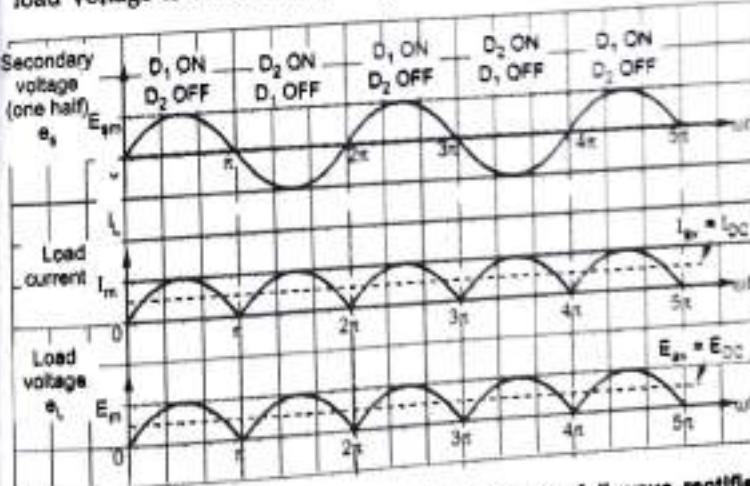


Fig. Q.27.2 Load current and voltage waveforms for full wave rectifier

## Important Points to Remember

- $R_f$  = Forward resistance of diodes and  $R_L$  = Load resistance
- $R_s$  = Winding resistance of each half of secondary
- $E_{sm}$  = Maximum value of a.c. input voltage across each half secondary winding
- The maximum value of the load current  $I_m = \frac{E_{sm}}{R_s + R_f + R_L}$

Q.28 Derive the expressions for the average d.c. current, d.c. load voltage and RMS value of the load current for the full wave rectifier circuit with two diodes.

ISCE [SPPU : May-04, 10, Dec.-07, March-09]

Ans. : The average or d.c. value of the load current ( $I_{DC}$ ) :

- Consider one cycle of the load current  $i_L$  from 0 to  $\pi$  to obtain the average value which is d.c. value of load current.

$$i_L = I_m \sin \omega t \quad 0 \leq \omega t \leq \pi$$

$$I_{av} = I_{DC} = \frac{1}{\pi} \int_0^{\pi} i_L d(\omega t)$$

$$= \frac{1}{\pi} \int_0^{\pi} I_m \sin \omega t dt$$

$$= \frac{I_m}{\pi} \left[ (-\cos \omega t) \Big|_0^\pi \right] = \frac{I_m}{\pi} [-\cos \pi - (-\cos 0)]$$

$$= \frac{I_m}{\pi} [+1 - (-1)] \dots \cos \pi = -1$$

$$\therefore I_{DC} = \frac{-2I_m}{\pi}$$

Average DC Load Voltage ( $E_{DC}$ ) :

- The d.c. load voltage is,  $E_{DC} = I_{DC} R_L = \frac{2I_m R_L}{\pi}$

Substituting value of  $I_m$ ,  $E_{DC} = \frac{2 E_{sm} R_L}{\pi [R_f + R_s + R_L]}$

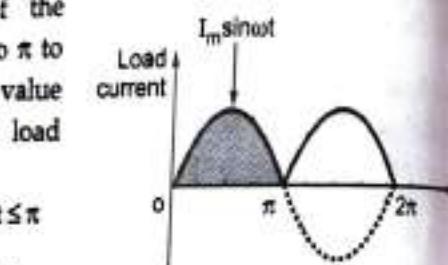


Fig. Q.28.1 Load current waveform

But as  $R_f$  and  $R_s \ll R_L$ , hence  $\frac{R_f + R_s}{R_L} \ll 1$ .

$$E_{DC} = \frac{2 E_{sm}}{\pi}$$

RMS Load Current ( $I_{RMS}$ ) : Mathematically it can be obtained as

$$I_{RMS} = \sqrt{\frac{1}{2\pi} \int_0^{2\pi} i_L^2 d(\omega t)} = \sqrt{2 \times \frac{1}{2\pi} \int_0^{\pi} [I_m \sin(\omega t)]^2 d(\omega t)}$$

The circuit has two half wave rectifiers similar in operation operating in two half cycles hence integration term is splitted as above.

$$I_{RMS} = I_m \sqrt{\frac{1}{\pi} \int_0^{\pi} \sin^2(\omega t) d(\omega t)} = I_m \sqrt{\frac{1}{\pi} \int_0^{\pi} \frac{1 - \cos 2\omega t}{2} d(\omega t)}$$

$$= I_m \sqrt{\frac{1}{\pi} \left[ \frac{\omega t}{2} - \frac{\sin(2\omega t)}{4} \right]_0^{\pi}} = I_m \sqrt{\frac{1}{\pi} \left[ \frac{\pi}{2} \right]}$$

$$I_{RMS} = \frac{I_m}{\sqrt{2}} \quad \text{and} \quad E_{L(RMS)} = I_{RMS} R_L = \frac{I_m}{\sqrt{2}} R_L$$

Q.29 Prove that the maximum theoretical efficiency of centre tap full wave rectifier is 81.2 %.

Ans. : • D.C. Power output =  $E_{DC} I_{DC} = I_{DC}^2 R_L$

$$P_{DC} = \left( \frac{2I_m}{\pi} \right)^2 R_L = \frac{4}{\pi^2} \frac{E_{sm}^2}{(R_f + R_s + R_L)^2} \times R_L = \frac{4}{\pi^2} I_m^2 R_L$$

$$\begin{aligned} \text{AC power input } P_{AC} &= I_{RMS}^2 (R_f + R_s + R_L) \\ &= \left( \frac{I_m}{\sqrt{2}} \right)^2 (R_f + R_s + R_L) = \frac{I_m^2 (R_f + R_s + R_L)}{2} \end{aligned}$$

• Substituting value of  $I_m$  we get,

$$P_{AC} = \frac{E_{sm}^2}{(R_f + R_s + R_L)^2} \times \frac{1}{2} \times (R_f + R_s + R_L) = \frac{E_{sm}^2}{2(R_f + R_s + R_L)}$$

$$\text{Rectifier efficiency } \eta = \frac{P_{DC} \text{ output}}{P_{AC} \text{ input}} = \frac{\frac{4}{\pi^2} I_m^2 R_L}{I_m^2 (R_f + R_s + R_L)} \\ = \frac{8 R_L}{\pi^2 (R_f + R_s + R_L)}$$

- But if  $R_f + R_s \ll R_L$ , neglecting it from denominator,

$$\eta_{max} = \frac{8 R_L}{\pi^2 (R_L)} = \frac{8}{\pi^2}$$

$$\% \eta_{max} = \frac{8}{\pi^2} \times 100 = 81.2 \%$$

**Q.30 Derive the ripple factor for centre tap full wave rectifier.**  
[SPPU : May-04, 10, Dec.-07, Marks 4]

**Ans. :** • The ripple factor is given by a general expression,

$$\text{Ripple factor} = \sqrt{\left[ \frac{I_{RMS}}{I_{DC}} \right]^2 - 1}$$

- For full wave  $I_{RMS} = I_m / \sqrt{2}$  and  $I_{DC} = 2I_m / \pi$  so substituting above,

$$\text{Ripple factor} = \gamma = \sqrt{\left[ \frac{I_m / \sqrt{2}}{2I_m / \pi} \right]^2 - 1} = \sqrt{\frac{\pi^2}{8} - 1} = 0.48$$

- This indicates that the ripple contents in the output are 48 % of the d.c. component which is much less than that for the half wave circuit.

**Important Points to Remember**

- PIV rating of diode in two diode full wave rectifier

$$\text{PIV of diode} = 2 E_{sm}$$

- Note that  $E_{sm}$  = Maximum value of a.c. voltage across half the secondary of transformer
- The ripple frequency in full wave rectifier is 2F Hz.
- The average TUF for full wave rectifier is 0.693.

**Q.31 In a centre tapped FWR, the rms half secondary voltage is 10 V. Assuming ideal diodes and load resistance of 2 kΩ. Find DC load current, ripple factor and efficiency of rectification.**

[SPPU : May-17, Marks 4]

**Ans. :**  $E_{s(RMS)} = 10 \text{ V}$ ,  $R_L = 2 \text{ k}\Omega$ . Ideal diodes

$$E_{sm} = \sqrt{2} E_{s(RMS)} = 10\sqrt{2} \text{ V}$$

$$I_m = \frac{E_{sm}}{R_L} = \frac{10\sqrt{2}}{2 \times 10^3} = 7.071 \text{ mA} \quad \text{Peak current}$$

$$I_{DC} = \frac{2I_m}{\pi} = \frac{2 \times 7.071}{\pi} = 4.502 \text{ mA}$$

$$I_{RMS} = \frac{I_m}{\sqrt{2}} = \frac{7.071}{\sqrt{2}} = 5 \text{ mA}$$

$$\text{Ripple factor} = \sqrt{\left[ \frac{I_{RMS}}{I_{DC}} \right]^2 - 1} = \sqrt{\left[ \frac{5}{4.502} \right]^2 - 1} = 0.483$$

$$P_{DC} = I_{DC}^2 R_L = 40.536 \text{ mW}, P_{AC} = I_{RMS}^2 R_L = 50 \text{ mW}$$

$$\% \eta = \frac{P_{DC}}{P_{AC}} \times 100 = \frac{40.536}{50} \times 100 = 81.07 \%$$

**1.19 : Bridge Rectifier**

**Q.32 Draw the circuit of bridge rectifier and explain its operation. Give the input and output waveforms.**  
[SPPU : Dec.-05, Marks 4]

**Ans. :** • The basic bridge rectifier circuit is shown in Fig. Q32.1.

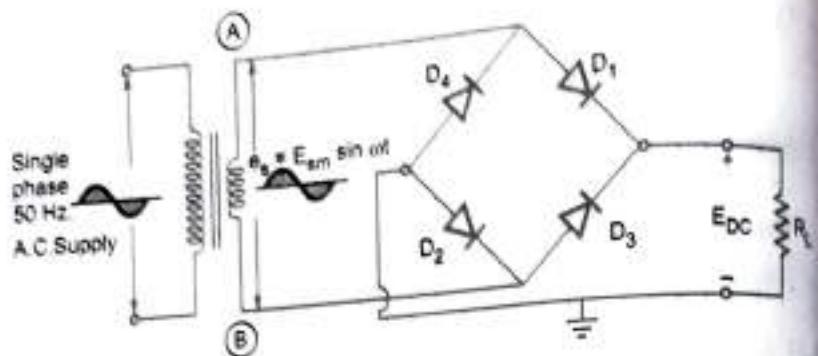


Fig. Q.32.1 Bridge rectifier circuit

- The bridge rectifier circuit is essentially a full-wave rectifier circuit, using four diodes, forming the four arms of an electrical bridge.
- To one diagonal of the bridge, the ac voltage is applied through a transformer if necessary and the rectified dc voltage is taken from the other diagonal of the bridge.

#### Operation of the circuit :

- Consider the positive half of ac input voltage. The point A of secondary becomes positive. The diodes D<sub>1</sub> and D<sub>2</sub> will be forward biased, while D<sub>3</sub> and D<sub>4</sub> reverse biased. The two diodes D<sub>1</sub> and D<sub>2</sub> conduct in series with the load and the current flows as shown in Fig. Q.32.2.

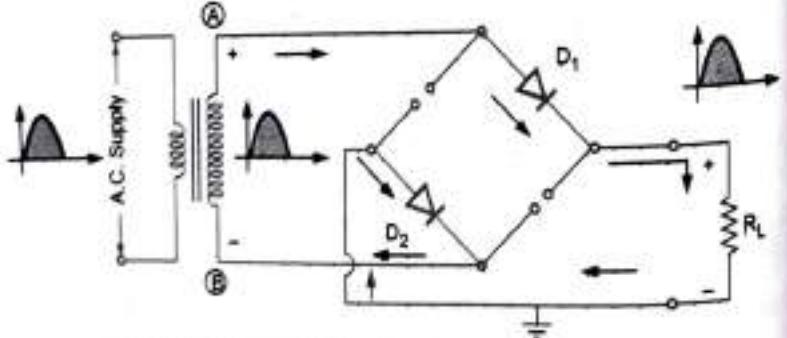


Fig. Q.32.2 Current flow during positive half cycle

- In the next half cycle, when the polarity of ac voltage reverses hence point B becomes positive diodes D<sub>3</sub> and D<sub>4</sub> are forward biased, while D<sub>1</sub> and D<sub>2</sub> reverse biased. Now the diodes D<sub>3</sub> and D<sub>4</sub> conduct in series with the load and the current flows as shown in Fig. Q.32.3.

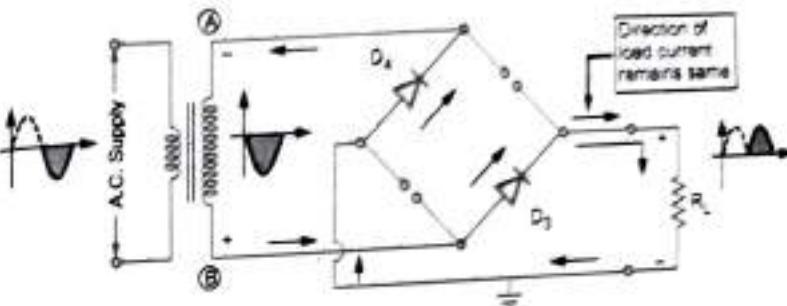


Fig. Q.32.3 Current flow during negative half cycle

- It is seen that in both cycles of ac, the load current is flowing in the same direction hence, we get a full-wave rectified output.
- The waveforms of load current and voltage are shown in the Fig. Q.32.4.

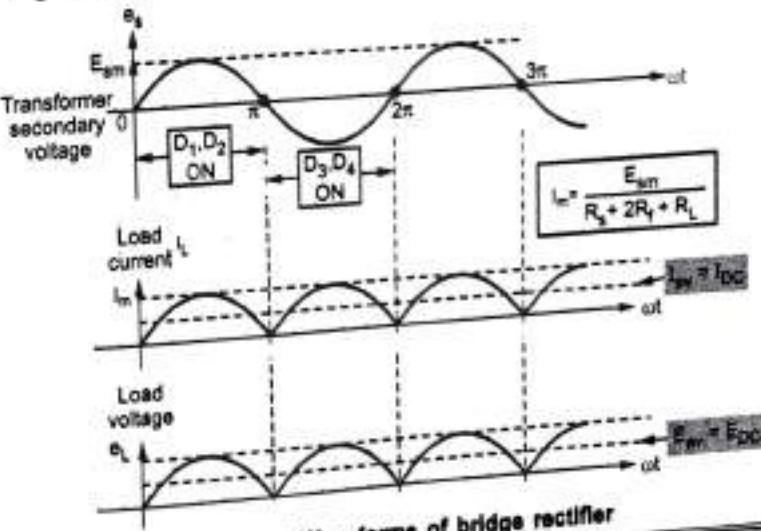


Fig. Q.32.4 Waveforms of bridge rectifier

**Important Points to Remember**

- For bridge rectifier, in each half cycle two diodes conduct hence in the various expressions  $R_f$  must be replaced by  $2R_f$ .

$$\bullet I_m = \frac{E_{sm}}{R_s + 2R_f + R_L}$$

$$\bullet E_{DC} = I_{DC} R_L = \frac{2E_{sm}}{\pi}, E_{RMS} = \frac{I_m}{\sqrt{2}} R_L = \frac{E_{sm}}{\sqrt{2}(R_s + 2R_f + R_L)} R_L$$

$$\bullet P_{DC} = I_{DC} R_L = \frac{4}{\pi^2} I_m^2 R_L \quad \text{and} \quad P_{AC} = I_{RMS}^2 (R_s + 2R_f + R_L) \\ = \frac{I_m^2 (2R_f + R_s + R_L)}{2}$$

$$\bullet \eta = \frac{8R_L}{\pi^2 (R_s + 2R_f + R_L)}, \% \eta_{max} = 81.2\%,$$

ripple factor  $\gamma = 0.48$ , T.U.F. = 0.812

- The  $E_{sm}$  is the maximum value of a.c. voltage across full secondary winding of the transformer used.

**Q.33** Determine r.m.s. value of secondary voltage of a transformer which provides 9 V d.c. output voltage when connected to a bridge rectifier. If the secondary winding has resistance of  $3\Omega$  and diode forward resistance is  $1\Omega$ , what will be the output voltage when  $90\Omega$  load is connected to the power supply?

[SPU : May-01, Marks 6, Dec.-06, Marks 4]

**Ans.:** For a bridge rectifier,

$$E_{DC} = \frac{2E_{sm}}{\pi} \quad \text{i.e.} \quad 9 = \frac{2E_{sm}}{\pi}$$

$$\therefore E_{sm} = \frac{9 \times \pi}{2} = 14.137 \text{ V}$$

$$\therefore E_{RMS} = \frac{E_{sm}}{\sqrt{2}} = \frac{14.137}{\sqrt{2}} = 10 \text{ V} \quad \dots \text{RMS value of secondary}$$

Now  $R_s = 3\Omega$ ,  $R_f = 1\Omega$ ,  $R_L = 90\Omega$

$$\therefore I_m = \frac{E_{sm}}{R_s + 2R_f + R_L} = \frac{14.137}{3+2+90} = 0.1488 \text{ A}$$

$$E_{DC} = I_m R_L = \frac{2E_{sm}}{\pi} \times R_L = \frac{2 \times 0.1488}{\pi} \times 90 = 8.9262 \text{ V}$$

- Q.34** For a bridge rectifier, the RMS secondary voltage of transformer is 12.7 V. Assume ideal diodes and  $R_L = 1k\Omega$ .

- Find (i) Peak current (ii) DC load current (iii) DC load voltage (iv) RMS current (v) Peak inverse voltage of diode & RMS voltage across load.

[SPU : Dec.-16, Marks 5]

**Ans.:**  $E_s(\text{RMS}) = 12.7 \text{ V}, R_L = 1k\Omega, E_{sm} = \sqrt{2} E_s(\text{RMS}) = 17.96 \text{ V}$

$$\text{i)} \quad I_m = \frac{E_{sm}}{R_L} = \frac{17.96}{1 \times 10^3} = 17.96 \text{ mA} \quad \text{Peak current}$$

$$\text{ii)} \quad I_{DC} = \frac{I_m}{\pi} = \frac{2 \times 17.96}{\pi} = 11.434 \text{ mA}$$

$$\text{iii)} \quad E_{DC} = I_{DC} R_L = 11.434 \times 10^{-3} \times 1 \times 10^3 = 11.434 \text{ V}$$

$$\text{iv)} \quad I_{RMS} = \frac{I_m}{\sqrt{2}} = \frac{17.96}{\sqrt{2}} = 12.7 \text{ mA}$$

$$\text{v)} \quad \text{PIV} = E_{sm} = 17.96 \text{ V}$$

$$\text{vi)} \quad \text{RMS voltage across load} = I_{RMS} \times R_L = 12.7 \text{ V}$$

**1.20 : Comparison of Rectifier Circuits**

**Q.35** Compare performance of half wave, full wave and bridge rectifier circuits with respect to the following parameters : (i)  $I_{DC}$  (ii)  $I_{rms}$  (iii) Efficiency (iv) Ripple factor (v) PIV (vi) TUF.

[SPU : Dec.-09, 12, 14, May-13, Marks 6]

**Ans.:** The comparison of rectifier circuits is :

Sr. No.	Parameter	Half Wave	Full Wave	Bridge
1.	Number of diodes	1	2	4
2.	Average D.C. current ( $I_{DC}$ )	$\frac{I_m}{\pi}$	$\frac{2I_m}{\pi}$	$\frac{4I_m}{\pi}$
3.	Average D.C. voltage ( $E_{DC}$ )	$\frac{E_{sm}}{\pi}$	$\frac{2E_{sm}}{\pi}$	$\frac{4E_{sm}}{\pi}$

	$\frac{I_m}{\sqrt{2}}$	$\frac{I_m}{\sqrt{2}}$	$\frac{I_m}{\sqrt{2}}$
4. RMS current ( $I_{RMS}$ )	$\frac{I_m}{\sqrt{2}}$	$\frac{I_m}{\sqrt{2}}$	$\frac{I_m}{\sqrt{2}}$
5. D.C. power output ( $P_{DC}$ )	$\frac{I_m^2 R_L}{\pi^2}$	$\frac{4}{\pi^2} I_m^2 R_L$	$\frac{4}{\pi^2} I_m^2 R_L$
6. A.C. power input ( $P_{AC}$ )	$\frac{I_m^2 (R_L + R_f + R_s)}{4}$	$\frac{I_m^2 (R_f + R_s + R_L)}{2}$	$\frac{I_m^2 (2R_f + R_s + R_L)}{2}$
7. Maximum rectifier efficiency ( $\eta$ )	40.6 %	81.2 %	81.2 %
8. Ripple factor ( $\gamma$ )	1.21	0.482	0.482
9. PIV rating of diode	$E_{sm}$	$2 E_{sm}$	$E_{sm}$
10. Ripple frequency	50 Hz	100 Hz	100 Hz
11. T.U.F.	0.287	0.693	0.812

### Part C : Special Purpose Diodes

#### 1.21 : Zener Diode

**Q.36 Explain the basic principle of zener diode. Draw its symbol.**

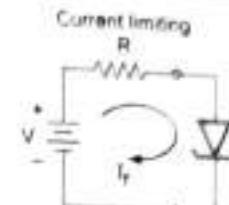
EEF [SPPU : Marks 6]

**Ans. :** • A zener diode is a silicon p-n junction semiconductor device which is operated in its reverse breakdown region.

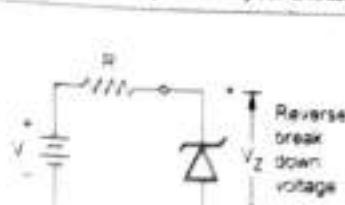
- The zener diodes are fabricated with precise breakdown voltage by controlling the doping level during manufacturing.
- When reverse biased, if the reverse current of zener diode limited using a series resistance the zener diode continues operate safely in reverse breakdown region.
- The Fig. Q.36.1 (a) shows the symbol of zener diode. Fig. Q.36.1 (b) shows the forward biasing of zener diode. It is similar to the conventional diode in forward biased.
- The Fig. Q.36.1 (c) shows the reverse biasing of zener diode. In reverse biased, it is operated in reverse breakdown region.



(a) Symbol



(b) Forward biasing



(c) Reverse biasing

**Fig. Q.36.1 Zener diode**

- In reverse breakdown region the voltage across it remains constant called zener voltage denoted as  $V_Z$ .

**Q.37 Draw and explain the V-I characteristics of a zener diode. What are the two breakdown mechanisms in a zener diode ?**

EEF [SPPU : Dec-18, Marks 6]

**Ans. :** • In the forward biased condition, the normal diode and the zener diode operate in similar fashion.

- But zener diode is designed to operate in reverse breakdown region hence its reverse V-I characteristics is important.
- When the reverse voltage is applied to zener diode, initially current is small, which is it's reverse saturation current.
- At a certain reverse voltage, the reverse breakdown occurs and current in the zener diode increases rapidly. The sharp change in the zener current is called knee or zener knee of the reverse characteristics.
- The reverse bias voltage at which the breakdown occurs is called zener breakdown voltage, denoted as  $V_Z$ . This value is carefully designed by controlling the doping level during manufacturing.
- The V-I characteristics of zener diode is shown in the Fig. Q.37.1.
- For zener diodes, practically two currents are specified. The  $I_{Zmin}$  is minimum current required through the zener diode to maintain its reverse breakdown operation.
- The  $I_{Zmax}$  is the maximum current which zener diode can take safely maintaining its reverse breakdown operation, i.e. constant  $V_Z$  across it. If reverse current exceeds this value, the diode may get damaged due to excessive power dissipation.

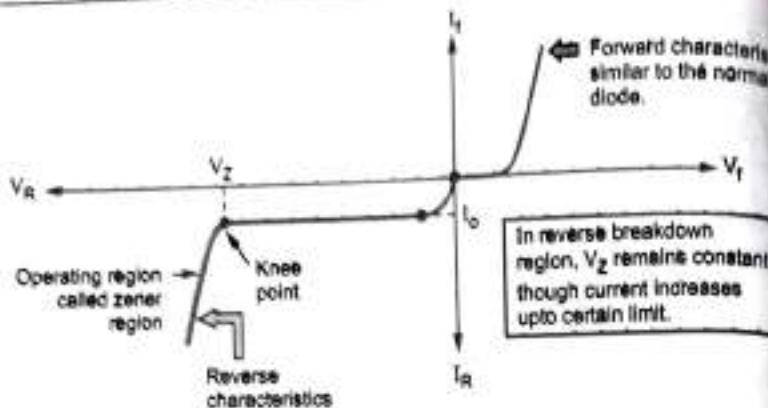


Fig. Q.37.1 V-I characteristics of zener diode

- The two breakdown mechanisms in zener diode are,
  - Zener breakdown
  - Avalanche breakdown

### 1.22 : Zener Diode as a Shunt Regulator

#### Important Points to Remember

- A voltage regulator circuit is the one which is designed to keep the output voltage of a power supply nearly constant under varying input voltage conditions and varying load conditions.

**Q.38** Describe with the help of neat circuit diagram the operation of zener voltage regulator under varying load and varying input conditions.  
[SPPU : Dec-04, 09, May-11, 13, 16, Marks 8]

**Ans. :** The zener diode has a characteristics that as long as the current through it is between  $I_{Z\min}$  and  $I_{Z\max}$ , the voltage across it is constant equal to zener voltage  $V_Z$ , as shown in the Fig. Q.38.1.

- As zener diode is connected in shunt with the load resistance, the output voltage is equal to the zener voltage.

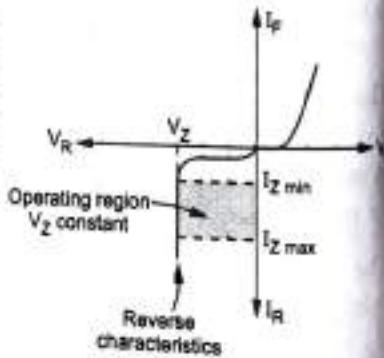


Fig. Q.38.1

- A shunt voltage regulator using zener diode is shown in the Fig. Q.38.2.
- From the Fig. Q.38.2 we can write,

$$V_0 = V_Z \text{ and } I = I_Z + I_L$$

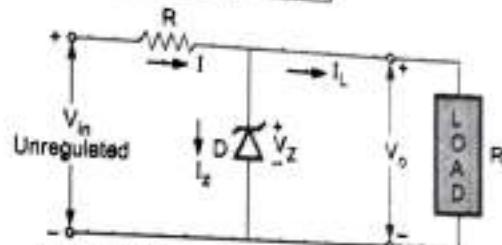


Fig. Q.38.2 Zener diode as a shunt regulator

#### Regulation with varying input voltage :

- The load current  $I_L = \frac{V_0}{R_L} = \frac{V_Z}{R_L} = \text{constant}$  and  $I = I_Z + I_L$ .
- If  $V_{in}$  increases, then the total current  $I$  increases. But  $I_L$  is constant as  $V_Z$  is constant. Hence the current  $I_Z$  increases to keep  $I_L$  constant.
- Similarly if  $V_{in}$  decreases, then current  $I$  decreases. But to keep  $I_L$  constant,  $I_Z$  decreases.
- But in both cases, as long as  $I_Z$  is between  $I_{Z\min}$  and  $I_{Z\max}$ , the  $V_Z$  i.e. output voltage  $V_0$  is constant.
- Thus the changes in input voltage get compensated and output is maintained constant.

#### Regulation with varying load :

- The input voltage is constant while the load resistance  $R_L$  is variable.
- As  $V_{in}$  is constant and  $V_0 = V_Z$  is constant, then for constant  $R$  the current  $I$  is constant.

$$\therefore I = \frac{V_{in} - V_Z}{R} \text{ constant} = I_L + I_Z$$

- If  $R_L$  decreases,  $I_L$  increases and to keep  $I$  constant  $I_Z$  decreases accordingly. But as long as it is between  $I_{Z\min}$  and  $I_{Z\max}$ , output voltage  $V_o$  will be constant.
- Similarly if  $R_L$  increases,  $I_L$  decreases and to keep  $I$  constant  $I_Z$  increases accordingly. But as long as it is between  $I_{Z\min}$  and  $I_{Z\max}$ , output voltage  $V_o$  will be constant.
- Thus the changes in the load get compensated and output is maintained constant.

**Q.39** For zener voltage regulator, If  $I_{Z\min} = 2 \text{ mA}$ ,  $I_{Z\max} = 20 \text{ mA}$ ,  $V_Z = 4.7 \text{ V}$ . Determine the range of input voltage over which output voltage remains constant.

$$R_S = 1 \text{ k}\Omega, R_L = 1 \text{ k}\Omega, Z_2 = 0 \Omega$$

[SPPU : Dec.-11, May-05, 12, Marks 6]

**Ans.** : The circuit is shown in the Fig. Q.39.1.

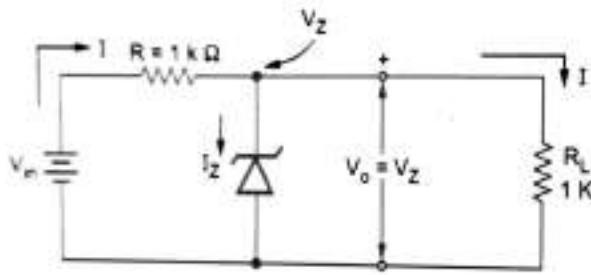


Fig. Q.39.1

$$\begin{aligned} I &= I_Z + I_L \\ I_L &= \frac{V_o}{R_L} = \frac{V_Z}{R_L} = \frac{4.7}{1 \times 10^3} = 4.7 \text{ mA} \end{aligned}$$

The load current is constant as  $V_o = V_Z$  is constant.

For  $V_{in} (\text{min})$ ,  $I_Z = I_{Z\min} = 2 \text{ mA}$

$$\therefore I = I_{Z\min} + I_L = 2 + 4.7 = 6.7 \text{ mA}$$

$$\begin{aligned} \text{But } I &= \frac{V_{in} (\text{min}) - V_Z}{R} \quad \text{i.e. } 6.7 \times 10^{-3} = \frac{V_{in} (\text{min}) - 4.7}{1 \times 10^3} \\ \therefore V_{in} (\text{min}) &= 11.4 \text{ V} \end{aligned}$$

For  $V_{in} (\text{max})$ ,  $I_Z = I_{Z\max} = 20 \text{ mA}$

$$I = I_{Z\max} + I_L = 20 + 4.7 = 24.7 \text{ mA}$$

$$\text{But } I = \frac{V_{in} (\text{max}) - V_Z}{R} \quad \text{i.e. } V_{in} (\text{max}) = 29.4 \text{ V}$$

Hence the range of input voltage is 11.4 V to 29.4 V.

**Q.40** For the given circuit (Fig. Q.40.1), If,  $V_Z = 12 \text{ V}$ ,  $I_{Z\min} = 1 \text{ mA}$  and  $I_{Z\max} = 50 \text{ mA}$ . Calculate Min. and Max.  $I_L$  and  $R_L$  for which zener diode maintains its regulation.

[SPPU : May-05, Dec.-10, 12, 17, Marks 6]

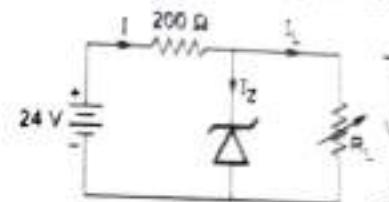


Fig. Q.40.1

$$\text{Ans. : } I = I_Z + I_L \quad \text{But } I = \frac{V_{in} - V_Z}{R} = \frac{24 - 12}{200} = 60 \text{ mA}$$

when  $I_Z = I_{Z\max}$ ,  $I_L = I_{L\min}$

$$\therefore 60 = I_{Z\max} + I_{L\min} = 50 + I_{L\min} \therefore I_{L\min} = 10 \text{ mA}$$

when  $I_Z = I_{Z\min}$ ,  $I_L = I_{L\max}$

$$\therefore 60 = I + I_{L\max} \quad \therefore I_{L\max} = 59 \text{ mA}$$

$$\therefore R_{L\min} = \frac{V_o}{I_{L\max}} = \frac{V_Z}{I_{L\max}} = \frac{12}{59 \times 10^{-3}} = 203.389 \Omega$$

$$\therefore R_{L\max} = \frac{V_o}{I_{L\min}} = \frac{V_Z}{I_{L\min}} = \frac{12}{10 \times 10^{-3}} = 1.2 \text{ k}\Omega$$

### 1.23 : Light Emitting Diode (LED)

**Q.41** What is LED ? Draw its symbol and explain its construction.

[SPPU : May-17, Marks 4]

**Ans.** : • A diode which emits light when forward biased is called a Light Emitting diode (LED).

- In LED three semiconductor layers on the substrate are used as shown in the Fig. Q41.1 (a).
- In between p type and n type region there exists a region called active region. This region is responsible for the emission of light.
- The LED emits light all the way around the layered structure. This layered structure is placed in a tiny reflective cup so that light gets reflected towards the desired exit direction. This cup type structure is shown in the Fig. Q41.1 (b).
- The symbol of the LED is shown in the Fig. Q41.1 (c).

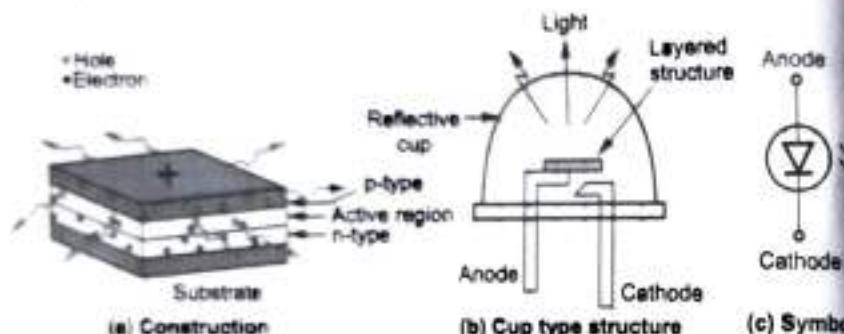


Fig. Q41.1 LED

**Q.42 Explain the working principle of LED.**EE<sup>2</sup> [SPPU : May-08, 10, 17, Dec.-09, Marks 4]

- Ans. :**
- The LED works on the principle of **electroluminescence**.
  - When a p-n junction is forward biased, the electrons in n region cross the junction and recombine with holes in p region.
  - The free electrons exist in the conduction band while the hole exist in the valence band.
  - The energy level of free electrons is higher than the energy level of the holes.
  - When electrons recombine with the holes, they move from conduction band to valence band which is at lower energy level.

- While moving, the difference between the energy levels of conduction band and valence band is released by the free electrons which appears in the form of light due to the special material used in the LED.
- The Fig. Q42.1 shows the principle of working of LED.

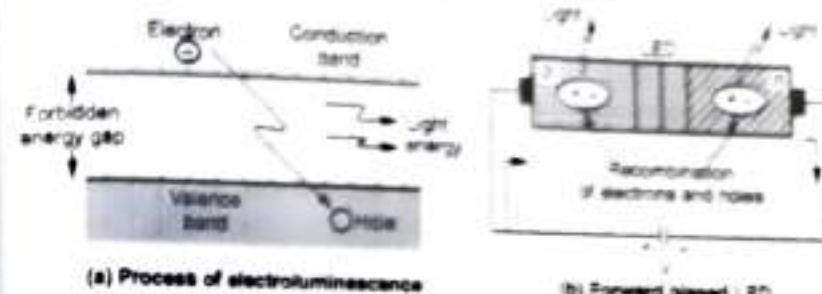


Fig. Q42.1 Principle of operation of LED

- The energy released depends on the forbidden gap energy which determines the wavelength and the colour of the emitted light.

**Q.43 State the advantages, disadvantages and applications of LED.****Ans. :**

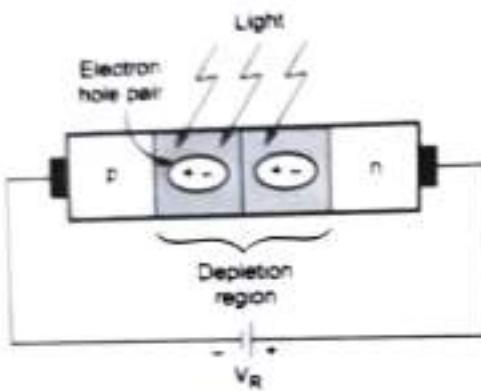
- The various **advantages** of LED are,
  - Small in size.
  - Very fast in operation.
  - Have long life.
  - Cheap and readily available.
  - Easy to interface with various other electronic circuits.
  - Light in weight.
  - Available in various colours.
- The various **disadvantages** of LED are,
  - Draws considerable current requiring frequent replacement of battery in low power battery operated devices.
  - Low luminous efficiency.
  - Temperature dependent characteristics.
  - Need large power for the operation than normal diode.
- The various **applications** of LED are,
  - All kinds of visual displays i.e. seven segment displays and alpha numeric displays. Such displays are commonly used in the watches and calculators.

2. In the optical devices such as optocouplers.
3. As on-off indicator in various types of electronic circuits.
4. Some LEDs radiate infrared light which is invisible. But some LEDs are useful in remote controls and applications like burglar alarm.

### 1.24 : Photodiode

**Q.44 Explain the working of photodiode along with its characteristics. Why photodiode is operated in reverse biased condition when operated as a optical detector?**  
 QB [SPPU : May-14, Dec-17, Marks 6]

**Ans. :** • The Fig. Q.44.1 (a) shows the construction of a photodiode and the Fig. Q.44.1 (b) shows the symbol of a photodiode.



(a) Construction



(b) Symbol

Fig. Q.44.1 Photodiode

- The glass lens is fixed over the junction through which the light is incident on the junction.
- Due to reverse biasing, the depletion region is wide.
- When the photons of light strike the depletion region, they give energy to the ions and generate the electron-hole pairs.
- The number of electron-hole pairs depend on the intensity of the light.

- Due to increased minority carriers, the reverse current increases, which is nothing but a photocurrent.
- More the light intensity, more is the number of electron-hole pairs and more is the photocurrent.
- The reverse current is directly proportional to the intensity of the light and is not dependent on the reverse voltage.
- The graph of  $V_R$  and reverse current  $I_R$  for various light intensities is called **characteristics of photodiode**.
- The Fig. Q.44.2 (a) shows the graph of reverse current and  $V_R$  for various intensities while the Fig. Q.44.2 (b) shows the graph of reverse current against light intensity.

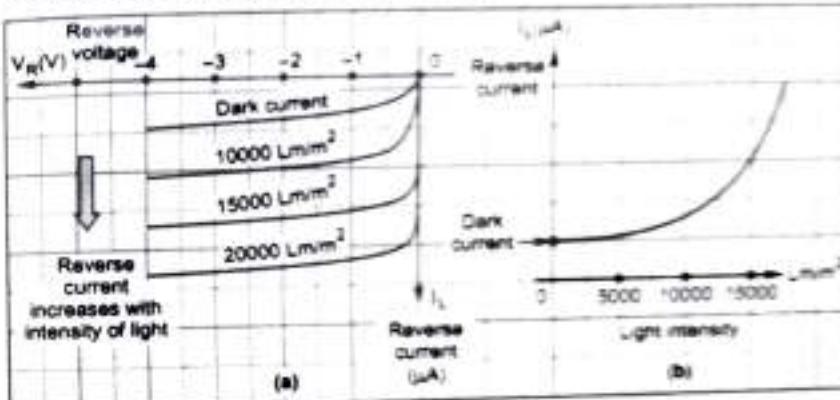


Fig. Q.44.2 Photodiode characteristics

- In reverse biased, the minority charge carriers control the current which are less in number. Thus the effect of light generated carriers is significant on the reverse current.
- In forward biased, there are large number of charge carriers thus the number of light generated charge carriers is comparatively less. Thus the applied voltage takes control of the current rather than the light. The effect of light is negligible in forward biased condition.
- Hence the photodiode is always used in reverse biased when used as an optical detector.

END... ↗

## UNIT - II

# 2

## Bipolar Junction Transistor

### Part A

#### 2.1 Construction, Type and Operation

##### Important Points to Remember

- Transistor is a three terminal device : base, emitter and collector.
- Transistor can be operated in three configurations : common base (CB), common emitter (CE) and common collector (CC).
- There are two types of transistors :
  - Unipolar junction transistor (UJT)
  - Bipolar junction transistor (BJT).
- Types of BJT : n-p-n and p-n-p

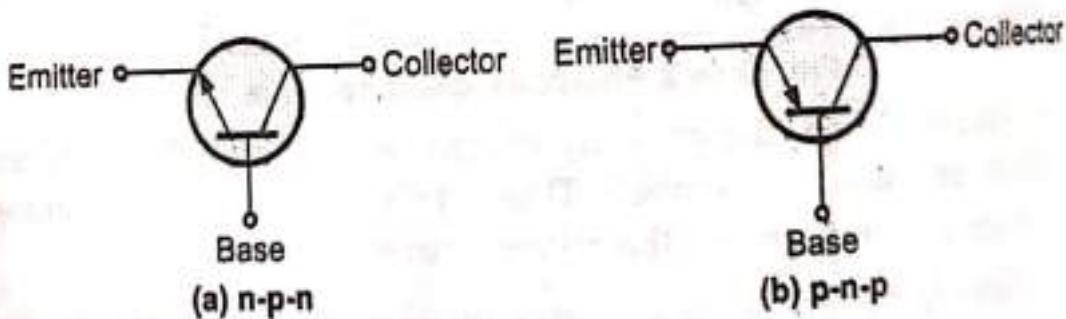


Fig. 2.1 Transistor symbols

- The process by which impurities are added to a pure semiconductor is called doping.

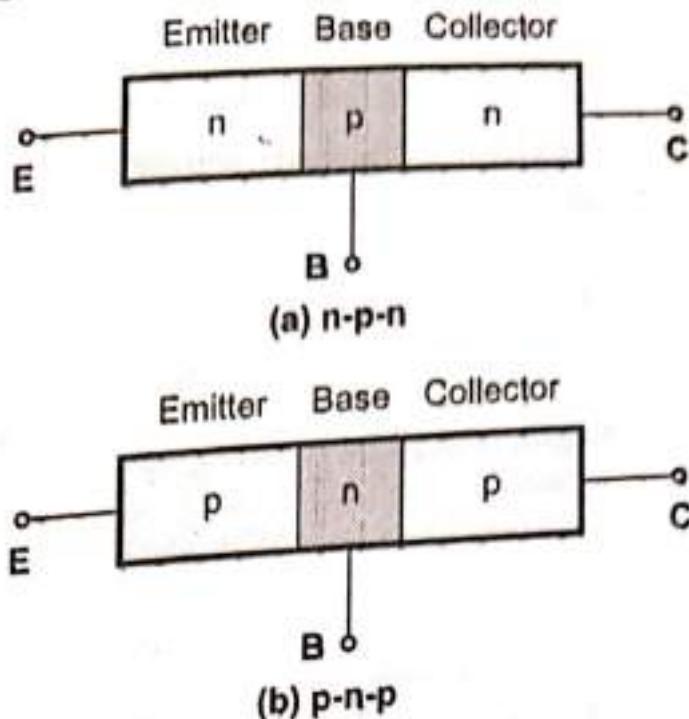


Fig. 2.2 Bipolar transistor construction

- Base : Lightly doped.
- Collector and emitter : heavily doped.
- Collector area > Emitter area > Base area
- Doping of emitter is slightly greater than collector.
- BJT has two junctions : EB and CB
- BJT has two depletion regions
- BJT works in one of the three regions :
  - 1. Active region
  - 2. Cut-off region and
  - 3. Saturation region
- The collector current is denoted as  $I_C$ .
- The base current is denoted as  $I_B$ .
- For both npn and pnp transistors,  $I_E = I_B + I_C$ .
- Since  $I_B$  is very small,  $I_E$  and  $I_C$  are nearly equal; however,  $I_E > I_C$ .

Q.1 State the biasing conditions required for the three regions of operation of a BJT.  
[SPPU : May-04, Marks 3]

Ans. : • Biasing is the process of applying external voltages to the transistor.

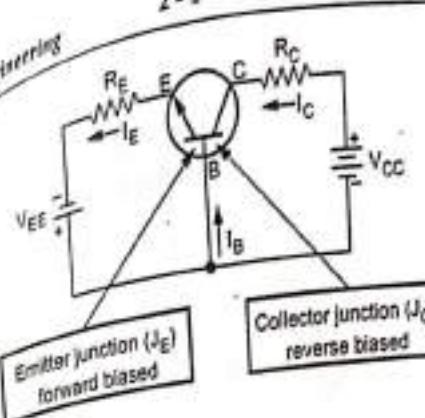
- Depending upon external bias voltage polarities applied to the junctions of transistor it can be operated in one of the four regions : 1) Active region 2) Cut-off region and 3) Saturation region 4) Inverse active.

Region	Emitter-base junction	Collector-base junction	Applications
Active	Forward biased	Reverse biased	Amplifier
Cut-off	Reverse biased	Reverse biased	Off-Switch
Saturation	Forward biased	Forward biased	On-Switch
Inverse active	Reverse biased	Forward biased	-

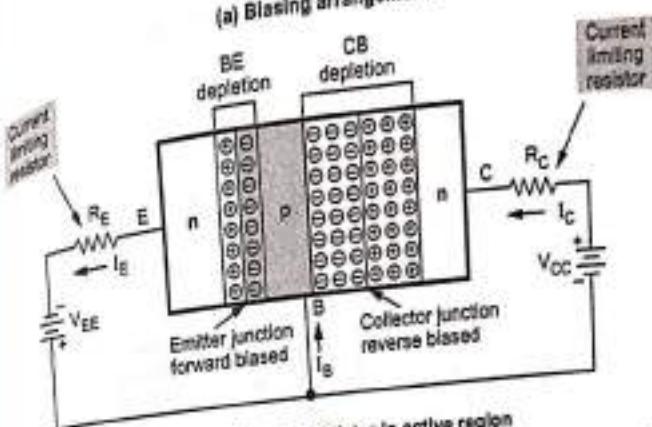
Table Q.1.1 Operating regions

- In order to operate transistor as an amplifier, it is necessary to bias it in the active region.
  - Q.2 Explain the working principle of npn transistor.
- Ans. :- Fig. Q.2.1 (a) shows the biasing arrangement for operating npn transistor in the active region.

- The supply voltage  $V_{EE}$ , forward biases the emitter junction ( $J_E$ ) and the supply voltage  $V_{CC}$  reverse biases the collector junction ( $J_C$ ).
- The base to emitter junction is forward biased by the d.c. source  $V_{EE}$ . Thus, the width of depletion region at this junction is small. The collector to base junction is reverse biased and hence width of depletion region at this junction is large, shown in Fig. Q.2.1 (b) (Fig. Q.2.1 (b) shows conventional currents)
- The forward biased EB junction causes the electrons in the n-type emitter to flow towards the base. This constitutes the emitter current  $I_E$ . As these electrons flow through the p-type base, they tend to combine with holes in p-region (base).



(a) Biasing arrangement



(b) Operation of npn transistor in active region

Fig. Q.2.1

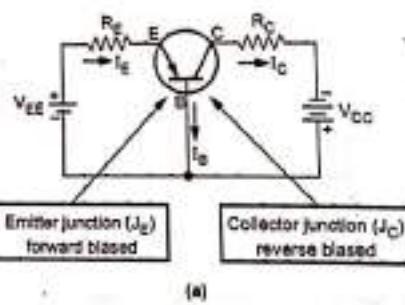
- Due to light doping, very few of the electrons injected into the base from the emitter recombine with holes to constitute base current,  $I_B$  and the remaining large number of electrons cross the base region and move through the collector region to the positive terminal of the external d.c. source. This constitutes collector current  $I_C$ .
- Forward biased EB junction also causes holes to flow from p-type base to n-type emitter. But as base is lightly doped holes become the minority carriers. Thus the electron flow constitutes the dominant current in an npn transistor.

- Since, the most of the electrons from emitter flow in the collector circuit and very few combine with holes in the base. Thus, the collector current is larger than the base current.
- The emitter current is summation of base current and collector current.

$$I_E = I_B + I_C$$

**Q.3 Explain the working principle of pnp transistor with the help of constructional diagram.**

**Ans. :** Fig. Q.3.1 (a) shows the biasing arrangement for operating pnp transistor in the active region.



(a)

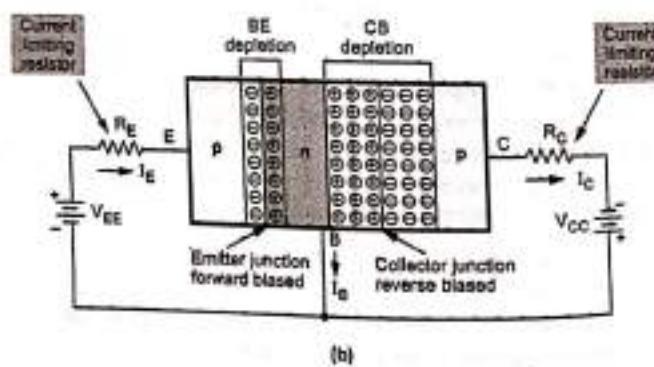


Fig. Q.3.1

- The pnp transistor has its bias voltages  $V_{EE}$  and  $V_{CC}$  reversed from those in the npn transistor, shown in Fig. Q.3.1 (b). (Fig. Q.3.1 (b) shows conventional currents). This is necessary to forward-bias the emitter-base junction and reverse-bias the collector base junction in pnp transistor.

The forward biased EB junction causes the holes in the p-type emitter to flow towards the base. This constitutes the emitter current  $I_E$ . As these holes flow through the n-type base, they tend to combine with electrons in n-region (base). As the base is very thin and lightly doped, very few of the holes injected into the base from the emitter recombine with electrons to constitute base current,  $I_B$ .

The remaining large number of holes cross the depletion region and move through the collector region to the negative terminal of the external dc source. This constitutes collector current  $I_C$ .

Forward biased EB junction also causes electrons to flow from n-type base to p-type emitter. But as base is lightly doped electron becomes the minority carriers. Thus the hole flow constitutes the dominant current in an pnp transistor.

Like npn transistor, in pnp transistor the emitter current is summation of base current and collector current.

$$I_E = I_B + I_C$$

**Q.4 Give comparison between pnp and npn transistors.**

**Ans. :**

No.	Parameter	npn transistor	pnp transistor
1.	Symbol		

2.	Carriers	Electrons are the majority carriers	Holes are the majority carriers
3.	Voltage applied and Current direction	A positive voltage is given to the collector terminal to produce a current flow from the collector to the emitter.	A positive voltage is given to the emitter terminal to produce a current flow from the emitter to the collector.
4.	$V_{CE}$	positive	negative
5.	Emitter arrow	pointed out	pointed in

## 2.2 CB, CE and CC Configurations, V-I Characteristics and Region of Operation

### Q.5 State the three transistor configurations.

Ans. : The transistor can be connected in a circuit in the following three configurations.

1. Common base configuration.

2. Common emitter configuration.

3. Common collector configuration.

**Key Point :** Regardless of circuit configuration, the base-emitter junction is always forward biased while the collector-base junction is always reverse biased, to operate transistor in active region.

### Q.6 Draw the neat circuit configuration of CB.

Ans. : The Fig. Q.6.1 shows the common base configuration. As shown in Fig. Q.6.1, in this configuration input is applied between emitter and base and output is taken from the collector and base. Here, base of the transistor is common to both input and output circuits and hence the name common base configuration. Common base configurations for both npn and pnp transistors are shown in Fig. Q.6.1 (a) and Q.6.1 (b), respectively.

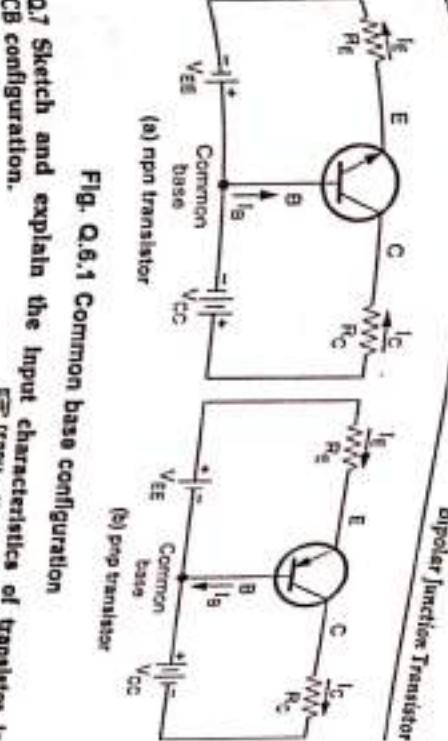


Fig. Q.6.1 Common base configuration

Q.7 Sketch and explain the Input characteristics of transistor in CB configuration. [SPU : May-05, Dec-07,10, Marks 3]

Ans. : It is the curve between  $i_E$  (emitter-base voltage) and input current  $i_E$  (emitter current) at constant collector-base voltage  $V_{CB}$ . The emitter current is taken along Y-axis and emitter base voltage along X-axis. Fig. Q.7.1 shows the input characteristics of a typical transistor in common-base configuration.

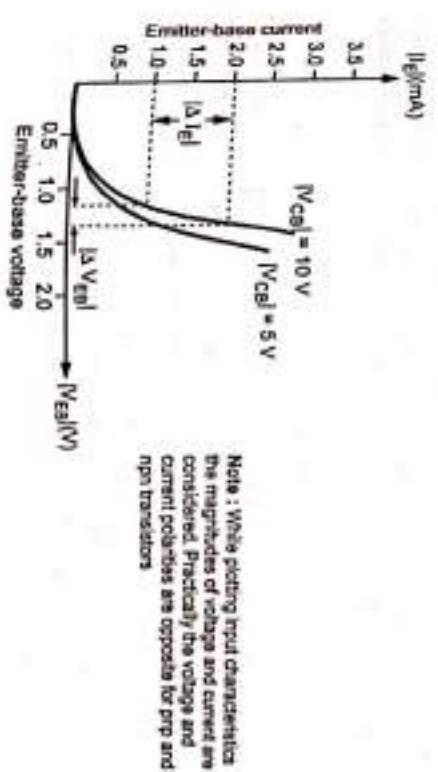


Fig. Q.7.1 Input characteristics of transistor in CB configuration

- From this characteristics we can observe the following important points :

- The input resistance is a ratio of change in emitter-base voltage ( $\Delta V_{EB}$ ) to the resulting change in emitter current ( $\Delta I_E$ ) at constant collector-base voltage ( $V_{CB}$ ). It is given by

$$r_i = \frac{\Delta V_{EB}}{\Delta I_E} \Big|_{V_{CB} = \text{constant}}$$

- After the cut-in voltage (barrier potential, normally 0.7 V for silicon and 0.3 V for germanium), the emitter current ( $I_E$ ) increases rapidly with small increase in emitter-base voltage ( $V_{EB}$ ). Thus, the input resistance is very small.
- It can be observed that there is slight increase in emitter current ( $I_E$ ) with increase in  $V_{CB}$ . This is due to change in the width of the depletion region in the base region under the reverse biased condition.

**Q.8 What is early effect? How can it account for the CB Input characteristics?** [SPPU : Dec.-10, Marks 4]

**Ans. :** • When reverse bias voltage  $V_{CB}$  increases, the width of depletion region also increases, which reduces the electrical base width. This effect is called as 'Early effect' or 'Base width modulation'.

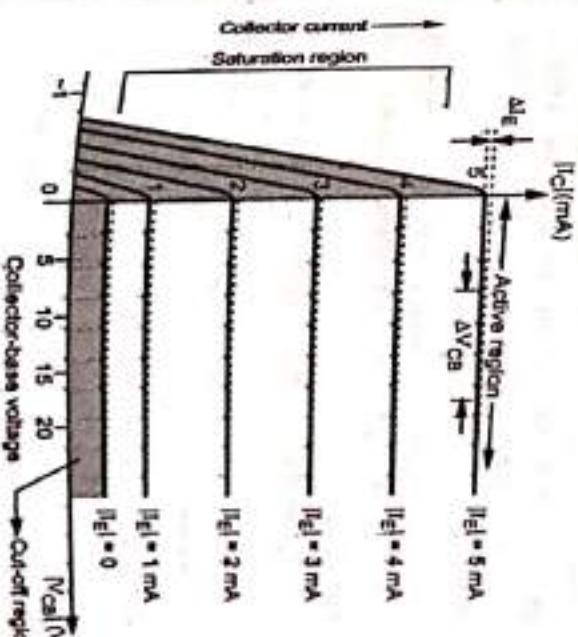
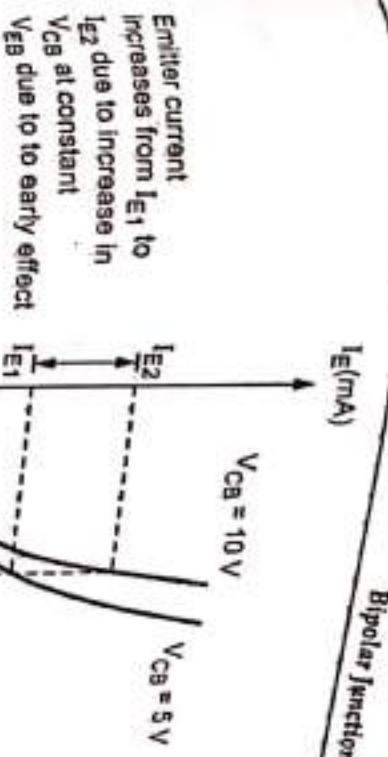
- This decrease in base width has two consequences.

- There is less chance for recombination within the base region. Hence the transport factor  $\beta^*$ , and also  $\alpha$ , increase with an increase in the magnitude of the collector junction voltage.
- The charge gradient is increased within the base, and consequently, the current of minority carriers injected across the junction increases. This increases emitter current slightly. Refer Fig. Q.8.1.

**Q.9 With a neat diagram explain the output characteristics of transistor in CB configuration.** [SPPU : May-05, 06, Dec-09, 10, Marks 3]

**Ans. :** It is the curve between collector current  $I_C$  and collector base voltage  $V_{CB}$  at constant emitter current  $I_E$ . The collector current is taken along Y-axis and collector-base voltage magnitude along X-axis. Fig. Q.9.1 shows the output characteristics of a typical transistor in common base configuration.

Fig. Q.8.1



Note : While plotting output characteristics the magnitudes of voltage and current are considered. Practically the voltage and current polarities are opposite for pnp and npn transistors.

From this characteristics we observe following points :

1. The output characteristics has three basic regions : Active cut-off and saturation.
2. Active region :
  - For the operation in the active region, the emitter-base junction ( $J_E$ ) is forward biased while collector base junction ( $J_C$ ) is reverse biased.
  - In this region, collector current  $I_C$  is approximately equal to the emitter current ( $I_E$ ) and transistor works as an amplifier.
  - In the active region, the collector current is essentially almost constant.

- The Dynamic output resistance is the ratio of change in collector base voltage ( $\Delta V_{CB}$ ) to the resulting change in collector current ( $\Delta I_C$ ) at constant emitter current ( $I_E$ ). It is given by

$$R_o = \left. \frac{\Delta V_{CB}}{\Delta I_C} \right|_{I_E=\text{constant}}$$

- The collector current  $I_C$  is almost independent on collector-base voltage  $V_{CB}$  and the transistor can be said to work as constant-current source. This provides very high dynamic output resistance.

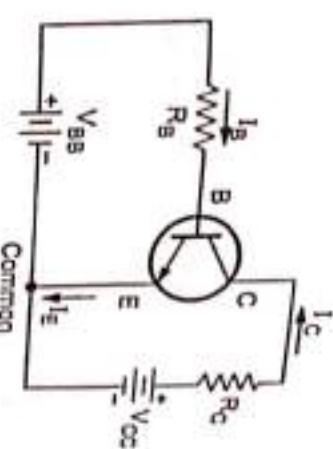
3. Saturation region : In this region, the emitter-base junction ( $J_E$ ) and collector base junction ( $J_C$ ) both are forward biased. Here,

4. Cut-off region : The region below the curve  $I_E = 0$  is known as cut-off region, where the collector current is nearly zero and the collector-base ( $J_C$ ) and emitter-base ( $J_E$ ) junctions of a transistor are reverse biased.

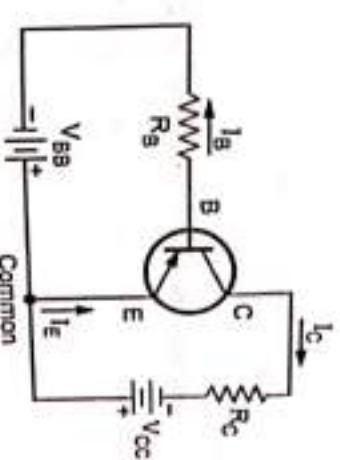
#### Q.10 Draw the neat circuit configuration of CE.

**Ans. :** • In this configuration input is applied between base and emitter, and output is taken from collector and emitter. Here emitter of the transistor is common to both, input and output circuits, and hence the name common emitter configuration

Common emitter configurations for both npn and pnp transistors are shown in Fig. Q.10.1 (a) and Q.10.1 (b), respectively. The input voltage in the CE configuration is the collector-emitter voltage ( $V_{BE}$ ) and the output voltage is the collector-emitter voltage ( $V_{CE}$ ). The input current is the base-emitter voltage ( $V_{BE}$ ) and the output current is  $I_C$ .



(a) npn transistor



(b) pnp transistor

Fig. Q.10.1 Common emitter configurations

Q.11 Sketch and explain the input characteristics of transistor in CE configuration.  
[PPU : Dec.-04, 05, May-14, Maths 6]

**Ans. :** • The input voltage in the CE configuration is the base-emitter voltage and the output voltage is the collector-emitter voltage. The input current is  $I_B$  and the output current is  $I_C$ .

- Input characteristics is the curve between input voltage  $V_{BE}$  (base-emitter voltage) and input current  $I_B$  (base current) at constant collector-emitter voltage,  $V_{CE}$ . The base current is taken along Y-axis and base-emitter voltage  $V_{BE}$  is taken along X-axis. Fig. Q.11.1 shows the input characteristics of a typical transistor in common-emitter configuration.

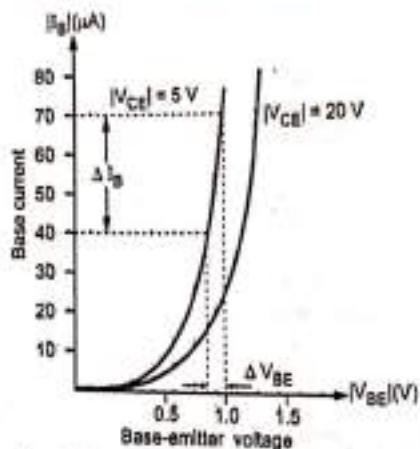


Fig. Q.11.1 Input characteristics of the transistor in CE configuration

From this characteristics we observe the following important points :

1. The input resistance is the ratio of change in base-emitter voltage ( $\Delta V_{BE}$ ) to the resulting change in base current ( $\Delta I_B$ ) at constant collector-emitter voltage  $V_{CE}$ . It is given by,

$$r_i = \left| \frac{\Delta V_{BE}}{\Delta I_B} \right|_{V_{CE}=\text{Constant}}$$

2. After the cut-in voltage, the base current ( $I_B$ ) increases rapidly with small increase in base-emitter voltage ( $V_{BE}$ ). Thus the dynamic input resistance is small in CE configuration.
3. For a fixed value of  $V_{BE}$ ,  $I_B$  decreases as  $V_{CE}$  is increased.

- Q.12 With a neat diagram explain output characteristics of an n-p-n transistor in CE-configuration. Indicate and explain three regions of operation.  
[SPPU : May-04, 14, 19, Dec-04, 05, 08, 10, Marks 6]

Ans.:

1. This characteristic shows the relation between the collector current  $I_C$  and collector voltage  $V_{CE}$  for various fixed values of  $I_B$ . This characteristic is often called collector characteristics. A typical family of output characteristics for an n-p-n transistor in CE configuration is shown in Fig. Q.12.1.

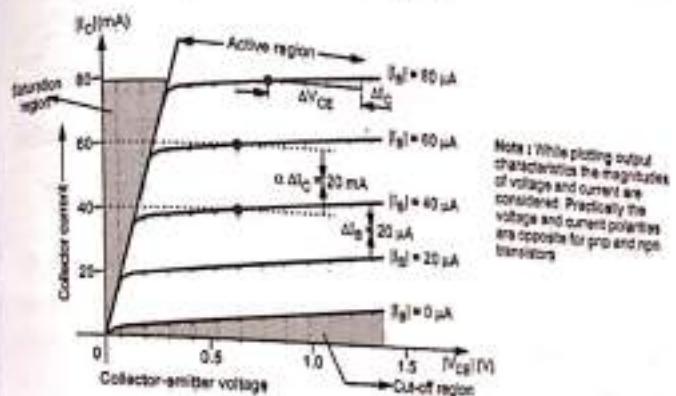


Fig. Q.12.1 Output characteristics of the transistor in CE configuration

2. The value of  $\beta_{dc}$  of the transistor can be found at any point on the characteristics by taking the ratio  $I_C$  to  $I_B$  at that point, i.e.  $\beta_{dc} = I_C / I_B$ . This is known as D.C. beta for the transistor.
3. From the output characteristics, we can see that change in collector-emitter voltage ( $\Delta V_{CE}$ ) causes the little change in the collector current ( $\Delta I_C$ ) for constant base current  $I_B$ . Thus the output dynamic resistance is high in CE configuration.

$$r_o = \left| \frac{\Delta V_{CE}}{\Delta I_C} \right|_{I_B=\text{Constant}} \text{ OR } \Delta I_B = 0$$

- The output characteristics of common emitter configuration consists of three regions : Active, Saturation and Cut-off.

#### Active Region :

- For the operation in the active region, the emitter-base junction ( $J_E$ ) is forward biased while collector base junction ( $J_C$ ) is reverse biased.

- The collector current rise more sharply with increasing  $V_{CE}$  in the linear region of output characteristics of CE transistor.

#### Saturation region :

- In this region, the emitter-base junction ( $J_E$ ) and collector base junction ( $J_C$ ) both are forward biased.

- The saturation value of  $V_{CE}$ , designated  $V_{CE(sat)}$ , usually ranges between 0.1 V to 0.3 V.

#### Cut-off region :

- The region below  $I_B = 0$  is the cut-off region of operation for the transistor. In this region, both the junctions of the transistor are reverse biased.

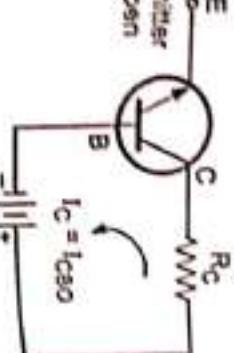
#### Q.13 Define $I_{C(NU)}$ and $I_{CBO}$ .

**Ans.:** In common base configuration, the collector current  $I_C$  is given by,

$$I_C = I_{C(NU)} + I_{CBO}$$

**Ques.:** It is an injected collector current due to number of electrons crossing the collector base junction.

**Ques.:** It is the reverse saturation current flowing due to the minority carrier between collector and base when the emitter is



**Fig. Q.13.1** CB configuration with base open

•  $I_{CBO}$  is negligible as compared to  $I_{C(NU)}$  and therefore we have

$$I_C = I_{C(NU)}$$

However, when emitter is open

$$I_C = I_{CBO}$$

Emitter open  
Collector to base leakage current

**Key Point :** The reverse saturation current,  $I_{CBO}$ , is temperature sensitive and it doubles for every  $10^{\circ}\text{C}$  rise in temperature.

#### Q.14 Define $\alpha$ .

**Ans.:** It is defined as the ratio of the collector current resulting from carrier injection to the total emitter current.

$$\therefore \alpha_{dc} = \alpha = \frac{I_{C(TN)}}{I_E} = \frac{I_C}{I_E} \quad ; \quad I_{CBO} \text{ is negligibly small}$$

Since  $I_C < I_E$  the value of  $\alpha_{dc}$  is always less than unity. It ranges from 0.95 to 0.995 depending on the thickness of the base region; larger the thickness of the base, smaller is the value of  $\alpha_{dc}$ .

#### Q.15 Define $\beta$ .

**QSPU : May-16, Dec-18, Marks 2]**

**Ans.:** • The  $\beta_{dc}$  is the ratio of output current  $I_C$  and input current  $I_B$  in common emitter configuration. It is common emitter amplification factor or current gain.

• It is given by,

$$\beta_{dc} = \frac{I_C}{I_B}$$

**QSPU : May-16, Dec-18, Marks 2]**

#### Q.16 Define $\gamma$ .

**Ans.:** The current gain of CC configuration is given by

$$\gamma = \frac{I_E}{I_B} = \frac{I_B + I_C}{I_B} = 1 + \frac{I_C}{I_B}$$

$$= 1 + \beta = 1 + \frac{\alpha}{1-\alpha} = \frac{1}{1-\alpha}$$

**Q.17 Derive the relationship between  $\alpha_{dc}$  and  $\beta_{dc}$ .**

**IE [SPRU : May-04, 07, 10, 16, Dec-04, 05, 08, Marks 3]**

**Ans. :**

$$\beta = \frac{I_C}{I_B}$$

We have,

$$I_E = I_C + I_B \text{ i.e. } I_B = I_E - I_C$$

$$\beta = \frac{I_C}{I_E - I_C} \quad ; \quad I_B = I_E - I_C$$

Dividing the numerator and denominator of R.H.S. of above equation by  $I_E$ , we get,

$$\beta = \frac{I_C/I_E}{I_E/I_E - I_C/I_E}$$

$$\beta = \frac{\alpha}{1-\alpha}$$

$$\therefore \alpha = \frac{I_C}{I_E}$$

$$\alpha = \frac{I_C}{I_E}$$

$$\alpha = \frac{I_C}{I_B + I_C}$$

We know that,  
 $I_E = I_B + I_C = \frac{I_C}{I_B + I_C}$   
 Dividing the numerator and denominator of R.H.S. of above equation by  $I_B$ , we get,

$$\alpha = \frac{I_C/I_B}{I_B/I_B + I_C/I_B}$$

$$\alpha = \frac{\beta}{1+\beta}$$

$$\therefore \beta = \frac{I_C}{I_B} \quad ; \quad \alpha = \frac{I_C}{I_E}$$

**Q.18 Calculate the values of  $I_C$  and  $I_E$  for a BJT with  $\alpha_{dc} = 0.97$  and  $I_B = 50 \mu A$ . Determine  $\beta_{dc}$  for the device.**

**IE [SPRU : May-02, Marks 4]**

**Ans. :** Given data :  $\alpha_{dc} = 0.97$ , and  $I_B = 50 \mu A$ .  
 To find :  $\beta_{dc}$ ,  $I_C$  and  $I_E$

$$\beta_{dc} = \frac{\alpha_{dc}}{1-\alpha_{dc}} = \frac{0.97}{1-0.97} = 32.33$$

$$I_C = \beta I_B = 32.33 \times 50 \mu A = 1.6165 mA$$

$$I_E = I_B + I_C = 50 \mu A + 1.6165 mA = 1.6665 mA$$

**Q.19 For a transistor in common emitter configuration, the reverse current is  $21 \mu A$ , whereas when the same transistor is connected in common base configuration, it reduces to  $1.1 \mu A$ . Calculate values of  $\alpha_{dc}$  and  $\beta_{dc}$  of the transistor.**

**IE [SPRU : May-05, Marks 4]**

**Ans. :** Given data :  $I_{CEO} = 1.1 \mu A$ ,  $I_{CEO} = 21 \mu A$ .  
 To find :  $\alpha_{dc}$  and  $\beta_{dc}$

$$I_{CEO} = (1 + \beta_{dc}) I_{CEO}$$

$$1 + \beta_{dc} = \frac{I_{CEO}}{I_{CEO}} = \frac{21 \mu A}{1.1 \mu A} = 19.09$$

$$\beta_{dc} = 18.09$$

$$\therefore \alpha_{dc} = \frac{\beta_{dc}}{1 + \beta_{dc}} = \frac{18.09}{1 + 18.09} = 0.9475$$

**Q.20 Calculate the  $\alpha_{dc}$  and  $\beta_{dc}$  for the given transistor for which  $I_C = 5 mA$ ,  $I_B = 50 \mu A$  and  $I_{CO} = 1 \mu A$ .**

**IE [SPRU : Dec-04, Marks 5]**

**Ans. :** Given data :  $I_C = 5 mA$ ,  $I_B = 50 \mu A$ ,  $I_{CO} = I_{CEO} = 1 \mu A$

To find :  $\alpha_{dc}$  and  $\beta_{dc}$ ,  $I_C = 5mA$ ,  $I_B = 50 \mu A$ ,  $I_{CO} = I_{CEO} = 1 \mu A$

$$I_C = \beta_{dc} I_B + (1 + \beta_{dc}) I_{CO}$$

$$5 \times 10^{-3} = \beta_{dc} \times 50 \times 10^{-6} + (1 + \beta_{dc}) \times 1 \times 10^{-6}$$

$$\therefore 5 \times 10^{-3} - 1 \times 10^{-6} = 51 \times 10^{-6} \beta_{dc}$$

$$\beta_{dc} = \frac{4.999 \times 10^{-3}}{51 \times 10^{-6}} = 98$$

$$\therefore \alpha_{dc} = \frac{\beta_{dc}}{1 + \beta_{dc}} = \frac{98}{1 + 98} = 0.9899$$

**Q.21 If  $\beta = 100$ , calculate the value of ' $\alpha$ '.**

**IE [SPRU : Dec-18, Marks 2]**

**Ans. :** Given data :  $\beta = 100$ .  
 To find :  $\alpha$

$$\alpha = \frac{\beta}{1 + \beta} = \frac{100}{1 + 100} = 0.99$$

**Q.22** Calculate values of  $I_C$  and  $I_E$  for BJT with  $\alpha_{dc} = 0.98$  and  $I_B = 50 \mu A$ . Also determine  $\beta_{dc}$  for BJT.

**ESE** [SPPU : May-16, Dec.-17, Marks 4]

**Ans. :** Given data :  $\alpha_{dc} = 0.98$  and  $I_B = 50 \mu A$

To find :  $\beta_{dc}$ ,  $I_C$  and  $I_E$

$$\beta = \beta_{dc} = \frac{\alpha_{dc}}{1-\alpha_{dc}} = \frac{0.98}{1-0.98} = 49$$

$$I_C = \beta I_B = 49 \times 50 \mu A = 2.45 \text{ mA}$$

$$I_E = I_B + I_C = 50 \mu A + 2.45 \text{ mA} = 2.5 \text{ mA}$$

**Q.23** Compare CB, CE and CC transistor configurations.

**ESE** [SPPU : May-15, Dec.-18, Marks 6]

**Ans. :**

Sr. No.	Characteristic	Common Base	Common Emitter	Common Collector
1.	Input resistance ( $R_I$ )	Very low ( $20 \Omega$ )	Low ( $1k\Omega$ )	High ( $500 k\Omega$ )
2.	Output resistance ( $R_O$ )	Very high ( $40 k\Omega$ )	High ( $50 \Omega$ )	Low ( $5 \Omega$ )
3.	Input current $I_E$	$I_B$	$I_B$	$I_E$
4.	Output current $I_C$	$I_C$	$I_B$	$I_E$
5.	Input voltage applied between Emitter and Base	Base and Emitter	Base and Collector	Collector and Emitter
6.	Output voltage taken between Collector and Base	Collector and Emitter	Emitter and Collector	Collector and Emitter
7.	Current amplification factor	$\alpha = \frac{I_C}{I_E}$	$\beta = \frac{I_C}{I_B}$	$\gamma = \frac{I_E}{I_B}$
8.	Current gain ( $A_I$ )	Less than unity	High (20 to few hundreds)	High (20 to few hundred)

9. Voltage gain ( $A_V$ )	Medium	Medium	Less than unity
10. Applications	As a input stage of multistage amplifier	For audio signal amplification	For impedance matching

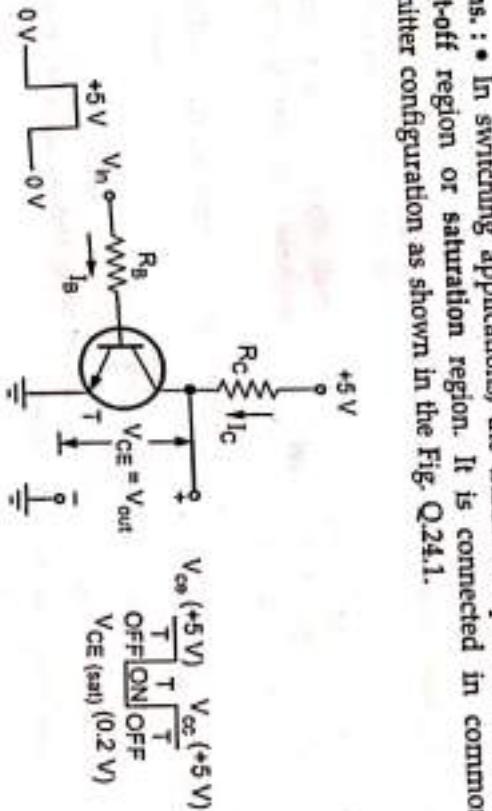
**Table Q.23.1 Comparison of CB, CE, CC Configurations**

### 2.3 BJT as Switch

**Q.24** Explain the working of a transistor as a switch.

**ESE** [SPPU : May-04,05,11,12; Dec-05,10,13,15,17, Marks 4]

**Ans. :** In switching applications, the transistor operates either in cut-off region or saturation region. It is connected in common emitter configuration as shown in the Fig. Q.24.1.



**Fig. Q.24.1 Transistor as a switch**

- In this circuit, when input is HIGH emitter junction is forward biased and base current flows. It is greater than  $I_C/\beta$ , hence transistor is operated in saturation. In saturation condition, voltage between collector and emitter,  $V_{CE(sat)}$  is typically 0.2 V to 0.3 V and hence transistor acts as closed switch.

- The minimum value of base current needed to operate transistor in saturation is

$$I_{B(\min)} = \frac{I_{C(\text{sat})}}{\beta}$$

- When input is LOW, emitter junction and collector junction both are reverse biased and hence transistor is operated in cut-off.  $I_B$  cut-off base current is zero and hence collector current is also zero, and transistor acts as an open switch.

- Applying KVL to the collector circuit we have,

$$V_{CC} = I_C R_C + V_{CE}$$

Since  $I_C = 0$ , we have

$$V_{OUT} = V_{CE} = V_{CC}$$

## 2.4 BJT as CE Amplifier

- Q.25 Explain the working of BJT as a CE amplifier.

[SPPU : Dec-14, Marks 6]

**Ans. :** A circuit which amplifies a small input signal to give magnified output signal having same frequency as that of input signal is called an amplifier.

The ratio of magnitude of output signal to input signal is called the voltage gain of the amplifier.

Fig. Q.25.1 shows the simplified CE amplifier circuit.

It is important to note that the values of  $R_B$  and  $R_C$  are chosen to operate transistor in active region.

As shown in Fig. Q.25.1 a small signal ac voltage,  $V_s$  is superimposed on the dc bias voltage  $V_{BB}$  by capacitive coupling.

The small ac input voltage produces an ac base current, which result in a much larger ac collector current.

$$\Delta I_B = \frac{\Delta V_{in}}{R_B}$$

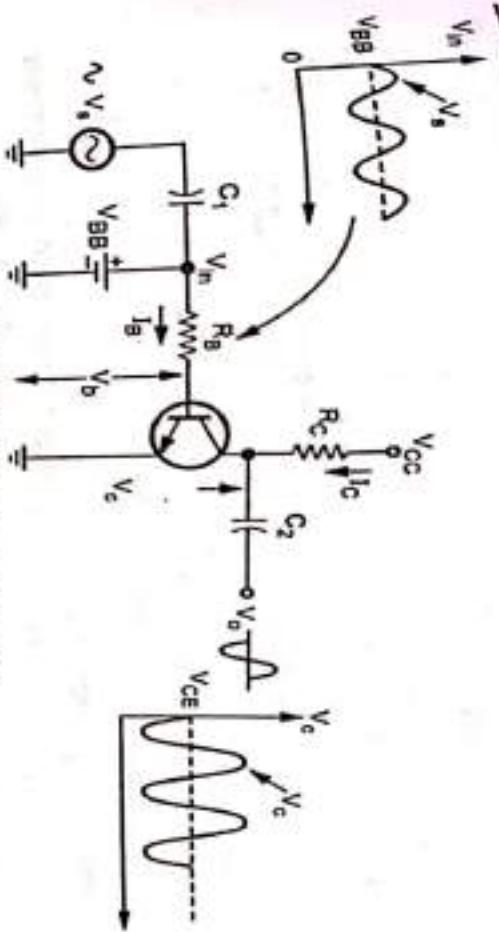


Fig. Q.25.1 CE amplifier circuit

- The corresponding change in collector current,  $I_C$  is given by

$$\Delta I_C = \beta \Delta I_B = \beta \frac{\Delta V_{in}}{R_B}$$

The change in the output voltage due to change in the input voltage is given by

$$\Delta V_o = \Delta I_C R_C \quad ; \quad \Delta I_C = \beta \frac{\Delta V_{in}}{R_B}$$

$$= \beta \frac{\Delta V_{in} R_C}{R_B} = \frac{\beta R_C}{R_B} \Delta V_{in}$$

$$\therefore A_V = \frac{\Delta V_o}{\Delta V_{in}} = \frac{\beta R_C}{R_B}$$

- Above expression shows that, for a small change in input signal ( $V_{in}$ ) there is a large change in the output signal ( $V_o$ ).

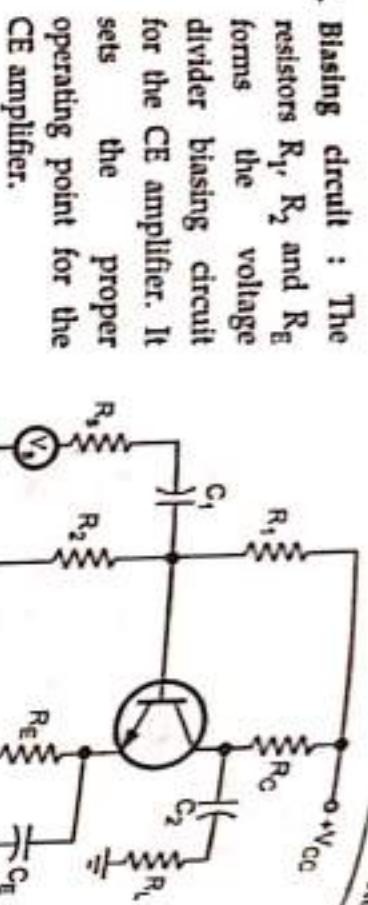
- Thus, we can say that, the CE amplifier operated in the active region acts as an voltage amplifier.

- Q.26 Explain with a circuit diagram a single stage common emitter amplifier. State the function of each component in the circuit.

[SPPU : Dec-12, Marks 6]

**Ans. :** Fig. Q.26.1 shows the practical circuit of common emitter transistor amplifier. It consists of different circuit components. The functions of these components are as follows :

1. **Biasing circuit :** The resistors  $R_1$ ,  $R_2$  and  $R_E$  forms the voltage divider biasing circuit for the CE amplifier. It sets the proper operating point for the CE amplifier.



2. **Input capacitor  $C_1$  :** This capacitor couples the signal to the base of the transistor. It blocks any d.c. component present in the signal and passes only a.c. signal for amplification. Because of this biasing conditions are maintained constant.

3. **Emitter bypass capacitor  $C_E$  :** An emitter bypass capacitor  $C_E$  is connected in parallel with the emitter resistance,  $R_E$  to provide a low reactance path to the amplified a.c. signal. If it is not inserted, the amplified a.c. signal passing through  $R_E$  will cause a voltage drop across it. This will reduce the output voltage, reducing the gain of the amplifier.

4. **Output coupling capacitor  $C_2$  :** The coupling capacitor  $C_2$  couples the output of the amplifier to the load or to the next stage of the amplifier. It blocks d.c. and passes only a.c. part of the amplified signal.

**Need for  $C_1$ ,  $C_2$  and  $C_E$ :**

We know that, the impedance of capacitor is given as,

$$X_C = \frac{1}{2\pi fC}$$

Thus, at signal frequencies all the capacitors have extremely small impedance and it can be treated as an a.c. short circuit. For bias/d.c. conditions of the transistor all the capacitors act as a d.c. open circuit. With this knowledge we will see the importance of  $C_1$ ,  $C_2$  and  $C_E$ .

## Metal Oxide Semiconductor Field Effect Transistors (MOSFET)

### 2.5 Introduction and Types

#### Important Points to Remember

- MOSFET stands for Metal Oxide Semiconductor Field Effect Transistor.
- The gate of the MOSFET is insulated from the channel by a silicon dioxide ( $\text{SiO}_2$ ) layer.
- MOSFETs are also called IGFETs.



Conventional symbol



Conventional symbol

- (a) Symbols for n-channel enhancement type MOSFETs
- (b) Symbols for p-channel enhancement type MOSFETs

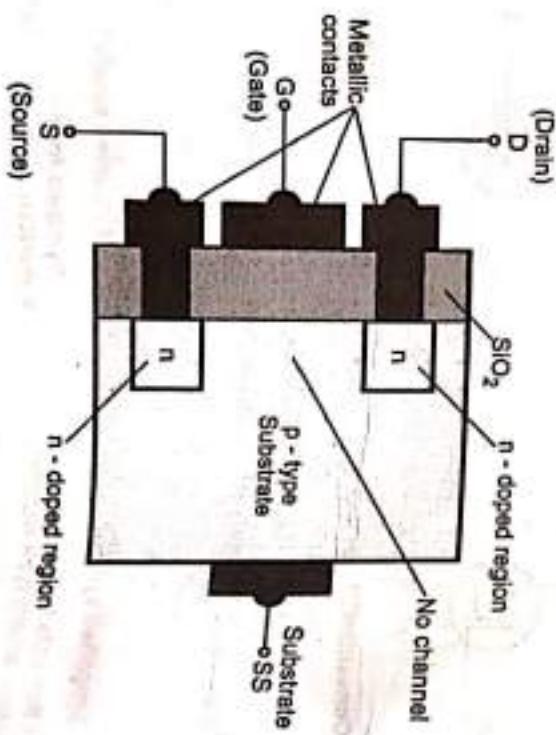
- MOSFET is a voltage controlled device. Input voltage  $V_{GS}$  controls drain current  $I_D$ .
- In MOSFET current flows only due to majority carriers and hence unipolar device.
- MOSFET has very high input resistance as compare to BJT.

## 2.6 Construction and Operation

- Q.27 Explain the construction of n-channel enhancement type MOSFET.**  
[SPPU : Dec-09, 11, 12, May-12, Marks 4]

Ans. : • Fig. Q27.1 shows the basic construction of n-channel enhancement type MOSFET.

- Two highly doped n-regions are diffused into a lightly doped p-type substrate. The source and drain are taken out through metallic contacts to n-doped regions as shown in the Fig. Q27.1.



**Fig. Q.27.1 n-channel enhancement type MOSFET**

- Q.28 Explain the working of n-channel enhancement MOSFET.**  
[SPPU : May-12, Dec-11, 12, Marks 3]

Ans. : • Enhancement type of MOSFET operates only in the enhancement mode and has no depletion mode.

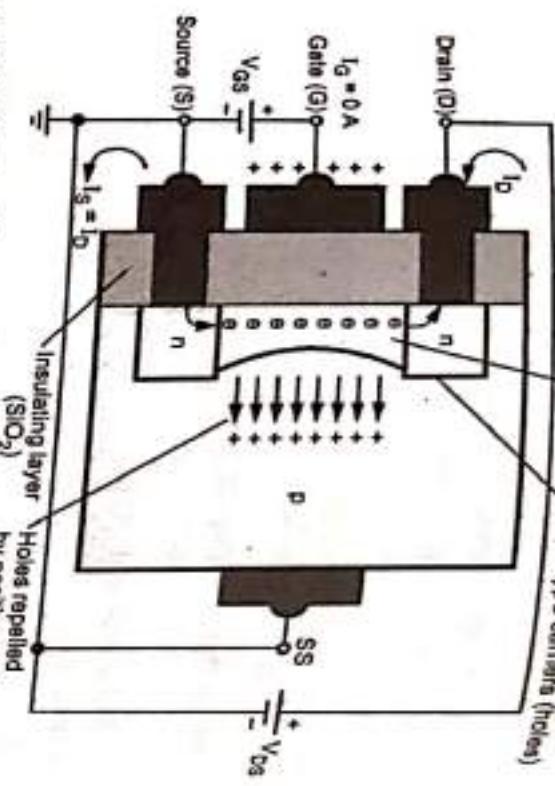
- $V_{GS} = 0$  : On application of drain to source voltage  $V_{DS}$  and keeping gate to source voltage zero by directly connecting gate terminal to the source terminal, practically zero current flows, quite different from the depletion type MOSFET.

- $V_{GS} > 0$  : If we increase magnitude of  $V_{GS}$  in the positive direction, the concentration of electrons near the  $\text{SiO}_2$  surface increases. At a particular value of  $V_{GS}$  there is a measurable current flow between drain and source. This minimum value of  $V_{GS}$  at which  $I_D$  starts flowing is called threshold voltage denoted by  $V_T$ .
- Thus we can say that in an enhancement type n-channel MOSFET, a positive gate voltage above a threshold value induces a channel and hence the drain current by creating a thin layer of negative charges in the substrate region adjacent to the  $\text{SiO}_2$  layer, as shown in the Fig. Q28.1.
- The conductivity of the channel is enhanced by increasing the gate to source voltage and thus pulling more electrons into the channel. For any voltage below the threshold value, there is no

- The channel between two n-regions is absent in the enhancement type MOSFET. The  $\text{SiO}_2$  layer is still present to isolate the gate from the region between the drain and source, but now it is simply separated from a section of the p-type material.
- It differs in construction from the depletion MOSFET in that it has no physical channel.

Electrons attracted to positive gate  
(induced n - channel)

Region depleted of  
p - type carriers (holes)



**Fig. Q28.1 Channel formation in the n-channel enhancement type MOSFET**

- Since the channel does not exist with  $V_{GS} = 0 \text{ V}$  and "enhanced" by the application of a positive gate to source voltage, this type of MOSFET is called an enhancement type MOSFET.

### 2.7 V-I Characteristics and Operating Regions

- Q.29 Draw and explain drain characteristics of an n-channel enhancement type MOSFET** [SPPU : Dec-11, May-12, 14, Marks 4]

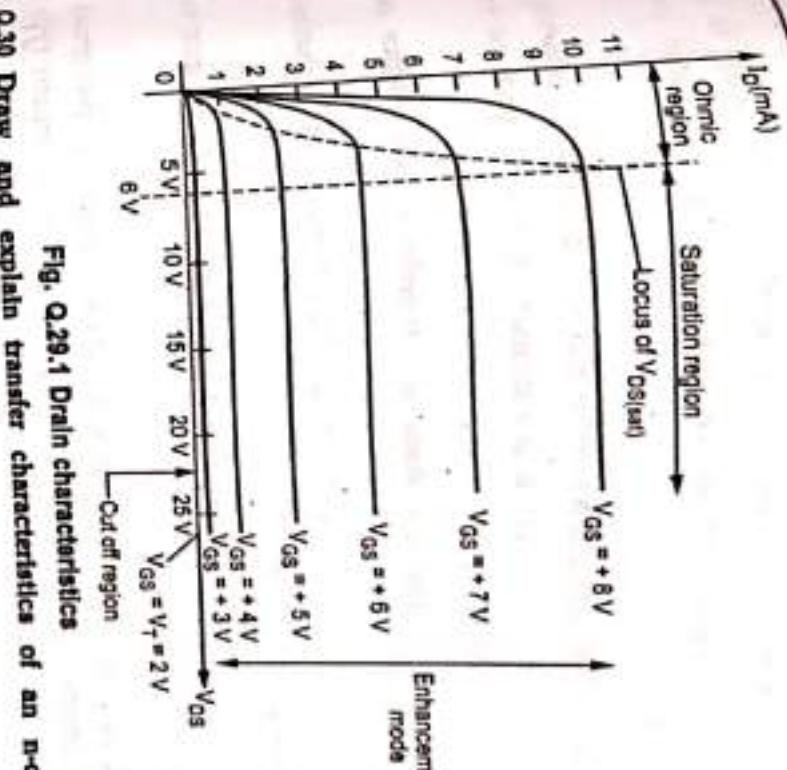
**Ans. :** Fig. Q.29.1 shows the drain characteristics for n-channel enhancement-type MOSFET.

- The drain characteristics of a MOSFET are drawn between the drain current  $I_D$  and the drain source voltage  $V_{DS}$ . Typical drain n-channel MOSFET are shown in fig Q.29.1.

- Looking at Fig. Q.29.1 we can say that as  $V_{GS}$  increases beyond the threshold level, the density of free carriers (electrons) in the induced channel increases, increasing the drain current.

- However, at some point of  $V_{DS}$  for constant  $V_{GS}$ , the drain current reaches a saturation level.

Basic Electronics Engineering

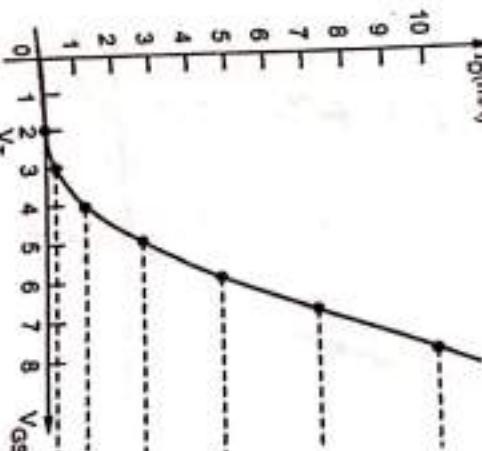


**Fig. Q29.1 Drain characteristics**

- Q.30 Draw and explain transfer characteristics of an n-channel enhancement type MOSFET**

**Ans. :** Fig. Q.30.1 shows the transfer characteristic for n-channel enhancement type MOSFET.

**Fig. Q30.1 Transfer characteristics**



**Fig. Q30.1 Transfer characteristics**

- For an n-channel enhancement type MOSFET it is totally in the positive  $V_{GS}$  region and as we know  $I_D$  does not flow until  $V_{GS(\text{th})} = V_T$ .

- The relation between drain current and  $V_{GS}$  is given by following equation  $I_D = K(V_{GS} - V_T)^2$ .  $K$  is a constant and it depends on the particular MOSFET.

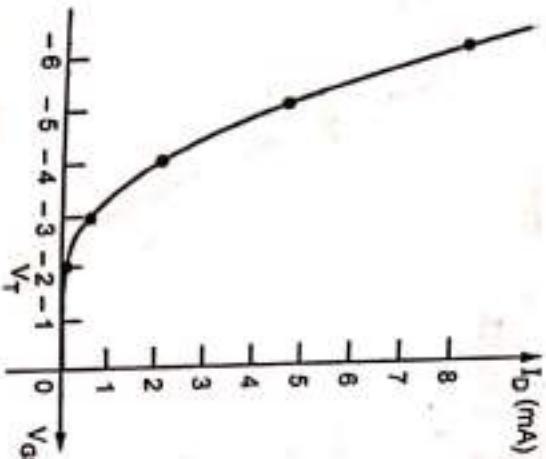
- Q.31 Draw and explain the drain and transfer characteristics of p-channel MOSFET.**

**Ans.:** Fig. Q.31.1 shows the drain characteristics of enhancement type MOSFET.

- Here, drain current increases with increase in the negative gate to source ( $V_{GS}$ ) voltage.

- Fig. Q.31.1 (a) shows the transfer characteristics of p-channel enhancement type MOSFET. In the p-channel enhancement type

(a)



(b)

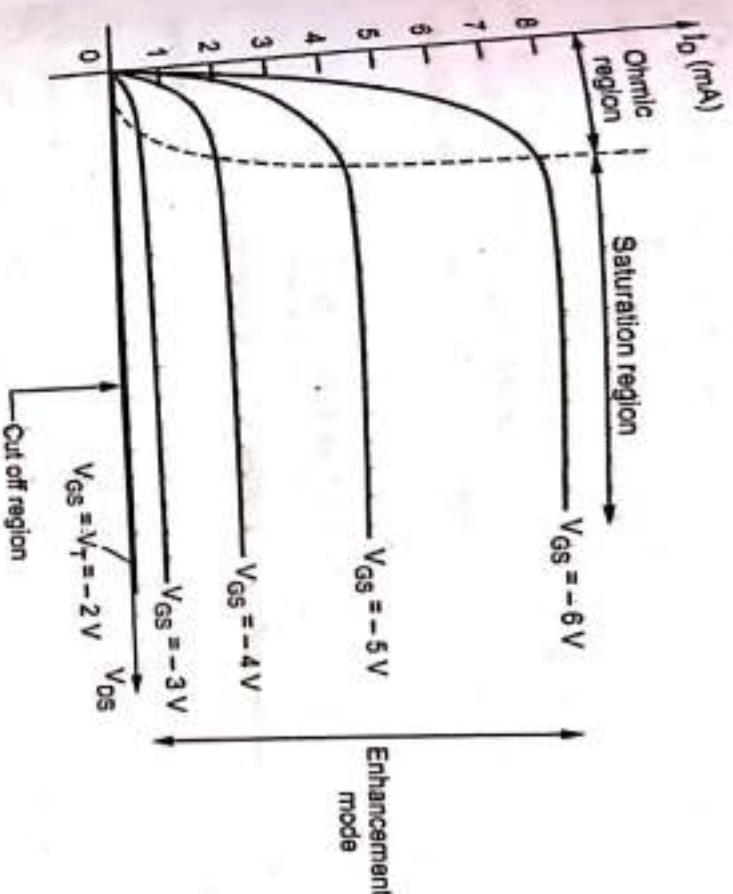


Fig. Q.31.1 Drain and transfer characteristics for p-channel Enhancement-type MOSFET

MOSFET, the transfer characteristic is a mirror image about the  $I_D$  axis (y axis) of the transfer characteristics of n-channel depletion type MOSFET, since the  $V_{GS}$  is negative.

- Q.32 Explain the operating regions of E-MOSFET.**

**Ans.:** As evident from characteristics curves, an E-MOSFET has three operating regions :

- Cut-off region 2. Ohmic or linear region 3. Saturation region

- Cut-off Region - with  $V_{GS} < V_{\text{threshold}}$  the gate-source voltage is much lower than the transistors threshold voltage so the MOSFET transistor is switched "fully-OFF" thus,  $I_D = 0$ , with the transistor acting like an open switch regardless of the value of  $V_{DS}$ .

(a)

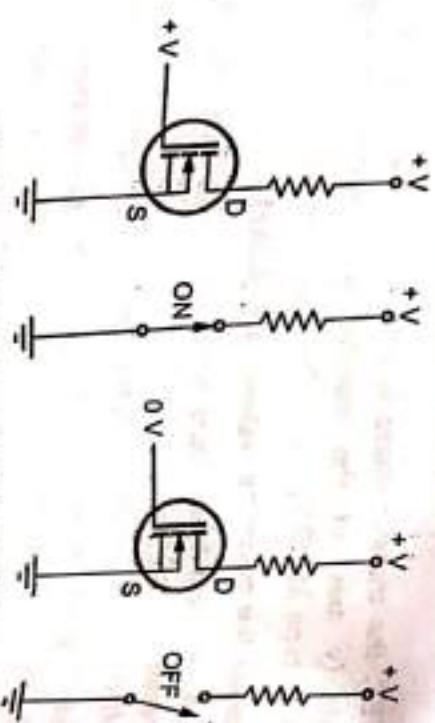
2. **Linear (Ohmic) Region** - with  $V_{GS} > V_{threshold}$  and  $V_{DS} < V_{GS}$  the transistor is in its constant resistance region behaving as a voltage-controlled resistance whose resistive value is determined by the gate voltage,  $V_{GS}$  level.
3. **Saturation Region** - with  $V_{GS} > V_{threshold}$  and  $V_{DS} > V_{GS}$  the transistor is in its constant current region and is therefore "fully-ON". The Drain current  $I_D = \text{Maximum}$  with the transistor acting as a closed switch.

## 2.8 MOSFET as a Switch

- Q.33 Explain the working of E-MOSFET as a switch.**

**Ans. :** • E-MOSFETs are generally used for switching applications because of their threshold characteristic,  $V_{GS(th)}$ .

- When the gate-to-source voltage is less than the threshold value, the MOSFET is off. When the gate-to-source voltage is greater than the threshold value, the MOSFET is on. When  $V_{GS}$  is varied between  $V_{GS(th)}$  and  $V_{GS(ON)}$ , the MOSFET is being operated as a switch, as illustrated in Fig. Q.33.1.



**Fig. Q.33.1 (b) p-channel MOSFET and switch equivalent**

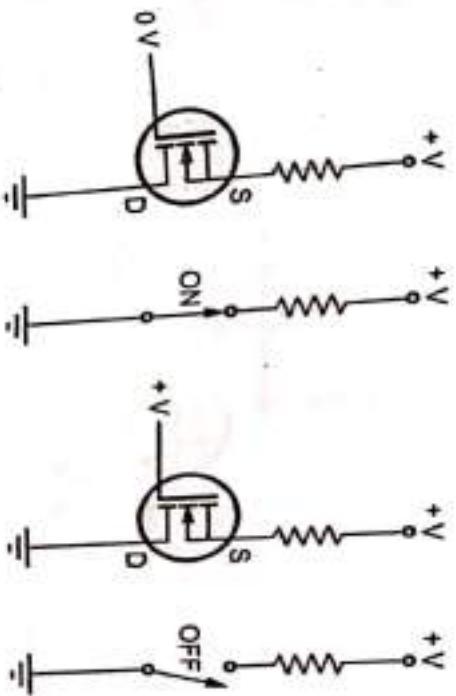
## 2.9 MOSFET as an Amplifier

- Q.34 Explain the operation of MOSFET as an amplifier with the help of suitable circuit diagram and waveform.**

**Ans. :** • Fig. Q.34.1 shows a common source amplifier using n-channel D-MOSFET. Here, the source terminal is common to the input and output terminals and hence the name.

- The amplifier circuit is positive biased (i.e.  $V_{GS} = 5$  V) with an a.c. source coupled to the gate through the coupling capacitor  $C_1$ .
- When a.c. input signal is absent, the gate is at 5 V d.c. and the source terminal is grounded, thus  $V_{GS} = 5$  V.
- When a.c. input signal is applied,  $V_{GS}$  swings above and below its 5 V value, producing a swing in drain current  $I_D$ .
- During the positive half-cycle of the signal, the positive voltage on the gate increases. This increases the channel conductivity and hence the drain current.
- During the negative half-cycle of the signal, the voltage on the gate decreases. This decreases the conductivity and hence the drain current.

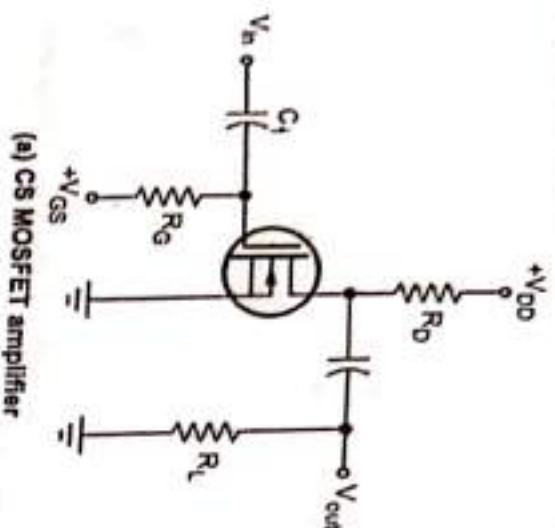
(a) n-channel MOSFET and switch equivalent



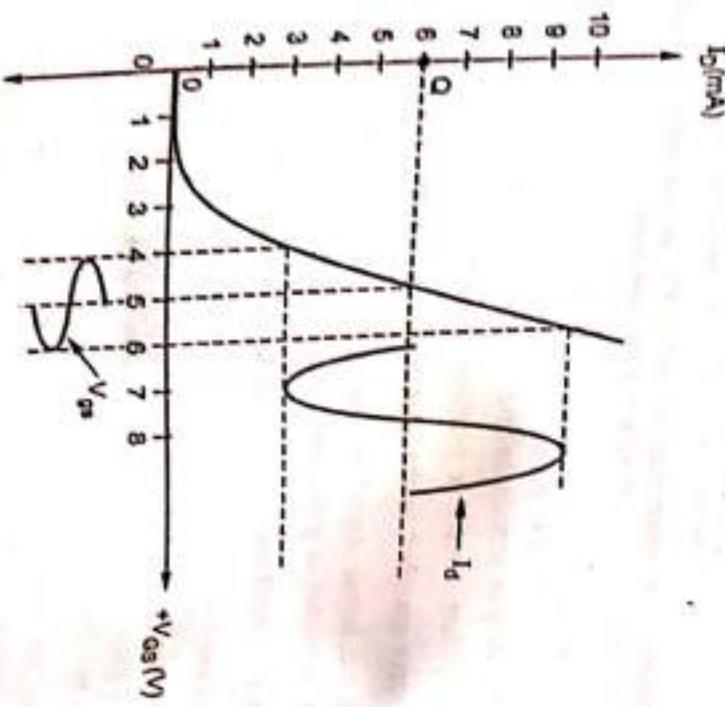
- As a result of above action, a small change in gate voltage produces a large change in drain current. This fact makes MOSFET capable of raising the strength of a weak signal and hence act as an amplifier.

- The slope of transfer characteristics is represented by transconductance,  $g_m$ . It is defined as

$$g_m = \frac{\Delta I_D}{\Delta V_{GS} \text{ } |V_{DS} \text{ constant}|}$$



(a) CS MOSFET amplifier



(b) Transfer characteristics

### Q.35 State the applications of MOSFET.

Ans. :

1. E-MOSFET is used as a switch. As a switch, they are used in digital circuits. They are also used in chopping circuits.
2. Used to fabricate digital gates from NMOS, PMOS and CMOS families.
3. Since they require less space used in LSI and VLSI circuits.
4. Used in regulated DC power supplies.
5. Used in high current switching applications.
6. Used as an inverter.
7. Used as an active load (in integrator circuits).
8. It can be used as a high frequency amplifier.
9. It can be used as a resistor.

- The voltage gain of the CS amplifier is given by,  
Voltage gain,  $A_V = -g_m R'_L$  where  $R'_L = R_D | R_L = -g_m (R_D | R_C)$
- The negative sign indicates the output voltage is 180° out of phase with the input signal voltage.

### 2.10 Applications of MOSFET

## 2.11 Comparison Between BJT and MOSFET

**Q.36 Give the comparison between BJT and MOSFET.**

IITG [SPRU : Dec.-16, Marks 6]

Ans. :

Sr. No.	Parameter	BJT	MOSFET
1.	Control element	Current controlled device. Input current $I_B$ controls output current $I_C$	Voltage controlled device. Input voltage $V_{GS}$ controls drain current $I_D$
2.	Device type	Current flows due to both, majority and minority carriers and hence bipolar device.	Current flows only due to majority carriers and hence unipolar device.
3.	Types	n-p-n and p-n-p	n-channel and p-channel.
4.	Symbols		
5.	Configurations	CE, CB, CC	CS, CG, CD
6.	Input resistance	Less compare to MOSFET.	Very high compare to BJT.

7.	Size	Bigger than MOSFET.	Smaller in construction than BJT, thus making them useful in integrated circuits (IC).
8.	Sensitivity	Higher sensitivity to changes in the applied signals.	Less sensitivity to changes in the applied voltage.
9.	Thermal stability	Less	More
10.	Thermal runaway	Exists in BJT, because of cumulative effect of increase in $I_C$ with temperature, resulting in increase in temperature in the device.	Does not exist in MOSFET, because drain resistance $r_d$ increases with temperature, which reduces $I_D$ , reducing the $I_D$ and hence the temperature of the device.
11.	Relation between input and output	Linear	Non-linear
12.	Ratio of output to input	$\frac{\Delta I_C}{\Delta I_B} = \beta$	$\frac{\Delta I_D}{\Delta V_{GS}} = g_m$
13.	Thermal noise	More in BJT as more charge carriers cross junctions.	Much lower in MOSFET as very few charge carriers cross the junction.
14.	Gain bandwidth product	High	Low

**PART C****Operational Amplifier (Op-amp)****2.12 : Introduction****Q.37 What is operational amplifier ?**

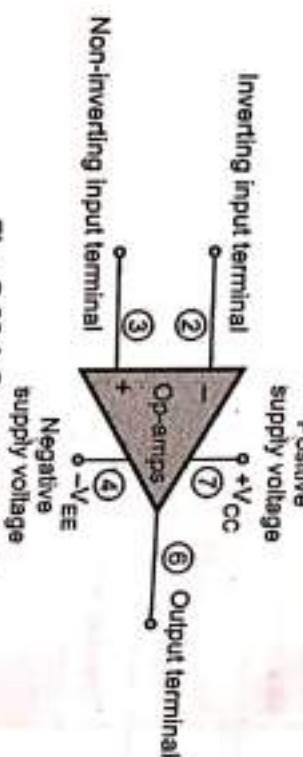
ESE [SPU : Dec.-12, Marks 2]

Ans. : • The operational amplifier, most commonly referred as 'op-amp' was introduced in 1940s.

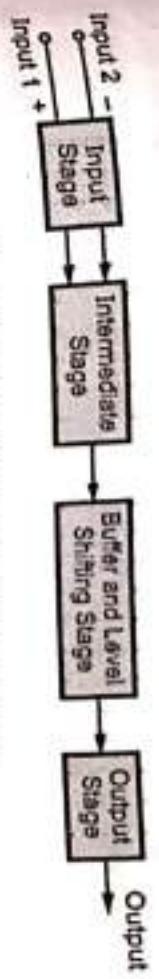
- In earlier days it was used to perform various mathematical operations such as addition, subtraction, multiplication etc. in the analog computers hence it is called operational amplifier.
- Now a days it is available in IC form which is used to build variety of electronic circuits.

**2.13 : Op-amp Symbol and Terminals****Q.38 With the op-amp symbol explain the importance of inverting and noninverting terminals.**

Ans. : • The Fig. Q.38.1 shows the symbol of op-amp.

**Fig. Q.38.1 Op-amp symbol**

- When input is applied to inverting terminal, op-amp produces the output which is inverted with respect to input i.e. having  $180^\circ$  phase difference in between input and output.
- When input is applied to noninverting terminal, op-amp produces the output which is in phase with the input i.e. having  $0^\circ$  phase difference in between input and output.

**Fig. Q.39.1 Block diagram of an op-amp****1. Input Stage**

- The input stage requires high input impedance to avoid loading on the sources. It requires two input terminals. It also requires low output impedance.
- All such requirements are achieved by using the dual input, balanced output differential amplifier as the input stage.

- The function of a differential amplifier is to amplify the difference between the two input signals. This stage provides most of the voltage gain of the amplifier.

**2. Intermediate Stage**

- The output of the input stage drives the next stage which is an intermediate stage.

- This is another differential amplifier with dual input, unbalanced i.e. single ended output.
- The overall gain requirement of the op-amp is very high. The input stage alone cannot provide such a high gain.
- The main function of the intermediate stage is to provide an additional voltage gain required with the help of the chain of cascaded amplifiers called multistage amplifiers.

**Q.39 Draw the internal block schematic of op-amp and mention the role of each stage.**

ESE [SPU : May-08,11,12, Dec-10,11,12, Marks 6]

Ans. : • Commercial integrated circuit op-amps usually consists of four cascaded blocks.

- The block diagram of IC op-amp is shown in the Fig. Q.39.1.
- The block diagram of IC op-amp is shown in the Fig. Q.39.1.

**3. Level Shifting Stage**

- All the stages are directly coupled to each other. The coupling capacitors are not used to cascade the stages. Hence the d.c. quiescent voltage level of previous stage gets applied as the input to the next stage. Hence stage by stage d.c. level increases well above ground potential.

- Such a high d.c. voltage level may drive the transistors into saturation. This further may cause distortion in the output due to clipping. This may limit the maximum a.c. output voltage swing without any distortion.

- Hence before the output stage, it is necessary to bring such a high d.c. voltage level to zero volts with respect to ground.

- The level shifter stage brings the d.c. level down to ground potential, when no signal is applied at the input terminals. Then the signal is given to the last stage which is the output stage.

**4. Output Stage**

- The basic requirements of an output stage are low output impedance, large a.c. output voltage swing and high current sourcing and sinking capability.
- The push-pull complementary amplifier meets all these requirements and hence used as an output stage. This stage increases the output voltage swing and keeps the voltage swing symmetrical with respect to ground.
- The stage raises the current supplying capability of the op-amp.

**Important Points to Remember**

- The supply voltages of the op-amp are  $+V_{CC}$  and  $-V_{EE}$ . These supply voltage levels decide the maximum output voltage levels of the op-amp.
- Practically the op-amp output saturates at the voltages slightly less than the supply voltages  $+V_{CC}$  and  $-V_{EE}$ .

- Practically maximum output voltage swing of the op-amp is 0.9 times the supply voltages.

- The output of an op-amp saturates if tries to increase more than its supply voltages.

**2.15 : Ideal Op-amp Characteristics**

**Q40** Explain all the characteristics of op-amp. State their values for an ideal op-amp.  
[5PU : Dec-05, M.A., May-07, Marks 6]

**OR** Explain the following Ideal characteristics of op-amp :

- BW
  - Slew rate
  - Band width.
- [5PU : Dec-07, Marks 6]

**OR** Define : i) BW ii) PSRR iii) CMRR for an op-amp.  
[5PU : May-15, Marks 6]

**OR Define :** i) Input bias current ii) Input offset current  
iii) Input offset voltage iv) Output offset voltage for an op-amp.  
State their ideal values.

**Ans. :** The various characteristics of op-amp and their values for an ideal op-amp are,

- Open loop voltage gain : The gain of the op-amp in open loop condition is called its open loop gain denoted as A<sub>OL</sub>.

- It is infinite for an ideal op-amp.

- Input impedance : The equivalent resistance measured at either of the two terminals with the other terminal grounded is input impedance. It is denoted as R<sub>in</sub>.

- It is infinite for an ideal op-amp. Hence input current of an ideal op-amp is zero.

- Output impedance : The equivalent resistance measured between the output terminal of the op-amp and the ground. It is denoted as R<sub>o</sub>.

- It is zero for an ideal op-amp.

- Input offset voltage : When both the input terminals are grounded there exists a small voltage at the output though it should be ideally zero.

- To make this output voltage zero, a small voltage is required to be applied to one of the input terminals. This d.c. voltage, which makes the output voltage zero, when the other terminal is grounded is called **input offset voltage** denoted as  $V_{ios}$ .
- It is zero for an ideal op-amp.
- Input bias current :** For ideal op-amp, no current flows into the input terminals.
- Practically small currents flow into the two input terminals of an op-amp. These are denoted as  $I_{b1}$  and  $I_{b2}$ .
- The input bias current is the average value of the magnitudes of the two input currents  $I_{b1}$  and  $I_{b2}$  of an op-amp. It is denoted as  $I_b$ .

Input bias current,

$$I_b = \frac{|I_{b1}| + |I_{b2}|}{2}$$

- It is zero for an ideal op-amp.

- f) **Input offset voltage :** The difference in magnitudes of  $I_{b1}$  and  $I_{b2}$  is called as input offset current and is denoted as  $I_{ios}$ .

Input offset current,

$$I_{ios} = |I_{b1} - I_{b2}|$$

- It is zero for an ideal op-amp.
- Output offset voltage :** The voltage existing at the output when inputs are zero due to the input offset voltage and bias currents is called **output offset voltage** and denoted as  $V_{oos}$ .
  - It is zero for an ideal op-amp.
- Slew rate :** The slew rate is defined as the maximum rate of change of output voltage with time. It is denoted as  $S$  and expressed in  $\text{V}/\mu\text{s}$ .
- This ensures that the changes in the output voltage occur simultaneously with the changes in the input voltage.

$$\boxed{\text{Slew rate} = S = \left. \frac{dV_o}{dt} \right|_{\text{maximum}}}$$

- Its ideal value is infinite for the op-amp.
- i) **Power supply rejection ratio :** The power supply rejection ratio is defined as the ratio of the change in input off set voltage due to the change in supply voltage producing it, keeping other power supply voltage constant.
- It is denoted as PSRR and measured in  $\text{mV/V}$  or  $\mu\text{V/V}$ .
- It is also called **power supply sensitivity** or **supply voltage rejection ratio (SVRR)**.

$$\boxed{\text{PSRR} = \left. \frac{\Delta V_{ios}}{\Delta V_{CC}} \right|_{\text{constant } V_{EE}}} = \left. \frac{\Delta V_{ios}}{\Delta V_{EE}} \right|_{\text{constant } V_{CC}}$$

- It is zero for an ideal op-amp.

- j) **CMRR :** The ratio of differential gain and common mode gain is defined as CMRR.

- It is infinite for an ideal op-amp.

- k) **Bandwidth :** The range of frequency over which the amplifier performance is satisfactory is called its **bandwidth**.

- It is denoted as BW measured in Hz.

- It is infinite for an ideal op-amp.

### Summary of Ideal Op-amp Characteristics

Characteristics	Symbol	Values
Open loop voltage gain	$A_{OL}$	$\infty$
Input impedance	$R_{in}$	$\infty$
Output impedance	$R_o$	0
Offset voltage	$V_{oos}$	0
Bandwidth	B.W.	$\infty$

C.M.R.R	$\rho$	$\infty$
Slew rate	S	$\infty$
Power supply rejection ratio	PSRR	0

### 2.16 : IC 741 Op-amp

**Q41** Draw the pin diagram of IC 741 op-amp and state its features.

**Ans. :** • The IC 741 is 8 pin IC available in dual in line package (DIP).

• The pin diagram of IC 741 op-amp is shown in the Fig. Q41.1.

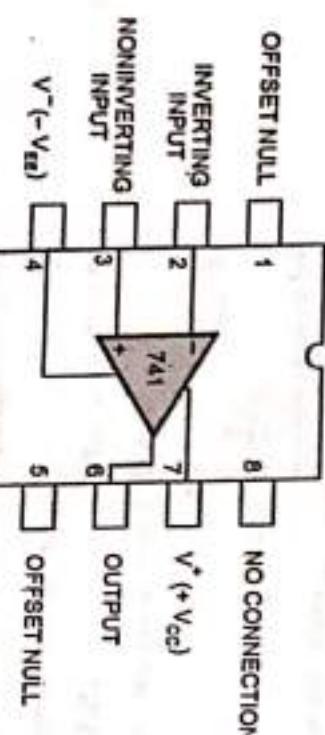


Fig. Q41.1 Pin diagram of IC 741 op-amp

- The pins 1 and 5 are offset null pins. These are used to nullify offset voltages and provide offset voltage compensation.
- The pin 2 is inverting input while pin 3 is noninverting input terminal.
- The output is to be taken from pin 6.
- The pin 4 is for  $-V_{EE}$  supply while pin 7 is for  $+V_{CC}$  supply.
- The pin 8 is the dummy pin and no connection are to be made to this pin externally.

#### Features of IC 741 :

- No frequency compensation required.
- Short circuit protection provided.

- Offset voltage null capability.
  - Large common mode and differential voltage range.
  - No latch up.
  - Compare ideal and practical characteristics of IC 741 op-amp.
- ESE [PPU : May-04, Dec.-08, Marks 6]

**Ans. :** • The Table Q42.1 lists the ideal op-amp characteristics and the typical values of these characteristics for 741 IC.

Sr. No.	Parameter	Symbol	Ideal	Typical for 741 IC
1.	Open loop voltage gain	$A_{OL}$	$\infty$	$2 \times 10^5$
2.	Output Impedance	$Z_{out}$	0	$75 \Omega$
3.	Input Impedance	$Z_{in}$	$\infty$	$2 M\Omega$
4.	Input offset current	$I_{ios}$	0	$2 \text{ mA}$
5.	Input offset voltage	$V_{ios}$	0	$2 \text{ mV}$
6.	Bandwidth	B.W	$\infty$	$1 \text{ MHz}$
7.	CMRR	$\rho$	$\infty$	$90 \text{ dB}$
8.	Slew rate	S	$\infty$	$0.5 \text{ V}/\mu\text{sec}$
9.	Input bias current	$I_b$	0	$80 \text{ nA}$
10.	Power supply rejection ratio	PSRR	0	$30 \text{ \mu V/V}$

Table Q42.1

### 2.17 : Realistic Simplifying Assumptions

**Q43** State the realistic simplifying assumptions related to op-amp.

- The current drawn by either of the input terminals (inverting and noninverting) is zero.

**Ans. :** Realistic simplifying assumptions :

ESE [Marks 3]

## 2. Virtual Ground :

- This means the differential input voltage  $V_d$  between the noninverting and inverting input terminals is essentially zero i.e.  $V_d = (V_1 - V_2) = 0$  i.e.  $V_1 = V_2$ .
- Thus we can say that under linear range of operation there is virtually short circuit between the two input terminals, in the sense that their voltages are same.
- If the non-inverting terminal is grounded, by the concept of virtual short, the inverting terminal is also at ground potential, though there is no physical connection between the inverting terminal and the ground. This is the principle of virtual ground.

### Steps to Analyse Op-amp Circuits

**Step 1 :** Input current of the ideal op-amp is always zero. Using this, the current distribution in the circuit is to be obtained.

**Step 2 :** The input terminals of the op-amp are always at the same potential. Thus if one is grounded, the other can be treated to be virtually grounded. From this, the expressions for various branch currents can be obtained.

**Step 3 :** Analyzing the various expressions obtained, eliminating unwanted variables, the output expression in terms of input and circuit parameters can be obtained.

### 2.18 : Inverting Amplifier Using Op-amp

**Q.44 Prove that for an inverting amplifier,  $A_V = -\frac{R_f}{R_i}$ .**

$$\text{ESE [SPRU : May-04, 07, Marks 6]}$$

**Ans. :** • The basic circuit diagram of an inverting amplifier using op-amp is shown in the Fig. Q.44.1.

- By the concept of virtual ground the two input terminals are always at the same potential.

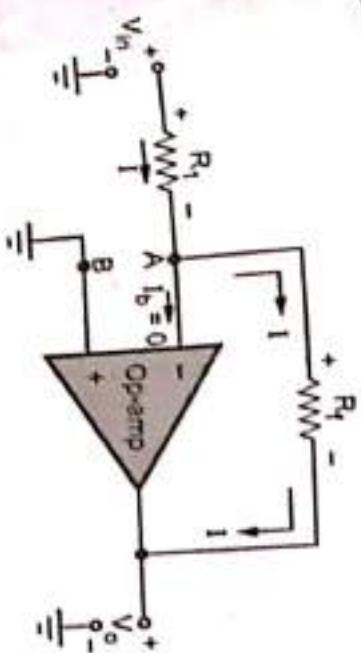


Fig. Q.44.1 Inverting amplifier

• As node B is grounded, node A is also at ground potential, from the concept of virtual ground, so  $V_A = 0$

$$I = \frac{V_{in} - V_A}{R_i} = \frac{V_{in}}{R_i} \quad (\text{as } V_A = 0) \quad \dots (1)$$

• The op-amp input current is always zero hence entire current I passes through the resistance  $R_f$ .

• From the output side, considering the direction of current I we can write,

$$I = \frac{V_A - V_o}{R_f} = \frac{-V_o}{R_f} \quad (\text{as } V_A = 0) \quad \dots (2)$$

• Equating (1) and (2) we get,  $\frac{V_{in}}{R_i} = -\frac{V_o}{R_f}$

$$A_V = \frac{V_o}{V_{in}} = -\frac{R_f}{R_i} \quad (\text{Gain with feedback}) \quad \dots (3)$$

• The  $\frac{R_f}{R_i}$  is the gain of the amplifier while negative sign indicates that the polarity of output is opposite to that of input. Hence it is called inverting amplifier.

- The waveforms of inverting amplifier are shown in the Fig. Q.44.2.

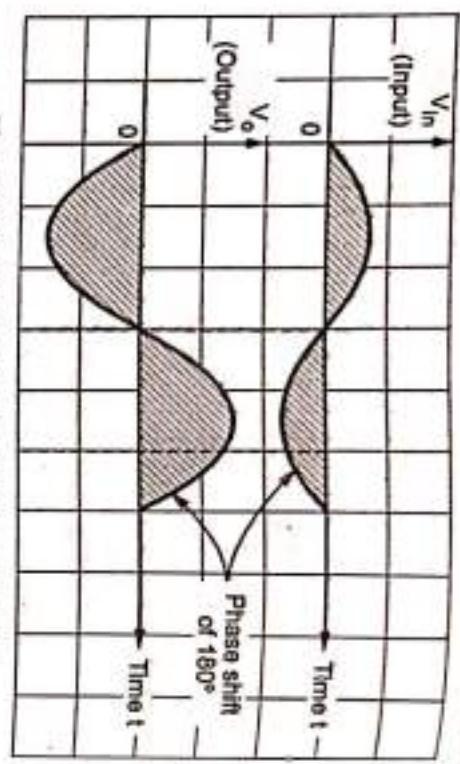


Fig. Q.44.2 Waveforms of Inverting amplifier

**Important Points to Remember**

- The voltage gain of an inverting amplifier depends on the ratio of the two resistances. Hence selecting  $R_f$  and  $R_1$ , the required value of gain can be easily obtained.

- If the ratio of  $R_f$  and  $R_1$  is  $K$  which is other than one, the circuit is called scale changer while for  $R_f/R_1 = 1$  it is called phase inverter.

- Depending upon the ratio  $R_f/R_1$ , the output voltage can be greater than, less than or equal to the input voltage, in magnitude.

**Q.45** For the inverting amplifier using op-amp if  $R_f = 100 \text{ k}\Omega$ ;  $R_1 = 10 \text{ }\Omega$ ,  $V_{CC} = \pm 10 \text{ V}$ ,  $V_i = 2 \text{ V}$  d.c. Calculate : 1) Output voltage 2) Is the result in part (1) Is practically possible ? Justify. [ISPU : May-05, 09, Marks 6]

Ans. : 1) For an inverting amplifier,

$$\frac{V_o}{V_i} = -\frac{R_f}{R_1} \quad \text{i.e.} \quad V_o = -\frac{100}{10} \times (2)$$

∴  $V_o = -20 \text{ V}$  ... Output voltage

- 2) As  $V_{CC} = \pm 10 \text{ V}$ , due to the saturating property of op-amp, the output saturates at  $\pm 10 \text{ V}$ . Hence the output voltage of  $-20 \text{ V}$  is practically impossible.

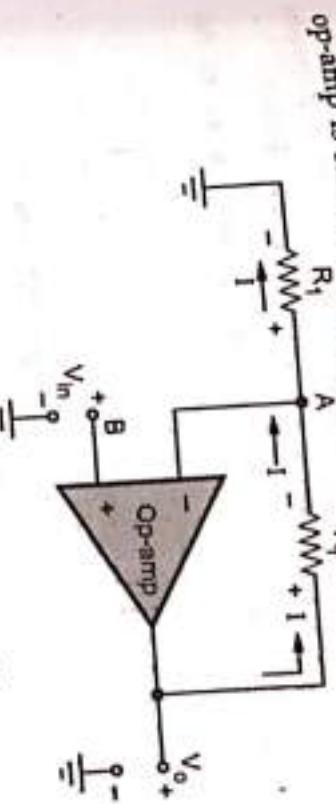


Fig. Q.46.1 Non-Inverting amplifier

- The input is applied to the noninverting input terminal of the op-amp.
- The node B is at potential  $V_{in}$ , hence the potential of point A is same as B which is  $V_{in}$ , from the concept of virtual ground.

$$V_A = V_B = V_{in}$$

- From the output side we can write,

$$I = \frac{V_o - V_A}{R_f} = \frac{V_o - V_{in}}{R_f} \quad (\text{As } V_A = V_{in}) \quad \dots (1)$$

- At the inverting terminal,  $I = \frac{V_A - 0}{R_1} = \frac{V_{in}}{R_1}$  (As  $V_A = V_{in}$ ) ... (2)

- Entire current passes through  $R_1$  as input current of op-amp is zero.

$$\frac{V_o - V_{in}}{R_f} = \frac{V_{in}}{R_1}$$

$$\frac{V_o}{R_f} = \frac{V_{in}}{R_1} + \frac{V_{in}}{R_f} = V_{in} \left[ \frac{(R_1 + R_f)}{R_1 R_f} \right]$$

$$A_V = \frac{V_o}{V_{in}} = \frac{(R_1 + R_f) R_f}{R_1 R_f} = \frac{R_1 + R_f}{R_1}$$

$$A_V = \frac{V_o}{V_{in}} = 1 + \frac{R_f}{R_1}$$

∴ (3)

- The positive sign indicates that there is no phase shift between input and output. Hence it is called noninverting amplifier.

- The waveforms of the non-inverting amplifier are shown in the Fig. Q.46.2.

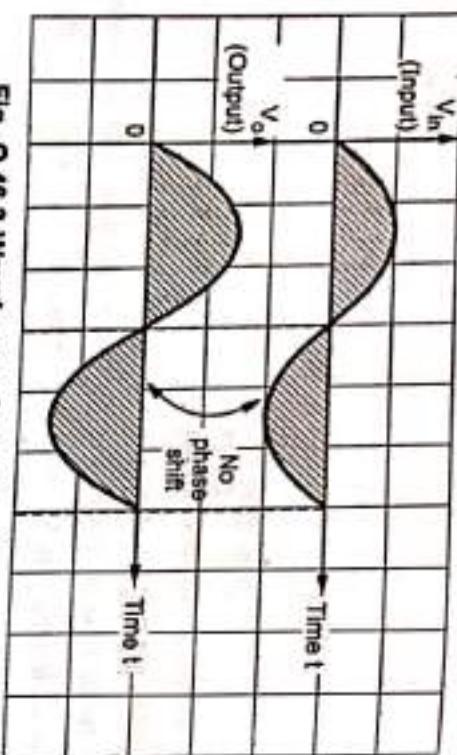


Fig. Q.46.2 Waveforms of non-inverting amplifier

#### Important Points Regarding Non-Inverting Amplifier

- In non-inverting amplifier the input may not be applied directly to the non-inverting terminal as considered while deriving the output expression but it may be applied through some circuit.
- Let  $V_{in}$  is the input voltage applied to the non-inverting amplifier through some resistive network such that the voltage available at the non-inverting input terminal is  $V_B$  which is different than  $V_{in}$ . Then the non-inverting amplifier always amplifies voltage available to its non-inverting terminal by the factor  $(1 + \frac{R_f}{R_1})$ . Hence  $V_o = \left(1 + \frac{R_f}{R_1}\right) V_B$ .

Q.47 An op-amp is used in noninverting mode with  $R_1 = 1 \text{ k}\Omega$ ,  $V_{CC} = \pm 15 \text{ V}$ . Calculate output voltage for

$$\begin{aligned} R_f &= 12 \text{ k}\Omega, V_{CC} = \pm 15 \text{ V} \\ V_{in} &= 250 \text{ mV} \end{aligned}$$

[SPPU : Dec.-05, Marks 6; May-12, Marks 4]

Ans. :  $R_1 = 1 \text{ k}\Omega, R_f = 12 \text{ k}\Omega, V_{CC} = \pm 15 \text{ V}$

For noninverting mode,

$$A = \left(1 + \frac{R_f}{R_1}\right) = \left(1 + \frac{12}{1}\right) = 13 = \frac{V_o}{V_{in}}$$

$$V_{in} = 250 \text{ mV}$$

$$V_o = A V_{in} = 13 \times 250 \times 10^{-3} = 3.25 \text{ V}$$

$$V_{in} = 3 \text{ V}$$

$$V_o = A V_{in} = 13 \times 3 = 39 \text{ V}$$

But op-amp output saturates at  $\pm V_{CC}$  i.e.  $\pm 15 \text{ V}$ . Thus practically output saturates at  $+ 15 \text{ V}$  and  $39 \text{ V}$  output is not practically possible.

Q.48 Calculate output voltage ' $V_o$ ' of Op - Amp circuit shown in Fig.Q.48.1. Draw I/P and O/P waveforms. [SPPU : May-17, Marks 6]

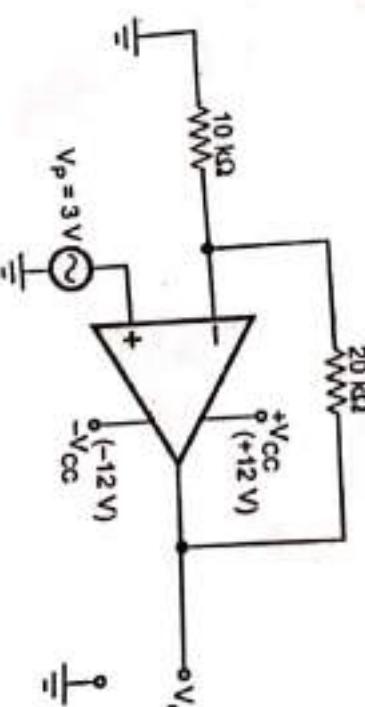


Fig. Q.48.1

Ans. : It is noninverting amplifier.

$$R_f = 20 \text{ k}\Omega, R_1 = 10 \text{ k}\Omega$$

$$V_o = \left(1 + \frac{R_f}{R_1}\right) V_p = \left(1 + \frac{20}{10}\right) \times 3 \sin \omega t = 9 \sin \omega t \text{ V.}$$

- The peak value of output is 9 V. Note that input is sinusoidal with a peak value  $V_p = 3$  V. The input and output waveforms are shown in Fig. Q.48.2.

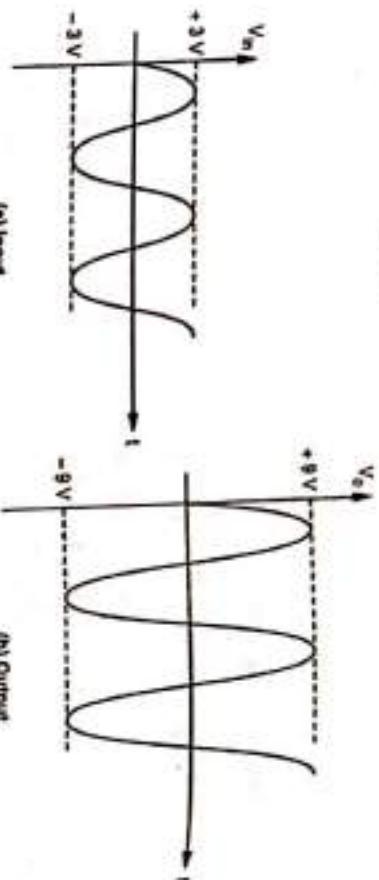


FIG. Q.48.2

## QUESTION BANK FOR IN SEM EXAM

### Unit - I

**Q.1** Differentiate between active and passive components. Give examples of each. (Refer Q.2 of Chapter 1)

**Q.2** Explain the three types of fixed resistors with neat diagrams. (Refer Q.3 of Chapter 1)

**Q.3** Explain any three types of variable resistors(potentiometers) with neat diagrams. (Refer Q.4 of Chapter 1)

**Q.4** Explain the three types of fixed capacitors with neat diagrams. (Refer Q.5 of Chapter 1)

**Q.5** Write a note on variable capacitors. (Refer Q.6 of Chapter 1)

**Q.6** Explain the various types of inductors. State its applications. (Refer Q.7 of Chapter 1)

**Q.7** Define switch and explain various types of switches. (Refer Q.8 of Chapter 1)

**Q.8** Define relay and explain the working principle of a relay circuit. (Refer Q.9 of Chapter 1)

**Q.9** What is extrinsic semiconductor ? What is doping and dopants ? Which are the two types of extrinsic semiconductors ? (Refer Q.11 of Chapter 1)

**Q.10** Explain the formation of n-type semiconductor.  
**(Refer Q.12 of Chapter 1)**

**Q.11** Explain the formation of p-type semiconductor.  
**(Refer Q.13 of Chapter 1)**

**Q.12** What is drift current ? State its expression.  
**(Refer Q.15 of Chapter 1)**

**Q.13** What is diffusion current ? State its equation.  
**(Refer Q.16 of Chapter 1)**

**Q.14** Explain the formation of depletion region in unbiased p-n junction diode. **(Refer Q.19 of Chapter 1)**

**Q.15** Explain the forward biasing of a diode.  
**(Refer Q.20 of Chapter 1)**

**Q.16** Explain the reverse biasing of a diode.  
**(Refer Q.21 of Chapter 1)**

**Q.17** Explain V-I characteristics of p-n junction diode.  
**(Refer Q.22 of Chapter 1)**

**Q.18** Explain how diode can be used as a switch.  
**(Refer Q.23 of Chapter 1)**

**Q.19** Draw the circuit and explain the operation of a half wave rectifier alongwith the waveforms.  
**(Refer Q.25 of Chapter 1)**

**Q.20** Draw the full wave rectifier circuit and explain its operation along with the waveforms. **(Refer Q.27 of Chapter 1)**

**Q.21** Derive the expressions for the average d.c. current, d.c. load voltage and RMS value of the load current for the full wave rectifier circuit with two diodes. **(Refer Q.28 of Chapter 1)**

**Q.22** Draw the circuit of bridge rectifier and explain its operation. Give the input and output waveforms.  
**(Refer Q.32 of Chapter 1)**

**Q.23** Draw and explain the V-I characteristics of a zener diode. What are the two breakdown mechanisms in a zener diode ?  
**(Refer Q.37 of Chapter 1)**

**Q.24** Describe with the help of neat circuit diagram the operation of zener voltage regulator under varying load and varying input conditions. **(Refer Q.38 of Chapter 1)**

**Q.25** Explain the working principle of LED.  
**(Refer Q.42 of Chapter 1)**

**Q.26** State the advantages, disadvantages and applications of LED.  
**(Refer Q.43 of Chapter 1)**

**Q.27** Explain the working of photodiode along with its characteristics. Why photodiode is operated in reverse biased condition when operated as a optical detector ? **(Refer Q.44 of Chapter 1)**

## Unit - II

**Q.1** State the biasing conditions required for the three regions of operation of a BJT. **(Refer Q.1 of Chapter 2)**

**Q.2** Explain the working principle of npn transistor.  
**(Refer Q.2 of Chapter 2)**

- Q.3** Explain the working principle of pnp transistor with the help of constructional diagram. (Refer Q.3 of Chapter 2)
- Q.4** Give comparison between pnp and npn transistors. (Refer Q.4 of Chapter 2)
- Q.5** State the three transistor configurations. (Refer Q.5 of Chapter 2)
- Q.6** Draw the neat circuit configuration of CB. (Refer Q.6 of Chapter 2)
- Q.7** Sketch and explain the input characteristics of transistor in CB configuration. (Refer Q.7 of Chapter 2)
- Q.8** What is early effect? How can it account for the CB input characteristics? (Refer Q.8 of Chapter 2)
- Q.9** With a neat diagram explain the output characteristics of transistor in CB configuration. (Refer Q.9 of Chapter 2)
- Q.10** Draw the neat circuit configuration of CE. (Refer Q.10 of Chapter 2)
- Q.11** Sketch and explain the input characteristics of transistor in CE configuration. (Refer Q.11 of Chapter 2)
- Q.12** With a neat diagram explain output characteristics of npn transistor in CE-configuration. Indicate and explain three regions of operation. (Refer Q.12 of Chapter 2)
- Q.13** Define  $I_{C(IV)}$  and  $I_{CBO}$ . (Refer Q.13 of Chapter 2)
- Q.14** Define  $\alpha$ . (Refer Q.14 of Chapter 2)
- Q.15** Define  $\beta$ . (Refer Q.15 of Chapter 2)

- Q.16** Define  $\gamma$ . (Refer Q.16 of Chapter 2)
- Q.17** Derive the relationship between  $\alpha_{dc}$  and  $\beta_{dc}$ . (Refer Q.17 of Chapter 2)
- Q.18** Compare CB, CE and CC transistor configurations. (Refer Q.23 of Chapter 2)
- Q.19** Explain the working of a transistor as a switch. (Refer Q.24 of Chapter 2)
- Q.20** Explain the working of BJT as a CE amplifier. (Refer Q.25 of Chapter 2)
- Q.21** Explain with a circuit diagram a single stage common emitter amplifier. State the function of each component in the circuit. (Refer Q.26 of Chapter 2)
- Q.22** Explain the construction of n-channel enhancement type MOSFET. (Refer Q.27 of Chapter 2)
- Q.23** Explain the working of n-channel enhancement MOSFET. (Refer Q.28 of Chapter 2)
- Q.24** Draw and explain drain characteristics of an n-channel enhancement type MOSFET. (Refer Q.29 of Chapter 2)
- Q.25** Draw and explain transfer characteristics of an n-channel enhancement type MOSFET. (Refer Q.30 of Chapter 2)
- Q.26** Draw and explain the drain and transfer characteristics of p-channel MOSFET. (Refer Q.31 of Chapter 2)
- Q.27** Explain the operating regions of E-MOSFET. (Refer Q.32 of Chapter 2)

**Q.28** Explain the working of E-MOSFET as a switch.  
 (Refer Q.33 of Chapter 2)

**Q.29** Explain the operation of MOSFET as an amplifier with the help of suitable circuit diagram and waveform.  
 (Refer Q.33 of Chapter 2)

**Q.30** State the applications of MOSFET.  
 (Refer Q.35 of Chapter 2)

**Q.31** Give the comparison between BJT and MOSFET.  
 (Refer Q.36 of Chapter 2)

**Q.32** Draw the internal block schematic of op-amp and mention the role of each stage. (Refer Q.39 of Chapter 2)

**Q.33** Explain all the characteristics of op-amp. State their values for an ideal op-amp. (Refer Q.40 of Chapter 2)

**Q.34** State the realistic simplifying assumptions related to op-amp.  
 (Refer Q.43 of Chapter 2)

**Q.35** Prove that for an inverting amplifier,  $A_v = -\frac{R_f}{R_1}$ .

(Refer Q.44 of Chapter 2)

**Q.36** Draw non-inverting amplifier using op-amp and derive expression for its output voltage.  
 (Refer Q.46 of Chapter 2)

## SOLVED SAMPLE QUESTION PAPER - 1 [IN SEM] [AS PER 2019 PATTERN]

Time : 1 Hour]

Instructions to the candidates :

- 1) Answer Q.1 or Q.2, Q.3 or Q.4.
- 2) Neat diagrams must be drawn wherever necessary.
- 3) Figures to the right indicate full marks.

- 4) Make suitable assumptions if necessary.
- Q.1 a) Explain the various types of fixed resistors.  
 (Refer Q.3 of Chapter 1) [4]

- b) Draw the circuit of half wave rectifier and explain its operation. (Refer Q.24 of Chapter 1) [5]

- c) Draw the symbol of LED and explain its working principle.  
 (Refer Q.40 and Q.41 of Chapter 1) [6]

**OR**

- Q.2 a) Explain any four types of switches.  
 (Refer Q.8 of Chapter 1) [4]

- b) Derive the expressions for average d.c. output voltage, average d.c. output current, and rms current for center-tap full wave bridge rectifier. (Refer Q.28 of Chapter 1) [5]

- c) For the given circuit (Fig. 1) if,  $V_Z = 12 V$ ,  $I_{Z\min} = 1 \text{ mA}$  and  $I_{Z\max} = 50 \text{ mA}$ . Calculate Min. and Max.  $I_L$  and  $R_L$  for which zener diode maintain its regulation.  
 (Refer Q.39 of Chapter 1) [6]

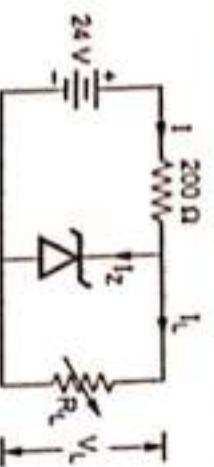


Fig. 1

- Q.3** a) Sketch and explain the input characteristics of transistor in CE configuration. (Refer Q.2 of Chapter 2) [6]

- b) Explain the working of MOSFET as an amplifier. (Refer Q.27 of Chapter 2)

[5]

- c) Draw the circuit of op-amp inverting amplifier and derive expression for its gain. (Refer Q.44 of Chapter 2) [4]

OR

- Q.4** a) Explain the construction and working of n-channel enhancement MOSFET. (Refer Q.29 of Chapter 2) [6]

- b) Define  $\beta$  and derive the relationship between  $\alpha_{dc}$  and  $\beta_{dc}$ . (Refer Q.7 of Chapter 2)

[4]

- c) State and explain various characteristics of an ideal op-amp. (Refer Q.40 of Chapter 2) [5]

### SOLVED SAMPLE QUESTION PAPER - 2 [IN SEM] [AS PER 2019 PATTERN]

Time : 1 Hour

[Maximum Marks : 30]

- Q.1** a) Differentiate between active and passive components. Give examples of each. (Refer Q.2 of Chapter 1) [4]

- b) Explain the formation of p-type semiconductor. (Refer Q.13 of Chapter 1)

[5]

- Q.2** a) Explain the basic principle of zener diode. Draw its symbol. (Refer Q.36 of Chapter 1) [3]
- b) Draw the full wave rectifier circuit and explain its operation along with the waveforms. (Refer Q.27 of Chapter 1) [6]
- c) Explain the working of photodiode along with its characteristics. Why photodiode is operated in reverse biased condition when operated as a optical detector ? (Refer Q.44 of Chapter 1) [6]

OR

- Q.3** a) Define  $\alpha$ ,  $\beta$  and derive relation between them. (Refer Q.14, Q.15 and Q.17 of Chapter 2) [6]

- b) Explain the working of n-channel enhancement MOSFET. (Refer Q.28 of Chapter 2) [5]

c) Define :

- i) Input bias current ii) Input offset current  
iii) Input offset voltage  
iv) Slew rate (Refer Q.40 of Chapter 2) [4]

OR

- Q.4** a) Explain with a circuit diagram a single stage common emitter amplifier. State the function of each component in the circuit. (Refer Q.26 of Chapter 2) [6]

- b) What is early effect ? How can it account for the CB input characteristics ? (Refer Q.8 of Chapter 2) [4]

- c) Draw the internal block schematic of op-amp and mention the role of each stage. (Refer Q.39 of Chapter 2) [5]

### SOLVED SAMPLE QUESTION PAPER - 3 [IN SEM] [AS PER 2019 PATTERN]

Time : 1 Hour

- Q.1 a)** Write a note on variable capacitors. [Maximum Marks : 30]

(Refer Q.6 of Chapter 1)

- b) Explain the formation of n-type semiconductor. [6]

(Refer Q.12 of Chapter 1)

- c) Draw the circuit and explain the operation of a half wave rectifier alongwith the waveforms. [5]

(Refer Q.25 of Chapter 1)

OR

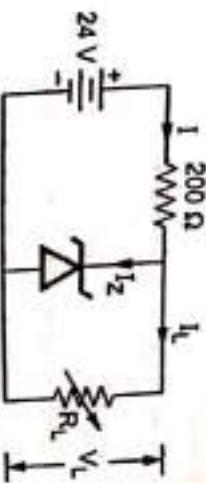
- Q.2 a)** State the advantages, disadvantages and applications of LED. [4]

(Refer Q.43 of Chapter 1)

- b) What is diffusion current ? State its equation. [4]

(Refer Q.16 of Chapter 1)

- c) For the given circuit (Fig. Q.40.1) if  $V_Z = 12$  V,  $I_{Z\min} = 1$  mA and  $I_{Z\max} = 50$  mA. Calculate Min. and Max.  $I_L$  and  $R_L$  for which zener diode maintain its regulation. (Refer Q.40 of Chapter 1) [6]



- Q.3 a)** With a neat diagram explain the output characteristics of transistor in CB configuration. (Refer Q.9 of Chapter 2) [6]

- b) Draw and explain transfer characteristics of an n-channel enhancement type MOSFET (Refer Q.30 of Chapter 2) [5]

- c) With the op-amp symbol explain the importance of inverting and noninverting terminals. (Refer Q.38 of Chapter 2) [4]

OR

- Q.4 a)** Give the comparison between BJT and MOSFET. [6]

(Refer Q.36 of Chapter 2)

- b) Calculate the values of  $I_C$  and  $I_E$  for a BJT with  $\alpha_{ac} = 0.97$  and  $I_S = 50 \mu A$ . Determine  $\beta_{ac}$  for the device. [5]

(Refer Q.18 of Chapter 2)

- c) Draw non-inverting amplifier using op-amp and derive expression for its output voltage. [5]

(Refer Q.46 of Chapter 2)

### SOLVED SAMPLE QUESTION PAPER - 4 [IN SEM] [AS PER 2019 PATTERN]

Time : 1 Hour

[Maximum Marks : 30]

- Q.1 a)** Explain the three types of fixed capacitors with neat diagrams. (Refer Q.5 of Chapter 1) [6]

- b) What is drift current ? State its expression. (Refer Q.15 of Chapter 1) [4]

- c) In a centre tapped FWR, the rms half secondary voltage is 10 V. Assuming ideal diodes and load resistance of 2 k $\Omega$ , Find : DC load current, ripple factor and efficiency of rectification. (Refer Q.31 of Chapter 1) [5]

**OR**

- Q.2 a)** Explain the formation of depletion region in unbiased p-n junction diode. (Refer Q.19 of Chapter 1) [5]

- b)** Explain V-I characteristics of p-n junction diode. (Refer Q.22 of Chapter 1) [6]

- c)** Explain the working principle of LED. (Refer Q.42 of Chapter 1) [4]

- Q.3 a)** Sketch and explain the input characteristics of transistor in CE configuration. (Refer Q.11 of Chapter 2) [6]

- b)** Explain the working of a transistor as a switch. (Refer Q.24 of Chapter 2) [5]

- c)** Explain : i) PSRR ii) CMRR iii) Bandwidth  
iv) Output offset voltage (Refer Q.40 of Chapter 2) [4]

**OR**

- Q.4 a)** Explain the working of E-MOSFET as a switch. (Refer Q.33 of Chapter 2) [6]

- b)** Compare CB, CE and CC transistor configurations. (Refer Q.23 of Chapter 2) [4]

- c)** For the inverting amplifier using op-amp if  $R_f = 100 \text{ k}\Omega$ ,  $R_i = 10 \text{ }\Omega$ ,  $V_{cc} = \pm 10 \text{ V}$ ,  $V_t = 2 \text{ V d.c. Calculate :}$

- Output voltage
- Is the result in part (1) Is practically possible ? Justify. (Refer Q.45 of Chapter 2) [5]

## SOLVED SAMPLE QUESTION PAPER - 5 [IN SEMI] [AS PER 2019 PATTERN]

**Time : 1 Hour**

[Maximum Marks : 30]

- Q.1 a)** Define relay and explain the working principle of a relay circuit. (Refer Q.9 of Chapter 1) [5]

**OR**

- b)** A bar of n type silicon has a length of 4 cm and cross-section of  $10 \text{ mm}^2$ . It is subjected to a voltage of 1 V across its length. Find the drift current if mobility of free electrons is  $1300 \text{ cm}^2/\text{V-sec}$  and charge on each electron is  $16 \times 10^{-19} \text{ C}$ . The concentration of free electrons is  $0.9615 \times 10^{21}/\text{m}^3$ . (Refer Q.17 of Chapter 1) [5]

- c)** Describe with the help of neat circuit diagram the operation of zener voltage regulator under varying load and varying input conditions. (Refer Q.38 of Chapter 1) [5]

**OR**

- Q.2 a)** Explain the reverse biasing of a diode. (Refer Q.21 of Chapter 1) [6]

- b)** Draw the circuit of bridge rectifier and explain its operation. Give the input and output waveforms. (Refer Q.32 of Chapter 1) [5]

- c)** Explain the working principle of photodiode (Refer Q.44 of Chapter 1) [6]

- Q.3 a)** With a neat diagram explain output characteristics of npn transistor in CE-configuration. Indicate and explain three regions of operation. (Refer Q.12 of Chapter 2) [6]

- b)** Explain the operation of MOSFET as an amplifier with the help of suitable circuit diagram and waveform. (Refer Q.34 of Chapter 2) [5]

- [6]

- c)** Prove that for an inverting amplifier,  $A_v = -\frac{R_f}{R_i}$ . (Refer Q.44 of Chapter 2) [4]

**OR**

- d)** Explain the working of BJT as a CE amplifier. (Refer Q.25 of Chapter 2) [6]

- b) Calculate the  $\alpha_{dc}$  and  $\beta_{dc}$  for the given transistor for which  
 $I_C = 5 \text{ mA}$ ,  $I_B = 50 \mu\text{A}$  and  $I_{CO} = 1 \mu\text{A}$ .  
 (Refer Q.20 of Chapter 2) [4]

- c) Calculate output voltage 'V<sub>o</sub>' of Op - Amp circuit shown in Fig. 1. Draw I/P and O/P waveforms.  
 (Refer Q.48 of Chapter 2) [5]

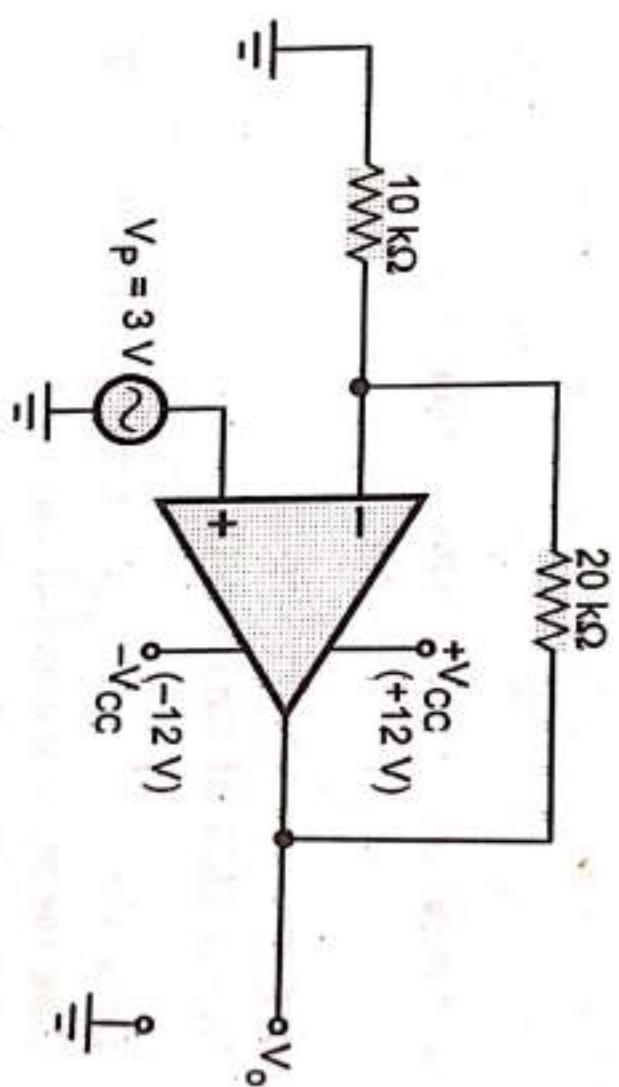


Fig. 1

END... ↗

**UNIT - III****3****Number System  
and Logic Gates****Part A : Number Systems****3.1 : Introduction****Important Points to Remember**

- Number system is a basis for counting various items.
- The decimal number system has 10 digits : 0, 1, 2, 3, 4, 5, 6, 7, 8 and 9.
- Modern computers communicate and operate with binary numbers which use only the digits 0 and 1.
- When decimal quantities are represented in the binary form, they take more digits.
- For large decimal numbers people have to deal with very large binary strings and therefore, they do not like working with binary numbers. This fact gave rise to three new number systems : Octal, Hexadecimal and Binary Coded Decimal (BCD).

Radix (Base) $r$	Characters in set
2 (Binary)	0, 1
3	0, 1, 2
4	0, 1, 2, 3
5	0, 1, 2, 3, 4
6	0, 1, 2, 3, 4, 5
7	0, 1, 2, 3, 4, 5, 6
8 (Octal)	0, 1, 2, 3, 4, 5, 6, 7
9	0, 1, 2, 3, 4, 5, 6, 7, 8
10 (Decimal)	0, 1, 2, 3, 4, 5, 6, 7, 8, 9
:	:
16 (Hexadecimal)	0, 1, 2, 3, 4, 5, 6, 7, 8, 9, A, B, C, D, E, F

Table 3.1 Radix and character set

(3 - I)

- Each number system has  $r$  set of characters. For example, in decimal number system  $r$  equals to 10 has 10 characters from 0 to 9, in binary number system  $r$  equals to 2 has 2 characters 0 and 1 and so on.
- In general we can say that, a number represented in radix  $r$ , has  $r$  characters in its set and  $r$  can be any value. This is illustrated in Table 3.1.
- Table 3.2 shows the relationship between decimal, binary, octal and hexadecimal.

Decimal	Binary	Octal	Hexadecimal
0	0000	0	0
1	0001	1	1
2	0010	2	2
3	0011	3	3
4	0100	4	4
5	0101	5	5
6	0110	6	6
7	0111	7	7
8	1000	10	8
9	1001	11	9
10	1010	12	A
11	1011	13	B
12	1100	14	C
13	1101	15	D
14	1110	16	E
15	1111	17	F

Table 3.2 Relation between decimal, binary, octal and hexadecimal numbers

**3.2 : Binary, Octal, Decimal, Hexadecimal their Conversion**

Q.1 Convert  $(1101.101)_2$  to decimal number and explain the process of conversion.

**Ans. :** • By adding each digit of a binary number in a power of 2 we can find the decimal equivalent of the given binary number.

This is illustrated in Fig. Q.1.1.

$2^3$	$2^2$	$2^1$	$2^0$	$2^{-1}$	$2^{-2}$	$2^{-3}$
1	1	0	1	.	1	0
$1 \times 2^3$	$1 \times 2^2$	$0 \times 2^1$	$1 \times 2^0$	.	$1 \times 2^{-1}$	$0 \times 2^{-2}$

$$N = 1 \times 2^3 + 1 \times 2^2 + 0 \times 2^1 + 1 \times 2^0 + 1 \times 2^{-1} + 0 \times 2^{-2} + 1 \times 2^{-3} = (13.625)_{10}$$

Fig. Q.1.1

**Q.2 Convert  $(5632.471)_8$  to decimal number and explain the process of conversion.**

**Ans. :** • By adding each digit of an octal number in a power of 8 we can find the decimal equivalent of the given octal number. This is illustrated in Fig. Q.2.1.

$8^3$	$8^2$	$8^1$	$8^0$	$8^{-1}$	$8^{-2}$	$8^{-3}$
5	6	3	2	.	4	7
$5 \times 8^3$	$6 \times 8^2$	$3 \times 8^1$	$2 \times 8^0$	.	$4 \times 8^{-1}$	$7 \times 8^{-2}$

$$N = 5 \times 8^3 + 6 \times 8^2 + 3 \times 8^1 + 2 \times 8^0 + 4 \times 8^{-1} + 7 \times 8^{-2} + 1 \times 8^{-3} = (3270.61125)_{10}$$

Fig. Q.2.1

**Q.3 Convert  $(3FD.84)_{16}$  into decimal number and explain the process of conversion.**

**Ans. :** By adding each digit of a hexadecimal number in a power of 16 we can find decimal equivalent of the given hexadecimal number.

$16^2$	$16^1$	$16^0$	$16^{-1}$	$16^{-2}$
3	F	D	.	8
$3 \times 16^2$	$F \times 16^1$	$D \times 16^0$	.	$8 \times 16^{-1}$

$$N = 3 \times 16^2 + F \times 16^1 + D \times 16^0 + 8 \times 16^{-1} + 4 \times 16^{-2}$$

$$= 3 \times 16^2 + 15 \times 16^1 + 13 \times 16^0 + 8 \times 16^{-1} + 4 \times 16^{-2} = (1021.515625)_{10}$$

**Step 2 : Write equivalent octal number for each group of 3-bits.**

$$\therefore (10101101.0111)_2 = (255.34)_8$$

**Q.6 Convert  $(125.62)_8$  to binary and explain the conversion process.**

**Ans. :**

**Step 1 : Write equivalent 3-bit binary number for each octal digit.**

1	2	3	.	6	2
0	0	1	0	1	0

Octal (Base 8)

**Step 2 : Remove any leading or trailing zeros.**

1	0	1	0	1	0	1	.	1	1	0	0
0	0	1	0	1	0	1	.	1	1	0	0

Octal (Base 8)

**Q.7 Convert  $11010110 \cdot 1001101$  to hexadecimal equivalent and explain the conversion process.**

**Ans. :** **Step 1 :** Make group of 4-bits starting from LSB for integer part and MSB for fractional part, by adding 0s at the end, if required.

II)  $(79.515)_{10}$ 

Integer part			Fractional part		
2	79	1 LSD	Fraction	Base	Product
2	39	1	0.515	*	2 = 1.030
2	19	1	0.030	*	2 = 0.060
2	9	1	0.060	*	2 = 0.120
2	4	0	0.120	*	2 = 0.240
2	2	0	0.240	*	2 = 0.480
2	1	1 MSD	0.480	*	2 = 0.960
0			0.960	*	2 = 1.920
			0.920	*	2 = 1.840

$\therefore (79.515)_{10} = (1001111.10000011)_2$

Note : In the example, we have restricted fractional part up to 8 digits. This answer is an approximate answer. To get more accurate answer we have to continue multiplying by 2 until we get fraction 0.

III)  $(109.125)_{10}$ 

Integer part			Fractional part		
2	109	1 LSD	Fraction	Base	Product
2	54	0	0.125	*	2 = 0.250
2	27	1	0.250	*	2 = 0.50
2	13	1	0.50	*	2 = 1.00
2	6	0			
2	3	1			
2	1	1 MSD			
0					

$\therefore (109.125)_{10} = (1101101.001)_2$

Q.12(a) Convert  $(153.513)_{10}$  to an octal number.

Ans. :

Integer part			Fractional part		
Fraction	Base	Product			
8	153	1	0.513	*	8 = 4.104
8	19	3	0.104	*	8 = 0.832
8	2	2	0.832	*	8 = 6.056
0			0.056	*	8 = 5.240

Restricting fractional part up to 4 digits we have

$$\therefore (153.513)_{10} = (231.4065)_8$$

Q.12 (b) Convert the decimal number 32.75 in octal, binary and hexadecimal.

Ans. :

16	32	0 LSB	$0.75 \times 16 = 12.00 \rightarrow C$
16	2	2 MSB	0

$$\therefore (32.75)_{10} = (20.C)_H = (100000.1100)_2 = (40.60)_8$$

**Unsolved Problems**

Q.13 Convert the decimal number 225.225 to binary number.

[Ans.:  $(11100001.00111001)_2$ ]**Drill Problems**Q.14 Determine the value of base x, if :  $(193)_x = (623)_8$ 

Ans. :  $(193)_x = (623)_8$

Converting octal into decimal :  $6 \times 8^2 + 2 \times 8 + 3 = (403)_{10} = (623)_8$ 

$$\therefore (193)_x = 1 \times x^2 + 9 \times x + 3 \times x^0 = (403)_{10}$$

$$\therefore x^2 + 9x + 3 = 403 \quad \therefore x = 16 \text{ or } x = -25$$

Negative is not applicable  $\therefore x = 16$

$$(193)_{10} = (623)_b$$

**Q.16** The solution to the quadratic equation " $x^2 - 11x + 21 = 0$ " are  $x = 3$  and  $x = 6$ . What is the base of the number system used?

Ans. : Let us assume that the base is  $b$ . We have,

$$(x - 3)(x - 6) = x^2 - 11x + 22$$

But 3 and 6 are same in any base, whose value is more than 6.  
i.e.  $(3)_b = (3)_{10}$  and  $(6)_b = (6)_{10}$

$$\therefore (x^2 - 9x + 18)_{10} = (x^2 - 11x + 22)_b$$

Comparing coefficients of  $x$  we have

$$(9)_{10} = (11)_b$$

$$9 = b^1 + b^0 = b^1 + 1$$

$$\therefore b = 8$$

OR

Comparing coefficients of  $x^0$  we have

$$(18)_{10} = (22)_b$$

$$18 = 2 \times b^1 + 2 \times b^0 = 2 \times b^1 + 2$$

$$16 = 2 \times b^1$$

$$\therefore b = 8$$

### 3.3 : Complement of Number

**Q.18** State different ways to represent negative binary number?

Ans. : There are three ways to represent negative numbers:

- Signed - magnitude representation.
- 1's complement representation.
- 2's complement representation.

**Q.19** Find 1's complement of  $(11010100)_2$ .

Ans. : The 1's complement of a binary number is the number that results when we change all 1's to zeros and the zeros to ones.

1	1	0	1	0	1	0	0
▽	▽	▽	▽	▽	▽	▽	▽
0	0	1	0	1	0	1	1

Number

NOT operation

1's complement of number

**Q.18** Find 2's complement of  $(11000100)_2$ .

Ans. : The 2's complement is the binary number that results when we add 1 to the 1's complement.

1	1	0	0	0	1	0	0
					1	1	
0	0	1	1	1	0	1	1
+							1
0	0	1	1	1	1	0	0

Number

Carry

1's complement of number

Add 1

2's complement of number

**Q.19** What is signed magnitude representation? Represent + 9 and - 9 using 8-bit signed - magnitude form.

OR What do you mean by sign magnitude representation? Discuss.

Ans. : In signed magnitude representation most significant bit is used to code sign of a number (1 = negative, 0 = +) and remaining bits are used to represent magnitude of the number in the range of  $+ 2^{n-1}$  to  $- 2^{n-1}$ .

$$+9 = 0\ 000\ 1001$$

$$-9 = 1\ 000\ 1001$$

**Q.21** Represent decimal number "- 13" in all three methods of negative binary number representation using eight bits.

Ans. :

$$\boxed{1\ 0\ 0\ 0\ 1\ 1\ 0\ 1} \quad -13 \text{ in sign magnitude representation}$$

$$\boxed{1\ 1\ 1\ 1\ 0\ 0\ 1\ 0} \quad -13 \text{ in 1's complement representation}$$

$$\boxed{1\ 1\ 1\ 1\ 0\ 0\ 1\ 1} \quad -13 \text{ in 2's complement representation}$$

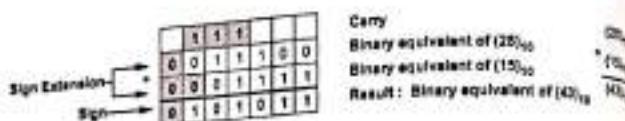
## 3.4 : Binary Arithmetic

**Q.22** Explain the binary addition operation.

- Ans. : 1. Add bits column-wise starting from LSB with carry if any.  
 2. Put the sum at the bottom of the same column.  
 3. Put the carry, if any, on the top of next column.

**Q.23** Add  $(28)_{10}$  and  $(15)_{10}$  by converting them into binary.

Ans. : Using decimal to binary conversion technique we have,  
 $(28)_{10} = (011100)_2$  and  $(15)_{10} = (01111)_2$



**Q.24** State the procedure to perform binary subtraction using 1's complement method.

Ans. : The operation  $A - B$  is performed using 1's complement method as follows :

1. Take 1's complement of B.
2. Result  $\leftarrow A + 1$ 's complement of B.
3. If carry is generated then the result is positive and in the true form. Add carry to the result to get the final result.
4. If carry is not generated then the result is negative and in the 1's complement form.

**Q.25** Perform  $(28)_{10} - (15)_{10}$  using 6-bit 1's complement representation.

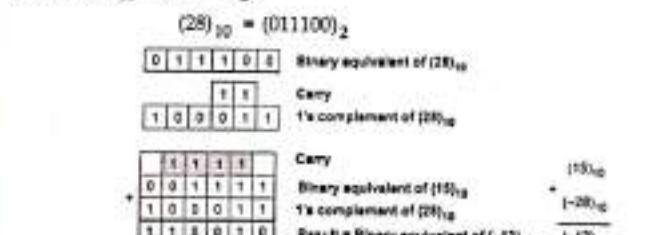
$$\text{Ans. : } (28)_{10} = (011100)_2$$

$$(15)_{10} = (001111)_2$$



**Q.26** Perform  $(15)_{10} - (28)_{10}$  using 6-bit 1's complement representation.

$$\text{Ans. : } (15)_{10} = (001111)_2$$



Verification : 0 0 1 1 0 1 → 1's complement of result (Binary equivalent of  $(13)_{10}$ )

**Q.27** State the procedure to perform binary subtraction using 2's complement method.

Ans. : The operation  $A - B$  is performed using 2's complement method as follows :

1. Take 2's complement of B.
2. Result  $\leftarrow A + 2$ 's complement of B.
3. If carry is generated then the result is positive and in the true form. In this case, carry is ignored.
4. If carry is not generated then the result is negative and in the 2's complement form.

**Q.28** Perform the following subtraction using 2's complement method :

$$0\ 0\ 1\ 0\ 0\ 0 - 0\ 1\ 0\ 0\ 1 \equiv 0\ 0\ 1\ 1\ 0\ 0\ 1 - 0\ 0\ 0\ 1\ 1\ 1\ 1\ 0$$

Ans. : 0 0 1 0 0 0 - 0 1 0 0 1

$$\begin{array}{r}
 \begin{array}{c} 0 & 1 & 0 & 0 & 1 \\ + & 1 & 0 & 1 & 1 & 0 \\ \hline & & & & 1 \\ & 1 & 0 & 1 & 1 & 1 \end{array} \\
 \text{Subtractor} \\
 \text{1's complement of subtractor} \\
 + \\
 \begin{array}{c} 0 & 1 & 0 & 0 & 0 \\ + & 1 & 0 & 1 & 1 & 1 \\ \hline & 1 & 1 & 1 & 1 & 1 \end{array} \\
 \text{Subtrahend} \\
 \text{2's complement of subtractor} \\
 \text{No carry, result is negative and in 2's complement form}
 \end{array}$$

iii) 0 0 1 1 1 0 0 1 - 0 0 0 1 1 1 1 0

$$\begin{array}{r}
 \begin{array}{c} 0 & 0 & 0 & 1 & - & 1 & 1 & 1 & 0 \\ + & 1 & 1 & 1 & 0 & + & 0 & 0 & 0 & 1 \\ \hline & & & & & & 1 \\ & 1 & 1 & 0 & - & 0 & 0 & 1 & 0 \end{array} \\
 \text{Subtractor} \\
 \text{1's complement of subtractor} \\
 \text{Add 1} \\
 \text{2's complement of subtractor} \\
 \begin{array}{c} 1 & 1 & 1 & 1 & 1 & 1 & 1 & 1 \\ + & 0 & 1 & 0 & 1 & 1 & 0 & 0 \\ \hline & 1 & 0 & 1 & 0 & 0 & 1 & 1 \end{array} \\
 \text{Carry} \\
 \text{Subtrahend} \\
 \text{2's complement of subtractor} \\
 \text{Result} \\
 \text{Discard carry} \quad \boxed{\times} \quad 0 0 0 1 1 1 1 1 \\
 \dots 0011-1001-0001-1110 = 0001-1011
 \end{array}$$

Q.29 Perform following arithmetic operation in binary using sign 2's complement representation : (- 42) - (- 13)

Ans. :

$$\begin{array}{r}
 \begin{array}{c} 0 & 1 & 0 & 1 & 0 & 1 & 0 \\ + & 1 & 0 & 1 & 0 & 1 & 0 & 1 \\ \hline & & & & 1 \\ & 1 & 0 & 1 & 0 & 1 & 1 & 0 \end{array} \\
 + 42 \\
 \text{1's complement of 42} \\
 + \\
 \begin{array}{c} 1 & 1 & 1 & 1 & 1 & 1 & 1 \\ + & 0 & 0 & 0 & 1 & 0 & 1 & 1 \\ \hline & 1 & 1 & 0 & 1 & 0 & 0 & 0 \end{array} \\
 \text{Add 1} \\
 \text{2's complement of 42} \\
 \begin{array}{c} 1 & 1 & 1 & 1 & 1 & 1 & 1 \\ + & 0 & 1 & 0 & 1 & 1 & 0 & 1 \\ \hline & 1 & 0 & 1 & 0 & 0 & 1 & 1 \end{array} \\
 \text{Carry} \\
 13 \\
 \text{2's complement of 42} \\
 \text{No carry, result is negative and in 2's complement form}
 \end{array}$$

$- 42 - (- 13) = - 42 + 13$

$(+13)_{10} = (0001101)_2$

$(+ 42)_{10} = (0101010)_2$

Q.29 (a) Perform the subtraction using 2's complement 46 - 23.

Ans. :  $(46)_{10} = (0101110)_2$

$(23)_{10} = (010111)_2$

$$\begin{array}{r}
 \begin{array}{c} 0 & 1 & 0 & 1 & 1 & 1 \\ + & 1 & 0 & 1 & 0 & 0 & 0 \\ \hline & & & & 1 \\ & 1 & 0 & 1 & 0 & 0 & 1 \end{array} \\
 \text{1's complement of } (23)_{10} \\
 \text{Add 1} \\
 \text{2's complement of } (23)_{10}
 \end{array}$$

$$\begin{array}{r}
 \begin{array}{c} 1 & 1 & 1 & 1 & 1 & 1 \\ + & 0 & 1 & 0 & 1 & 1 & 0 \\ \hline & 1 & 1 & 0 & 1 & 0 & 1 \end{array} \\
 \text{Carry} \\
 \text{Sign extension} \rightarrow \boxed{\times} \\
 \begin{array}{c} 0 & 0 & 1 & 0 & 1 & 1 & 1 \\ + & 0 & 0 & 1 & 0 & 1 & 1 & 1 \end{array} \\
 \text{Discard carry} \rightarrow \boxed{\times} \\
 \text{Result} = (23)_{10}
 \end{array}$$

Fig. Q.29(a).1

## Unsolved Problem

Q.30 Perform the following operations by using 2's complement method : i) 46 - 23 ii) 21 - 42

[Ans. : i)  $(10111)_2$  ii)  $(101011)_2$  in 2's complement form]

## 3.5 : BCD (Binary Coded Decimal) Number

Q.31 What is BCD Code ? State its advantages and disadvantages.

Ans. : • BCD is an abbreviation for binary coded decimal.

• BCD is a numeric code in which each digit of a decimal number is represented by a separate group of 4-bits. The most common BCD code is 8-4-2-1 BCD.

• It is called 8-4-2-1 BCD because the weights associated with 4 bits are 8-4-2-1 from left to right. This means that, bit-3 has weight 8, bit-2 has weight 4 bit-1 has weight 2 and bit-0 has weight 1.

- Table Q.31.1 shows the 4-bit 8-4-2-1 BCD code used to represent a single decimal digit.

Decimal	BCD code			
Digit	8	4	2	1
0	0	0	0	0
1	0	0	0	1
2	0	0	1	0
3	0	0	1	1
4	0	1	0	0
5	0	1	0	1
6	0	1	1	0
7	0	1	1	1
8	1	0	0	0
9	1	0	0	1

Table Q.31.1 8-4-2-1 BCD code

- In multi-digit coding, each decimal digit is individually coded with 8-4-2-1 BCD code, as shown in the Fig. Q.31.1. Total 8-bits are required to encode  $58_{10}$  in 8-4-2-1 BCD.

Decimal	5	8
8-4-2-1 BCD	0 1 0 1	1 0 0 0

Fig. Q.31.1

**Advantages**

- Easy to convert BCD to decimal and vice versa.

**Disadvantages**

- Since it requires more binary digits to represent multi-digit number than binary number system. It is less efficient for example, to represent the same number (58) in binary :  $111010_2$  we require only 6 digits.
- Arithmetic operations are more complex.

**3.6 : De-Morgan's Theorem**

Q.32 State and prove DeMorgan's theorem.

CB [SPPU : May-18, Dec-18, Marks 2]

Ans. : DeMorgan suggested two theorems that form an important part of Boolean algebra. In the equation form, they are :

- $AB = \bar{A} + \bar{B}$  : The complement of a product is equal to the sum of the complements. This is illustrated by truth Table Q.32.1.

Truth table :

A	B	$\bar{A}B$	$\bar{A} + \bar{B}$
0	0	1	1
0	1	1	1
1	0	1	1
1	1	0	0

LHS = RHS

Table Q.32.1

- $A + B = \bar{A} \cdot \bar{B}$  : The complement of a sum is equal to the product of the complements. The truth Table Q.32.2 illustrates this law.

Truth table :

A	B	$A + B$	$\bar{A} \cdot \bar{B}$
0	0	1	1
0	1	0	0
1	0	0	0
1	1	0	0

LHS = RHS

Table Q.32.2

Q.33 Use De-Morgan's theorem to simplify the following Boolean expression.

CB [SPPU : Dec-09, 12, Marks 6]

Ans. :  $Y = \overline{AB} + \overline{AB}$

$$\begin{aligned}
 Y &= \overline{AB} + \overline{AB} = \overline{AB} \cdot \overline{AB} = (\overline{A} + \overline{B}) \cdot (\overline{A} + \overline{B}) = (\overline{A} + \overline{B}) \cdot (\overline{A} + \overline{B}) \\
 &= \overline{AA} + \overline{AB} + \overline{A}\overline{B} + \overline{BB} = AB + \overline{A}\overline{B}
 \end{aligned}$$

Q.34 Prove the following using DeMorgan's theorem.

$$1. AB+CD = \overline{AB} \cdot \overline{CD}$$

$$2. (A+B) \cdot (C+D) = \overline{(A+B)} + \overline{(C+D)}$$

GATE [SPPU : Dec-10, May-06, Marks 10]

Ans. 1.  $AB+CD = \overline{AB} \cdot \overline{CD}$

$$\begin{aligned} &= \overline{AB} \cdot \overline{CD} \\ &\quad \dots A = \overline{A} \\ &\quad \dots \overline{A+B} = \overline{\overline{A} \cdot \overline{B}} \\ &\quad \dots \overline{A} = A \\ 2. \quad (A+B) \cdot (C+D) = (A+B) \cdot (C+D) \\ &\quad = (A+B) + (C+D) \quad \dots \overline{A \cdot B} = \overline{A} + \overline{B} \end{aligned}$$

Q.35 Prove the following using De Morgan's theorem :

$$(A+B) \cdot (C+D) = (\overline{A} \cdot \overline{B}) + (\overline{C} \cdot \overline{D})$$

GATE [SPPU : Dec-15, Marks 2]

$$\begin{aligned} \text{L.H.S.} &= (A+B) \cdot (C+D) = (A+B) + (C+D) \\ &= (\overline{A} \cdot \overline{B}) + (\overline{C} \cdot \overline{D}) = \text{R.H.S.} \end{aligned}$$

### Part B : Logic Gates and Adder Circuits

#### 3.7 : Logic Gates

##### Logic Gates

NOT gate (Inverter) : The output is a complement of input.

Logic Diagram (Symbol)	Switch Equivalent	Truth Table						
 <b>Pin Diagram</b> <b>IC 7404</b>		<table border="1"> <thead> <tr> <th>Input</th><th>Output</th></tr> </thead> <tbody> <tr> <td>0</td><td>1</td></tr> <tr> <td>1</td><td>0</td></tr> </tbody> </table> <b>Boolean Expression</b> $Y = \overline{A}$	Input	Output	0	1	1	0
Input	Output							
0	1							
1	0							

**Application :**  
Used to complement (invert) digital signal.

**AND gate :** The output is high only when all inputs are high.

Logic Diagram (Symbol)	Switch Equivalent	Truth Table										
 <b>Pin Diagram</b> <b>IC 7400</b>		<table border="1"> <thead> <tr> <th>Input</th><th>Output</th></tr> </thead> <tbody> <tr> <td>0 0</td><td>0</td></tr> <tr> <td>0 1</td><td>0</td></tr> <tr> <td>1 0</td><td>0</td></tr> <tr> <td>1 1</td><td>1</td></tr> </tbody> </table> <b>Boolean Expression</b> $Y = A \cdot B$	Input	Output	0 0	0	0 1	0	1 0	0	1 1	1
Input	Output											
0 0	0											
0 1	0											
1 0	0											
1 1	1											

**OR gate :** The output is high when any of the inputs is high.

Logic Diagram (Symbol)	Switch Equivalent	Truth Table										
 <b>Pin Diagram</b> <b>IC 7432</b>		<table border="1"> <thead> <tr> <th>Input</th><th>Output</th></tr> </thead> <tbody> <tr> <td>0 0</td><td>0</td></tr> <tr> <td>0 1</td><td>1</td></tr> <tr> <td>1 0</td><td>1</td></tr> <tr> <td>1 1</td><td>1</td></tr> </tbody> </table> <b>Boolean Expression</b> $Y = A + B$	Input	Output	0 0	0	0 1	1	1 0	1	1 1	1
Input	Output											
0 0	0											
0 1	1											
1 0	1											
1 1	1											

Buffer : The output is same as input.														
Symbol	Boolean Expression	Truth Table												
	$Y = A$	<table border="1"> <thead> <tr> <th>Input</th><th>Output</th></tr> </thead> <tbody> <tr> <td>A</td><td>Y</td></tr> <tr> <td>1</td><td>1</td></tr> <tr> <td>1</td><td>1</td></tr> </tbody> </table>	Input	Output	A	Y	1	1	1	1				
Input	Output													
A	Y													
1	1													
1	1													
Application : It is used to increase output driving capacity.														
NAND gate : The output is high only when one of the inputs is low.														
Symbol	Boolean Expression	Truth Table												
	$Y = \overline{A \cdot B}$	<table border="1"> <thead> <tr> <th>Input</th><th>Output</th></tr> </thead> <tbody> <tr> <td>A B</td><td>Y</td></tr> <tr> <td>0 0</td><td>1</td></tr> <tr> <td>0 1</td><td>1</td></tr> <tr> <td>1 0</td><td>1</td></tr> <tr> <td>1 1</td><td>0</td></tr> </tbody> </table>	Input	Output	A B	Y	0 0	1	0 1	1	1 0	1	1 1	0
Input	Output													
A B	Y													
0 0	1													
0 1	1													
1 0	1													
1 1	0													
Application : It can be used to implement any digital circuit.														
NOR Gate : The output is high when all the inputs are low.														
Symbol	Boolean Expression	Truth Table												
	$Y = \overline{A + B}$	<table border="1"> <thead> <tr> <th>Input</th><th>Output</th></tr> </thead> <tbody> <tr> <td>A B</td><td>Y</td></tr> <tr> <td>0 0</td><td>1</td></tr> <tr> <td>0 1</td><td>0</td></tr> <tr> <td>1 0</td><td>0</td></tr> <tr> <td>1 1</td><td>0</td></tr> </tbody> </table>	Input	Output	A B	Y	0 0	1	0 1	0	1 0	0	1 1	0
Input	Output													
A B	Y													
0 0	1													
0 1	0													
1 0	0													
1 1	0													
Application : It can be used to implement any digital circuit.														

A Guide for Engineering Students

TECHNICAL PUBLICATIONS

Exclusive OR (EX-OR) gate : The output is high only when odd number of inputs are high.														
Symbol	Boolean Expression	Truth Table												
	$Y = A \oplus B$	<table border="1"> <thead> <tr> <th>Input</th><th>Output</th></tr> </thead> <tbody> <tr> <td>A B</td><td>Y</td></tr> <tr> <td>0 0</td><td>0</td></tr> <tr> <td>0 1</td><td>1</td></tr> <tr> <td>1 0</td><td>1</td></tr> <tr> <td>1 1</td><td>0</td></tr> </tbody> </table>	Input	Output	A B	Y	0 0	0	0 1	1	1 0	1	1 1	0
Input	Output													
A B	Y													
0 0	0													
0 1	1													
1 0	1													
1 1	0													
Application : It is used to implement magnitude comparator, gray code converter, adder/subtractor circuits, parity generator, modulo-2 adder, etc.														
Exclusive NOR (EX-NOR) gate : The output is high only when even number of ones at the input or all inputs are high.														
Symbol	Boolean Expression	Truth Table												
	$Y = \overline{A \oplus B}$	<table border="1"> <thead> <tr> <th>Input</th><th>Output</th></tr> </thead> <tbody> <tr> <td>A B</td><td>Y</td></tr> <tr> <td>0 0</td><td>1</td></tr> <tr> <td>0 1</td><td>0</td></tr> <tr> <td>1 0</td><td>0</td></tr> <tr> <td>1 1</td><td>1</td></tr> </tbody> </table>	Input	Output	A B	Y	0 0	1	0 1	0	1 0	0	1 1	1
Input	Output													
A B	Y													
0 0	1													
0 1	0													
1 0	0													
1 1	1													
Applications : It is used to implement even parity generator, comparator, even parity checker, etc.														
Note : Ex-Or and EX - NOR gate are also known as mutually exclusive gates.														

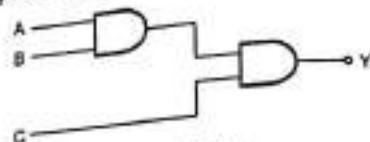
Q.36 Realize a 3-input gate using 2-input gates for the following  
1) AND 2) OR 3) NAND 4) NOR

CB [SPPU : Dec.-06, Marks 8]

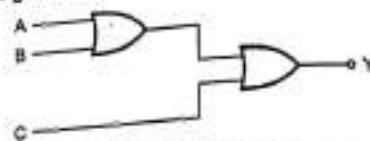
A Guide for Engineering Students

TECHNICAL PUBLICATIONS

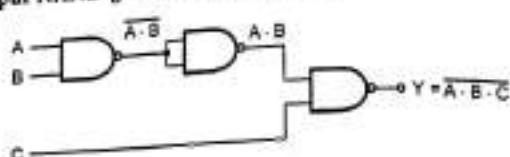
Ans. : 1) 3-input AND gate using 2-input gates :



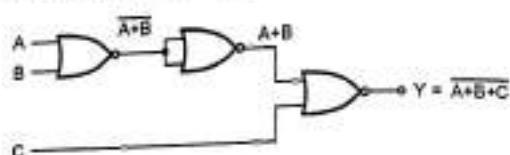
2) 3-input OR gate using 2-input gates :



3) 3-input NAND gate using 2-input gates :



4) 3-input NOR gate using 2-input gates :



Q.37 The voltage waveforms shown in Fig. Q.37.1 are applied at the inputs of 2-input AND and EX-OR gates. Determine the output waveform in each case.  
ESE [SPPU : May-07, Marks 1]

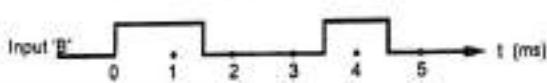
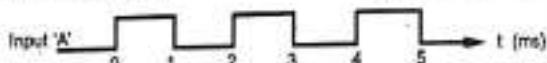


Fig. Q.37.1

Ans. :

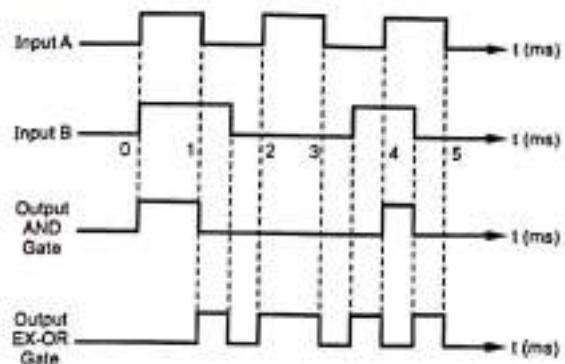


Fig. Q.37.1 (a)

Q.38 Write down the truth table for 3-input EX-OR gate.

ESE [SPPU : May-05, Marks 3]

Ans. :

A	B	C	Y
0	0	0	0
0	0	1	1
0	1	0	1
0	1	1	0
1	0	0	1
1	0	1	0
1	1	0	0
1	1	1	1

Table Q.38.1

Q.39 Make truth table for a 3 input :

1) AND gate, 2) OR gate, 3) NAND gate, 4) NOR gate.

ESE [SPPU : May-06, Marks 8]

Ans. :

A	B	C	Y
0	0	0	0
0	0	1	0
0	1	0	0
0	1	1	0
1	0	0	0
1	0	1	1
1	1	0	1
1	1	1	1

3 input AND

A	B	C	Y
0	0	0	0
0	0	1	1
0	1	0	1
0	1	1	1
1	0	0	1
1	0	1	0
1	1	0	0
1	1	1	0

3 input OR

Fig. Q.39.1 Truth table

Q.40 Prove that a positive logic NAND is equivalent to a negative logic NOR operation and vice versa.  
ESE [SPPU : May-06, Marks 6]

Ans. : Let us see the truth tables for 2-input NAND gate and 2-input NOR gate with positive logic.

A	B	Y
0	0	1
0	1	1
1	0	1
1	1	0

Truth table for NAND gate with positive logic

A	B	Y
0	0	1
0	1	0
1	0	0
1	1	0

Truth table for NOR gate with positive logic

Now see the truth tables for 2-input NAND gate and 2-input NOR gate with negative logic.

A	B	Y
1	1	0
1	0	0
0	1	0
0	0	1

Truth table for NAND gate with negative logic

A	B	Y
1	1	0
1	0	1
0	1	1
0	0	1

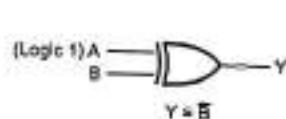
Truth table for NOR gate with negative logic

The truth tables for positive logic NAND gate and negative logic NOR gates are equivalent and vice versa.

Q.41 Explain how EX-OR gate can be used as an inverter.

ESE [SPPU : May-16, Marks 2]

Ans. : By connecting one input of EX-OR gate to logic 1 we can use EX-OR gate as an inverter. For EX-OR gate, when two inputs are different output is logic 1.



A	B	Y
1	0	1
1	1	0

Inverter operation

### 3.8 : Universal Gates

Q.42 What do you mean by universal gates? Show the implementation of basic gates using universal gates.

ESE [SPPU : Dec.-05, 16 May-07, 11, Marks 6]

Ans. : \* The NAND and NOR gates are known as universal gates, since any logic function can be implemented using NAND or NOR gates.

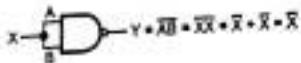


Fig. Q.42.1 NOT function using NAND gate

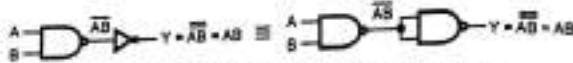


Fig. Q.42.2 AND function using NAND gates



Fig. Q.42.3 OR function using only NAND gates

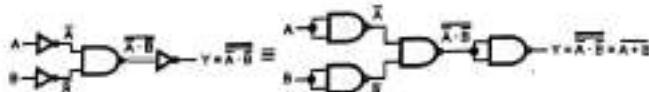


Fig. Q.42.4 NOR function using only NAND gates

- The NOR gate is also a universal gate, since it can be used to generate the NOT, AND, OR and NAND functions.

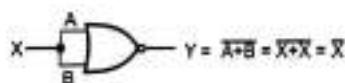


Fig. Q.42.5 NOT function using NOR gate

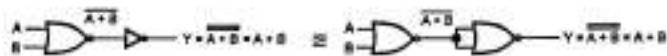


Fig. Q.42.6 OR function using NOR gates

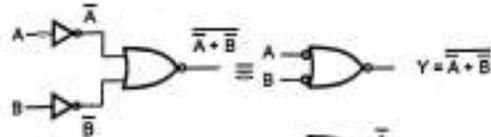


Fig. Q.42.7 AND function using NOR gates

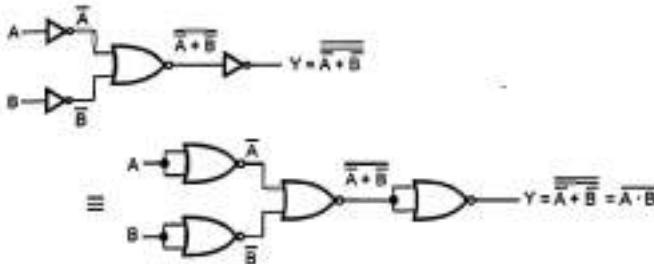


Fig. Q.42.8 NAND function using only NOR gates

**Q.43 Implement EX-OR gate using only NAND gates.**

OR Draw 2 Input Ex-OR gate, write logic equation and implement using basic logic gates.  
E&E [SPPU : May-18, Marks 6]

Ans. : The Boolean expression for EX-OR gate is :

$$Y = A\bar{B} + \bar{A}B$$

We can implement AND-OR logic by using NAND-NAND logic as shown in Fig. Q.43.1 (b).

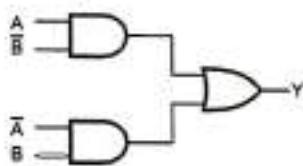


Fig. Q.43.1 (a)

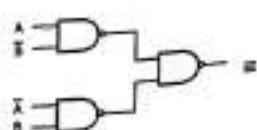


Fig. Q.43.1 (b)

**Q.44 Implement EX-NOR gate using only NAND gates.**

**Ans.:** The Boolean expression for EX-NOR gate is  $Y = AB + \bar{A}\bar{B}$ . We can implement AND-OR logic by using NAND-NAND logic as shown in Fig. Q.44.1.

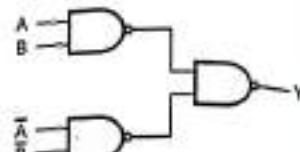


Fig. Q.44.1

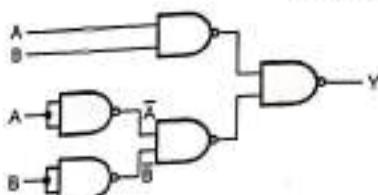


Fig. Q.44.1 (a)

**Q.45 Implement EX-NOR gate using only NOR gates.**

**Ans.:** The Boolean expression for EX-NOR gate is :

$$\begin{aligned} Y &= AB + \bar{A}\bar{B} = \overline{\bar{A}B + A\bar{B}} \\ &= \overline{\bar{A}B} \cdot \overline{A\bar{B}} = (\bar{A} + B) \cdot (A + \bar{B}) \end{aligned}$$

We can implement OR-AND logic by using NOR-NOR logic, as shown in Fig. Q.45.1 (b).

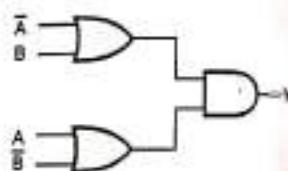


Fig. Q.45.1 (b)

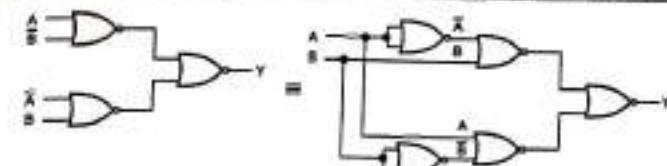


Fig. Q.45.1 (b)

**Q.46 Implement EX-OR gate using only NOR gates.**

**Ans.:** Boolean expression of EX-OR gate  $Y = AB + \bar{A}\bar{B} = \overline{AB + \bar{A}\bar{B}} = \overline{AB} \cdot \overline{\bar{A}\bar{B}} = (\bar{A} + B) \cdot (A + \bar{B})$

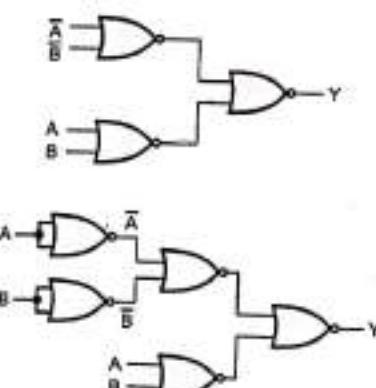


Fig. Q.46.1

### 3.9 : Half Adder and Full Adder

**Q.47 What is the difference between half adder and full adder.**

**CBT [SPPU : June-10, Marks 4]**

**Ans.:** \* The logic circuit which performs addition of two bits is called a half-adder.

\* The circuit which performs addition of three bits (two significant bits and a previous carry) is a full-adder.

Q.48 Implement half adder using gates, truth table and give equations for sum and carry.

EE [SPPU : Dec-18, Marks 8]

OR Design half adder circuit.

EE [SPPU : Dec-06, May-07, 08, Marks 8]

Ans. : \* The half-adder operation needs two binary inputs : augend and addend bits; and two binary outputs : sum and carry. The truth table shown in Table Q.48.1 gives the relation between input and output variables for half-adder operation.

Inputs		Outputs	
A	B	Carry	Sum
0	0	0	0
0	1	0	1 ( $\bar{A}B$ )
1	0	0	1 ( $A\bar{B}$ )
1	1	1 ( $AB$ )	0

Table Q.48.1 Truth table for half-adder

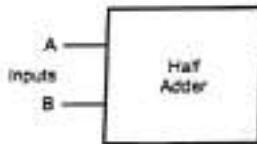


Fig. Q.48.1 Block schematic of half-adder



Fig. Q.48.1 (b) Logic diagram for half-adder

Q.49 Draw half adder using NAND gates.

EE [SPPU : Dec-11, May-12, Marks 4]

Ans. : For half adder :

$$\begin{aligned}\text{Sum} &= A\bar{B} + \bar{A}B \\ &= \overline{AB + \bar{AB}} \\ &= \overline{A \cdot \bar{B} + \bar{A} \cdot B}\end{aligned}$$

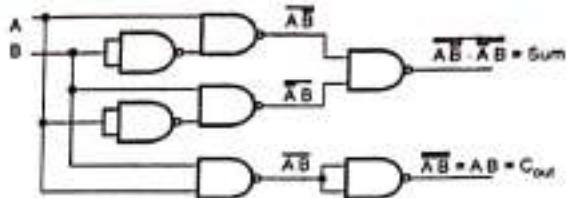


Fig. Q.49.1

Q.50 Implement full adder using basic gates along with its truth table and write the equations for sum and carry.

EE [SPPU : Dec-04, 05, 07, 09, 17, Marks 8, May-05, 19, June-10, Marks 6]

Ans. : \* A full-adder is a combinational circuit that forms the arithmetic sum of three input bits. It consists of three inputs and two outputs. Two of the input variables, denoted by A and B, represent the two significant bits to be added. The third input  $C_{in}$  represents the carry from the previous lower significant position. The truth table for full-adder is shown in Table Q.50.1.

Inputs			Outputs	
A	B	$C_{in}$	Carry	Sum
0	0	0	0	0
0	0	1	0	1
0	1	0	0	1
0	1	1	1	0
1	0	0	0	1
1	0	1	1	0
1	1	0	1	0
1	1	1	1	1

Table Q.50.1 Truth table for full-adder

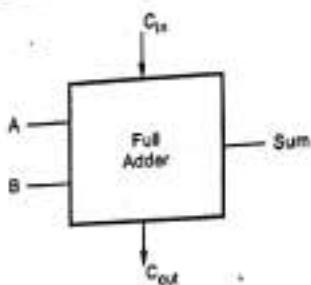


Fig. Q.50.1 Block schematic of full-adder

$$\begin{aligned} \text{Carry} &= \overline{A}B C_{in} + A \overline{B} C_{in} + A B \overline{C}_{in} + A B C_{in} \\ &= (\overline{A}B C_{in} + A B C_{in}) + (A \overline{B} C_{in} + A B C_{in}) + (A B \overline{C}_{in} + A B C_{in}) \\ &\dots A + A = A \\ &= B C_{in} (\overline{A} + A) + A C_{in} (\overline{B} + B) + A B (\overline{C}_{in} + C_{in}) \\ &= B C_{in} + A C_{in} + AB \quad \dots A + \overline{A} = 1 \end{aligned}$$

Logic Diagram:

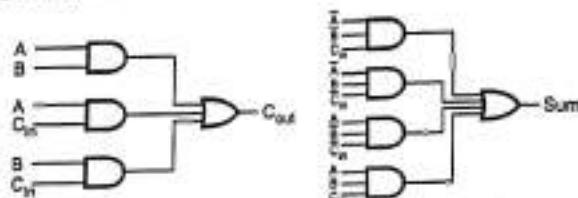


Fig. Q.50.1 (a) Sum of product implementation of full-adder

## Q.51 Realize full adder using EX-OR and basic gates.

Ans. : The Boolean function for sum can be further simplified as follows :

$$\begin{aligned} \text{Sum} &= \overline{A} \overline{B} C_{in} + \overline{A} B \overline{C}_{in} + A \overline{B} \overline{C}_{in} + A B C_{in} \\ &= C_{in} (\overline{A} \overline{B} + AB) + \overline{C}_{in} (\overline{A} B + A \overline{B}) \\ &= C_{in} (A \cdot B) + \overline{C}_{in} (A \oplus B) \end{aligned}$$

- $C_{in} (\overline{A} \oplus B) + \overline{C}_{in} (A \oplus B)$
- $C_{in} \oplus (A \oplus B)$

We have carry =  $B C + A C_{in} + AB$ 

\* With this simplified Boolean function circuit for full-adder can be implemented as shown in the Fig. Q.51.1.

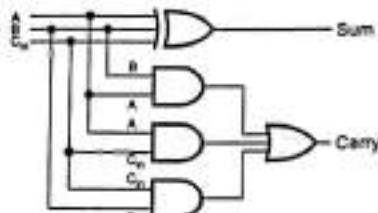


Fig. Q.51.1 Implementation of full-adder

## Q.52 Draw and explain full adder using two half-adders.

CBT [SPPU : May-13, 15, Dec-15, Marks 8]

Ans. : A full-adder can also be implemented with two half-adders and one OR gate, as shown in the Fig. Q.52.1. The sum output from the second half-adder is the exclusive-OR of  $C_{in}$  and the output of the first half-adder, giving

$$\begin{aligned} \text{Sum} &= C_{in} \oplus (A \oplus B) \\ &= \overline{A} \overline{B} C_{in} + \overline{A} B \overline{C}_{in} + A \overline{B} \overline{C}_{in} + A B C_{in} \end{aligned}$$

and the carry output is

$$\begin{aligned} C_{out} &= AB + C_{in} (\overline{A} \overline{B} + \overline{A} B) \\ &= AB + A \overline{B} C_{in} + \overline{A} B C_{in} \\ &= AB (C_{in} + 1) + A \overline{B} C_{in} + \overline{A} B C_{in} \quad \because C_{in} + 1 = 1 \\ &= AB C_{in} + AB + A \overline{B} C_{in} + \overline{A} B C_{in} \\ &= AB + A C_{in} (\overline{B} + \overline{B}) + \overline{A} B C_{in} \\ &= AB + A C_{in} + \overline{A} B C_{in} \\ &= AB (C_{in} + 1) + A C_{in} + \overline{A} B C_{in} \quad \because C_{in} + 1 = 1 \end{aligned}$$

$$\begin{aligned}
 &= ABC_{in} + AB + A C_{in} + \bar{A} BC_{in} \\
 &= AB + A C_{in} + BC_{in} (A + \bar{A}) \\
 &= AB + A C_{in} + BC_{in}
 \end{aligned}$$

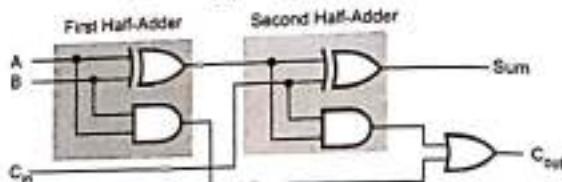


Fig. Q52.1 Implementation of a full-adder with two half-adders and an OR gate

Q53 Realize full adder circuit using NAND gates.

Ans. : We have,  $C_{out} = AB + AC_{in} + BC_{in}$   
 $Sum = \bar{A} \bar{B} C_{in} + \bar{A} B \bar{C}_{in} + A \bar{B} C_{in} + A B C_{in}$

We can implement AND-OR logic using NAND-NAND logic.

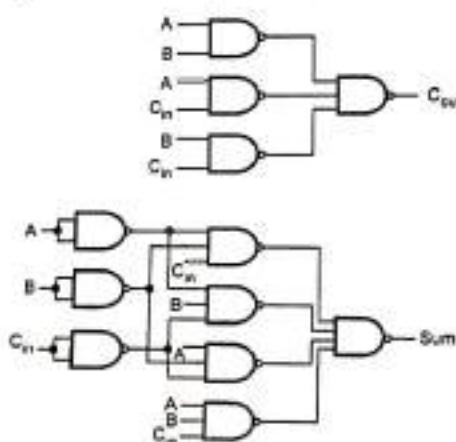


Fig. Q53.1

### Part C : Flip-Flops and Introduction to Microprocessor and Microcontroller

#### 3.10 : Introduction to Flip-Flops

Q54 Name the two storage elements.

Ans. : 1. Latches 2. Flip-Flop.

Q55 What is Flip-Flop ?

Ans. : Flip-flop is a sequential circuit driven by clock input either by positive edge or negative edge. It is a binary storage device capable of storing one bit of information.

#### 3.11 : SR Flip-Flop

Q56 Draw and explain the working of SR flip-flop.

Ans. : Fig. Q56.1 shows the positive edge triggered clocked SR flip-flop.

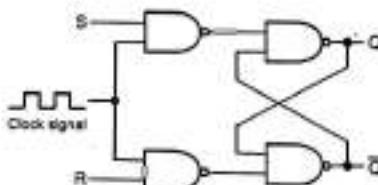


Fig. Q56.1 SR flip-flop using NAND gates

#### Operation

**Case 1 :** If  $S = R = 0$  and the clock pulse is applied, the output do not change, i.e.  $Q_{n+1} = Q_n$ . This is indicated in the first row of the truth table.

**Case 2 :** If  $S = 0$ ,  $R = 1$  and the clock pulse is applied,  $Q_{n+1} = 0$ . This is indicated in the second row of the truth table.

**Case 3 :** If  $S = 1$ ,  $R = 0$  and the clock pulse is applied,  $Q_{n+1} = 1$ . This is indicated in the third row of the truth table.

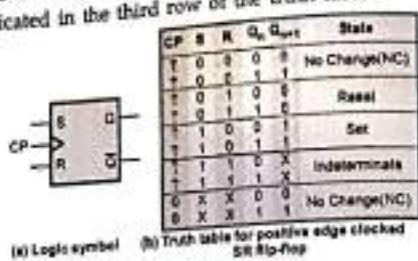


Fig. Q.56.1

**Case 4 :** If  $S = R = 1$  and the clock pulse is applied, the state of the flip-flop is undefined and therefore is indicated as indeterminate in the fourth row of the truth table.

### 3.12 : D Flip-Flop

Q.57 Draw and explain the operation of D-flip-flop.  
ECE [SPPU : Dec.-09, Marks 4]

**Ans. :** In SR Flip-Flop, when both inputs are same the output either does not change or it is invalid (Inputs  $\rightarrow 00$ , no change and inputs  $\rightarrow 11$ , invalid).

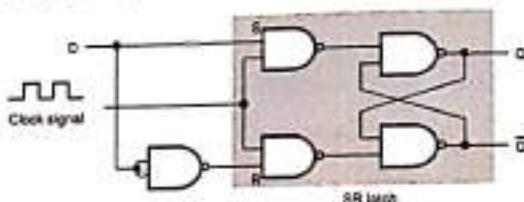


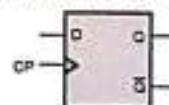
Fig. Q.57.1 D flip-flop using NAND gates

- These input conditions can be avoided by making the complement of each other. This modified SR flip-flop is known as D flip-flop.

- The D input goes directly to the S input, and its complement is applied to the R input. Due to these connections, only two input conditions exists, either  $S = 0$  and  $R = 1$  or  $S = 1$  and  $R = 0$ .

#### Truth Table :

- The truth table for D flip-flop consider only these two conditions and it is as shown in the Fig. Q.57.1 (b).



CP	D	$Q_{n+1}$
T	0	0
T	1	1
0	X	$Q_n$

Fig. Q.57.1 (a) Logic symbol Fig. Q.57.1 (b) Truth table of D flip-flop

- $Q_{n+1}$  function follows D input at the positive going edges of the clock pulses. Hence the characteristic equation for D flip-flop is  $Q_{n+1} = D$ .

### 3.13 : JK Flip-Flop

Q.58 Explain the operation of JK flip-flop.

**Ans. :** The uncertainty in the state of an SR flip-flop when  $S = R = 1$  can be eliminated by converting it into a JK flip-flop. The data inputs are J and K which are ANDed with  $Q$  and  $Q$ , respectively, to obtain S and R inputs, as shown in the Fig. Q.58.1. Thus,  $S = J \cdot \bar{Q}$  and  $R = K \cdot Q$ .

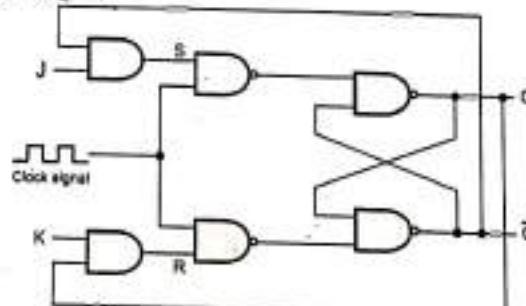


Fig. Q.58.1 Clocked JK flip-flop

**Operation :****Case 1 :  $J = K = 0$** 

When  $J = K = 0$ ,  $S = R = 0$  and according to truth table of SR flip-flop there is no change in the output.

**When inputs  $J = K = 0$ , output does not change.**

**Case 2 :  $J = 1$  and  $K = 0$** 

$Q = 0, \bar{Q} = 1$  : When  $J = 1, K = 0$  and  $Q = 0, S = 1$  and  $R = 0$ . According to truth table of SR flip-flop it is set state and the output  $Q$  will be 1.

$Q = 1, \bar{Q} = 0$  : When  $J = 1, K = 0$  and  $Q = 1, S = 0$  and  $R = 0$ . Since  $SR = 00$ , there is no change in the output and therefore,  $Q = 1$  and  $\bar{Q} = 0$ .

**The inputs  $J = 1$  and  $K = 0$ , makes  $Q = 1$ , i.e. set state.**

**Case 3 :  $J = 0$  and  $K = 1$** 

$Q = 0, \bar{Q} = 1$  : When  $J = 0, K = 1$  and  $Q = 0, S = 0$  and  $R = 0$ . Since  $SR = 00$ , there is no change in the output and therefore,  $Q = 0$  and  $\bar{Q} = 1$ .

$Q = 1, \bar{Q} = 0$  : When  $J = 0, K = 1$  and  $Q = 1, S = 0$  and  $R = 1$ . According to truth table of SR flip-flop it is a reset state and the output  $Q$  will be 0.

**The inputs  $J = 0$  and  $K = 1$ , makes  $Q = 0$ , i.e. reset state.**

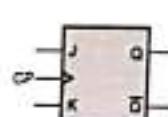
**Case 4 :  $J = K = 1$** 

$Q = 0, \bar{Q} = 1$  : When  $J = K = 1$  and  $Q = 0, S = 1$  and  $R = 0$ . According to truth table of SR flip-flop it is a set state and the output  $Q$  will be 1.

$Q = 1, \bar{Q} = 0$  : When  $J = K = 1$  and  $Q = 1, S = 0$  and  $R = 1$ . According to truth table of SR flip-flop it is a reset state and the output  $Q$  will be 0.

**The input  $J = K = 1$ , toggles the flip-flop output.**

- Fig. Q.58.2 shows logic symbol, truth table and input/output waveforms for positive edge triggered JK flip-flop.



(a) Logic symbol

$Q_0$	$J$	$K$	$Q_{out}$
0	0	0	0
0	0	1	0
0	1	0	1
0	1	1	1
1	0	0	1
1	0	1	0
1	1	0	1
1	1	1	0

$J$	$K$	$Q_{out}$
0	0	0
0	1	0
1	0	1
1	1	1

(b) Truth table

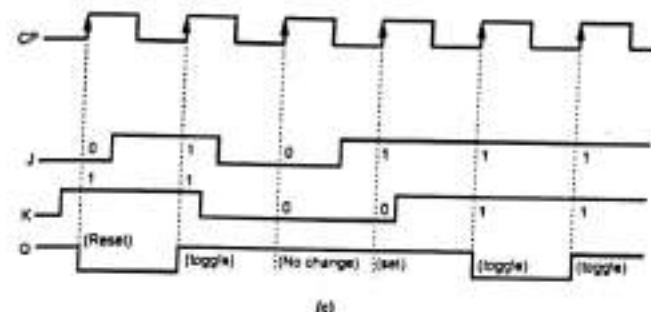


Fig. Q.58.2 Input and output waveforms for positive edge triggered JK flip-flop

**Q.59 What is race around condition ? Explain in brief.**

Ans. : \* In JK flip-flop, when  $J = K = 1$ , the output toggles (output changes either from 0 to 1 or from 1 to 0).

\* Consider that initially  $Q = 0$  and  $J = K = 1$ . After a time interval  $\Delta t$  equal to the propagation delay through two NAND gates in series, the output will change to  $Q = 1$  and after another time interval of  $\Delta t$  the output will change back to  $Q = 0$ . This toggling will continue until the flip-flop is enabled and  $J = K = 1$ . At the end of clock pulse the flip-flop is disabled and the value of  $Q$  is uncertain. This situation is referred to as the race-around condition. This is illustrated in Fig. Q.59.1.

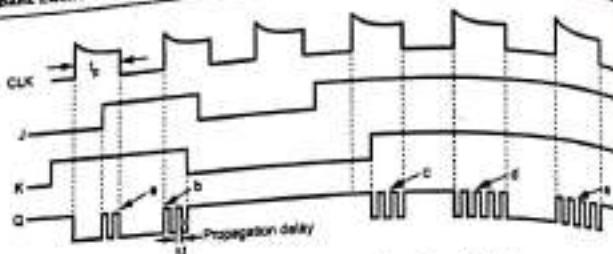


Fig. Q.59.1 Input and output waveforms for clocked JK flip-flop

- This condition exists when  $t_p \geq \Delta t$ . Thus by keeping  $t_p < \Delta t$  we can avoid race around condition.
- We can keep  $t_p < \Delta t$  by keeping the duration of edge less than  $\Delta t$ .
- A more practical method for overcoming this difficulty is the use of the Master-Slave (MS) configuration.

### 3.14 : T Flip-Flop

Q.60 Draw and explain the operation of T flip-flop.

Ans. : \* T flip-flop is also known as 'Toggle flip-flop'.

- As shown in the Fig. Q.60.1, the T flip-flop is obtained from a JK flip-flop by connecting both inputs, J and K together.

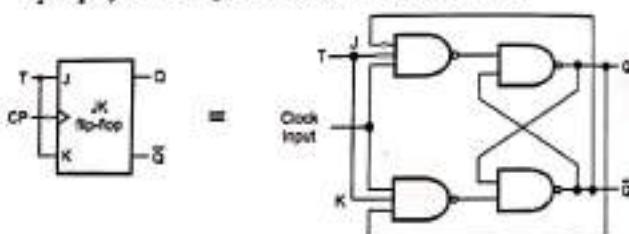


Fig. Q.60.1 T flip-flop using NAND gates

- When  $T = 0$ ,  $J = K = 0$  and hence there is no change in the output. When  $T = 1$ ,  $J = K = 1$  and hence output toggles.
- The Fig. Q.60.2 shows logic symbol and truth table for T flip-flop.

(a) Logic symbol	(b) Truth table																					
	<table border="1" style="margin-left: auto; margin-right: auto;"> <thead> <tr> <th><math>Q_n</math></th> <th>T</th> <th><math>Q_{n+1}</math></th> </tr> </thead> <tbody> <tr> <td>0</td> <td>0</td> <td>0</td> </tr> <tr> <td>0</td> <td>1</td> <td>1</td> </tr> <tr> <td>1</td> <td>0</td> <td>1</td> </tr> <tr> <td>1</td> <td>1</td> <td>0</td> </tr> </tbody> </table> $\equiv$ <table border="1" style="margin-left: auto; margin-right: auto;"> <thead> <tr> <th>T</th> <th><math>Q_{n+1}</math></th> </tr> </thead> <tbody> <tr> <td>0</td> <td><math>Q_n</math></td> </tr> <tr> <td>1</td> <td><math>\bar{Q}_n</math></td> </tr> </tbody> </table>	$Q_n$	T	$Q_{n+1}$	0	0	0	0	1	1	1	0	1	1	1	0	T	$Q_{n+1}$	0	$Q_n$	1	$\bar{Q}_n$
$Q_n$	T	$Q_{n+1}$																				
0	0	0																				
0	1	1																				
1	0	1																				
1	1	0																				
T	$Q_{n+1}$																					
0	$Q_n$																					
1	$\bar{Q}_n$																					

Fig. Q.60.2

### 3.15 : Applications of Flip-Flops

Q.61 State various applications of flip-flops.

CBT [SPPU : SPPU : Dec-09, Marks 2]

Ans. : Some of the important applications of flip-flops are :

- It can be used as a memory element.
- It can be used to eliminate key debounce.
- It is used as a basic building block in sequential circuits such as counters and registers.
- It can be used as a delay element.

### 3.16 : Block Diagram of Microprocessor

Q.62 Draw and explain the block diagram of microprocessor.

CBT [SPPU : May-09, 17, 18, Marks 6]

Ans. : \* A microprocessor is a sequential digital circuit which provides the flexibility to perform different tasks upon execution of corresponding instruction sequence.

- Each microprocessor has a fixed set of instructions which are coded in binary.

- Microprocessor has a circuitry to read instructions from memory and execute the instructions to perform particular task.
- The Fig. Q.62.1 shows the block diagram of a microprocessor.

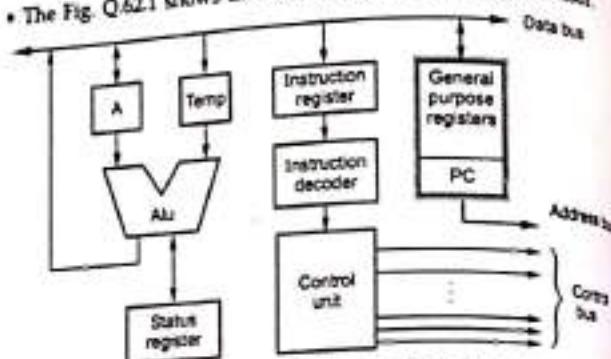


Fig. Q.62.1 Simplified block diagram of a microprocessor

- The block diagram shown in Fig. 9.7.1 includes three major devices.
  1. ALU
  2. Several registers : Accumulator, Status register, Instruction register, Program counter and general purpose registers.
  3. Control unit
- Program Counter : The program counter gives the address of memory location from where the next instruction is to be fetched.
- Instruction Register : Instruction read from memory is loaded into the instruction register. It is then sent to the instruction decoder. The instruction decoder decodes the instruction and gives decoded signals as an input to the control unit.
- Arithmetic Logic Unit (ALU) : The ALU of the microprocessor performs arithmetic and logic operations such as add, subtract, AND, OR, exclusive-OR, complement, shift right, shift left and so on.

- A Register (Accumulator) : In most of the microprocessors register A gives data for the ALU and after performing the operation, the resulting data word is sent to the register A and stored there. This special register, where the result is accumulated is commonly known as accumulator.
- Status Register : The status register is used to store the results of certain condition such as result is zero, negative etc., when certain operations are performed during execution of the program. The status register is also referred to as flag register.
- Control Unit : The control unit is responsible for working of all other parts of the microprocessor together. It maintains the synchronization in operation of different parts in the microprocessor. The control unit receives the signal from instruction decoder and generates the control signals necessary to carry out the instruction execution.
- Bus : A microprocessor communicates with memory and I/O devices with a common communication path called bus. There are three types of buses : address bus, data bus and control bus.

### 3.17 : Block Diagram of Microcontroller

- Q.63 Draw and explain the block diagram of a microcontroller.  
CB [SPPU : Dec-11,17, May-12,18, Marks 6]

Ans. : \* To make a complete microcomputer system, only microprocessor is not sufficient. It is necessary to add other peripherals such as Read Only Memory (ROM), read/write memory (RAM), input/output ports, programmable timers, serial ports and so on.

- The Fig. Q.63.1 shows the block diagram of a microcontroller. The microcontroller incorporates all the features that are found in microprocessor. However, it has also added features to make a complete microcomputer system on its own. The microcontroller has built-in ROM, RAM, parallel I/O, serial I/O and Timers/counters.

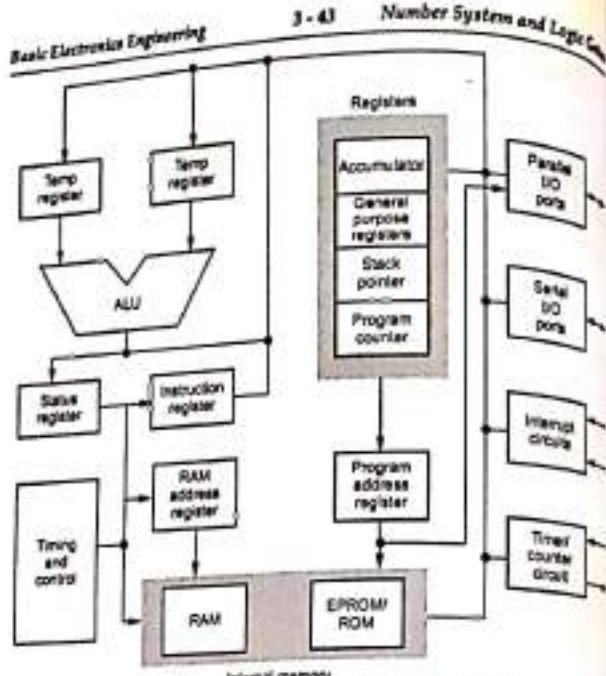


Fig. Q.63.1 Block diagram of microcontroller

**3.18 : Comparison Between Microprocessor and Microcontroller**

**Q.64 Give the comparison between microprocessor and microcontroller.**  
ESE [SPPU : Dec-10, 12, 14, 17, Muh]

**Ans. :**

Sr. No.	Microprocessor	Microcontroller
1.	Microprocessor contains ALU, control unit (clock and timing circuit), different register and interrupt circuit.	Microcontroller contains microprocessor, memory (ROM and RAM), I/O interfacing circuit and peripheral devices such as A/D converter, serial I/O, timer etc.

**Disconet**  
A Guide for Engineering Students

**EElectronics**  
A Guide for Engineering Students

Basic Electronics Engineering      3 - 44      Number System and Logic Gates

2.	It has many instructions to move data between memory and CPU.	It has one or two instructions to move data between memory and CPU.
3.	It has one or two bit handling instructions.	It has many bit handling instructions.
4.	Access times for memory and I/O devices are more.	Less access times for built-in memory and I/O devices.
5.	Microprocessor based system requires more hardware.	Microcontroller based system requires less hardware reducing PCB size and increasing the reliability.
6.	Microprocessor based system is more flexible in design point of view.	Less flexible in design point of view.
7.	It has single memory map for data and code.	It has separate memory map for data and code.
8.	Less number of pins are multi-functioned.	More number pins are multi-functioned.

**3.19 : Advantages using Microprocessor and Microcontroller**

**Q.65 State the advantages of microprocessor and microcontroller.**  
ESE [SPPU : Dec-09, Marks 4]

**OR Explain the importance of microprocessor.**

ESE [SPPU : Dec-10, Marks 4]

- Ans. :** 1. They are general purpose electronic processing devices which can be programmed to execute a number of tasks.  
 2. They have an ability to handle and manipulate numerical data.  
 3. They can store and access necessary data from memory whenever required.  
 4. They are compact. Thus use of microprocessor/microcontroller technology results in reduced parts count and smaller circuit boards.

5. Microprocessor/Microcontroller based systems are more versatile, programs may easily be changed to accept system changes.
6. Due to reduction in circuit connections they are more reliable.
7. Because of their large capabilities and integration they simplify system design.
8. Use of microprocessor/microcontroller reduces development time, cost and size of the system.
9. Due to less components such systems are easily maintainable.
10. Due to involvement of programming we can bring intelligence in these systems.
11. They use integrated technology and hence gives better performance and reliability, and decrease response times.

We know that microcontroller has built-in peripherals. They provide following additional benefits.

- Built-in peripherals have smaller access times hence speeds more.
- Hardware reduces due to single chip microcomputer system.
- Less hardware reduces PCB size and increases reliability of the system.

### 3.20 : Applications of Microprocessor and Microcontroller

#### Q.64 Give the applications of microprocessor and microcontroller.

**Ans. :** • The microprocessors are mainly used as general purpose processors. They are used in personal computers, laptops, servers and so on. Microcontrollers are more preferred in embedded products. Some applications of Microprocessors and Microcontrollers are listed below :

- Calculators
- Accounting systems
- Game machines
- Data acquisition systems
- Communication systems
- Complex industrial controllers
- Traffic light control systems
- Military applications.

END... ↗

## UNIT - IV

# 4

## Electronic Instruments

### 4.1 : Digital Multimeter

**Q.1** With the help of block diagram explain how digital multimeter is used to measure the various quantities.

**Ans. :** • The Fig. Q.1.1 shows the block diagram of digital multimeter.

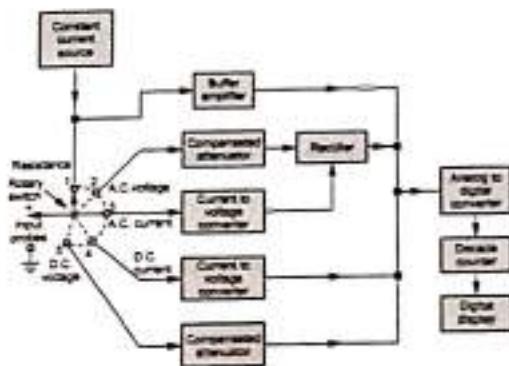
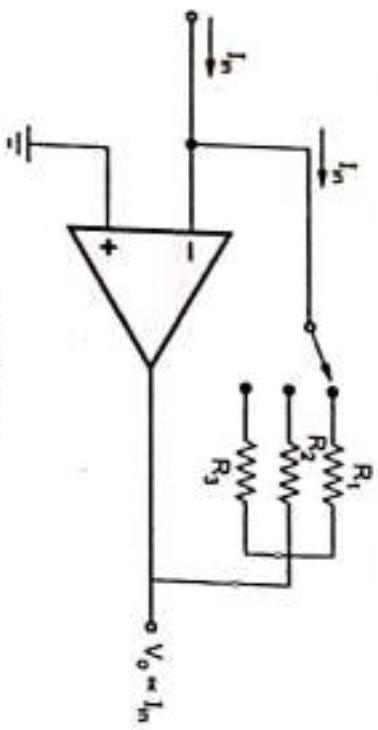


Fig. Q.1.1 Block diagram of digital multimeter

- The various measurements possible by DMM are resistance, a.c. voltage and current, d.c. voltage and current.
- The selection of the parameter is possible with the help of rotary switch connected to input probes of DMM.

- 1. Resistance measurement :** The rotary switch is in position '1' and resistance is connected to input probes. The constant current source drives a current through unknown resistance. This produces voltage across resistance which is directly proportional to the resistance. It is given to the buffer amplifier and then to analog to digital converter. The ADC converts it to equivalent digital signal and it is displayed with the help of digital display.
- 2. A.C. Voltage measurement :** The rotary switch is in position '2' and input a.c. voltage is applied to probes. If it is above the selected range, it is attenuated with the help of compensated attenuator. It is rectified to produce proportional d.c. voltage. Then it is given to ADC which displays it in volts.

- 3. A.C. Current measurement :** The rotary switch is in position '3' and unknown current is applied across input probes. It is converted to proportional voltage using current to voltage converter.
- This I-V converter is op-amp circuit as shown in the Fig. Q.1.2. The op-amp input current is zero hence  $I_{in}$  flows through  $R_1$  and drop across  $R_1$  is  $V_o \propto I_{in}$ .

**Fig. Q.1.2**

The resistances  $R_1$ ,  $R_2$  and  $R_3$  are used for the proper range selection. This voltage is rectified and then given to ADC which displays the current in amperes.

- 4. D.C. Current measurement :** The rotary switch is in position '4' and unknown d.c. current is applied across input probes. This is converted to proportional voltage with the help of current to voltage converter. This voltage is given to ADC without rectification. As this is proportional to d.c. current, ADC displays it in amperes on digital display.
- 5. D.C. Voltage measurement :** The rotary switch is in position '5' and unknown voltage is applied across input probes. It is attenuated and directly given to ADC without rectification. The ADC displays it in volts.

#### Q.2 Write the important specifications of digital multimeter.

■ [Marks 6]

**Ans. :** • The important specifications of a digital multimeter are as follows:

- D.C. voltage : This includes various d.c. voltage ranges available alongwith the resolution and accuracy.
- A.C. voltage : This includes various a.c. voltage ranges available alongwith the resolution and accuracy.
- D.C. current : This includes various d.c. current ranges available alongwith the resolution and accuracy.
- A.C. current : This includes various a.c. current ranges available alongwith the resolution and accuracy.
- Resistance : This includes the available resistance range. Typically six ranges are available from  $200\ \Omega$  to  $20\ M\Omega$ . The accuracy is  $\pm 0.1\%$  of reading + two digits +  $0.02\ \Omega$  on the lowest range.
- Input impedance : The input impedance is about  $10\ M\Omega$  on all the ranges.
- Normal mode noise rejection : This indicates the ability of the meter to reject the noise and unwanted signals. It is greater than  $60\ dB$  at  $50\ Hz$  while the common mode noise rejection is greater than  $90\ dB$  at  $50\ Hz$  and greater than  $120\ dB$  at d.c.

- viii) **Overload protection** : The overload protection of 1000 V d.c. and 750 r.m.s. a.c. is provided.

- ix) **Diode test** : The voltage drop across the diode can be measured for which  $1 \text{ mA} \pm 10\%$  of constant current source is used.

- x) **Conductance** : It can display conductance in siemens.

- xi) **Relative reference** : When 'REL' button is pressed, the displayed reading is stored as a reference and then subtracted from the subsequent readings to indicate only amount of deviation from the reference.

- xii) **Frequency** : The frequency range is 200 Hz to 200 kHz autoselection.

## 4.2 : Function Generator

- Q.3 Draw the block diagram of function generator and explain the function of each block.** [SPPU : Dec.-17, Marks 6]

**Ans. :** • The function generator is an instrument which generates different types of waveforms.

- The block diagram of a typical function generator is as shown in Fig. Q.3.1.

- In the function generator, the frequency is controlled by varying the magnitude of current which drives the integrator.
- The frequency controlled voltage is used to regulate two current sources namely **upper current source** and **lower current source**.
- The upper current source supplies constant current to an integrator. The output voltage of integrator then increases linearly with time.
- If the current charging the capacitor increases or decreases, the slope of output voltage increases or decreases respectively. Hence this controls frequency.
- The **voltage comparator multivibrator** circuit changes the state of the network when the output voltage of integrator equals the maximum predetermined upper level.

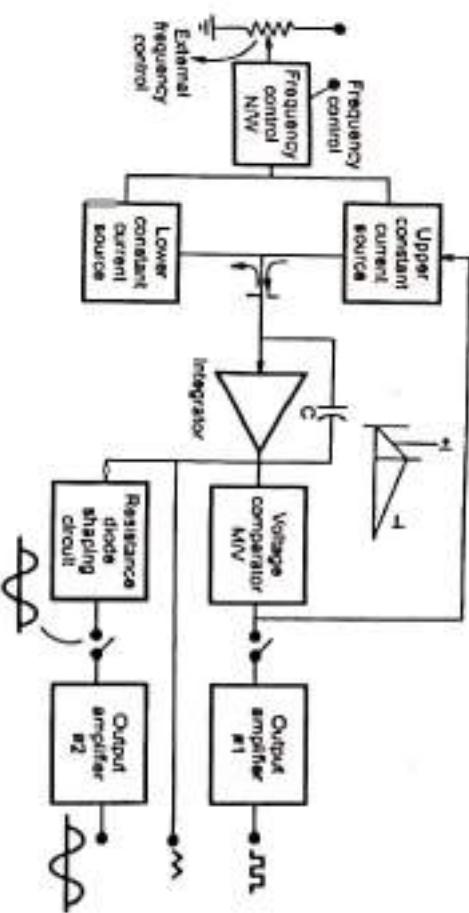


Fig. Q.3.1 Typical function generator

- Because of this change in state, the upper current source is removed and the lower current source is switched ON.
- This lower current source supplies opposite current to the integrator circuit. The output of integrator decreases linearly with time. When this output voltage equals maximum predetermined upper level on negative side, the voltage comparator multivibrator again changes the condition of the network by switching OFF the lower current source and switching ON the upper current source.
- The output voltage of the integrator has triangular waveform.
- To get square wave, the output of the integrator is passed through comparator.
- The voltage comparator delivers square wave output voltage of same frequency as that of input triangular waveform.
- The sine wave is derived from triangular wave. The triangular wave is synthesised into sine wave using diode resistance network. In this shaper circuit, the slope of triangular wave is changed as its amplitude changes. This results in a sine wave with less than 1 % distortion.

individually selected outputs of any of the waveform functions.

**Q.4 State the applications of function generator.** [SPPU : Marks 3]

- 1) It is used to generate different types of waveforms simultaneously such as sine wave, square wave, triangular wave and saw-tooth wave at a desired frequency from few hertz to several kilohertz.
- 2) It is used to test bandwidth of audio frequency amplifier using square wave testing method.
- 3) It can be used in troubleshooting of various analog as well as digital instruments.
- 4) It is most extensively used as signal source for radio receiver alignment procedures.

### 4.3 : Digital Storage Oscilloscope (DSO)

**Q.5 Draw the block diagram of digital storage oscilloscope and explain function of each block.** [SPPU : Marks 8]

**Ans. :** • The block diagram of digital storage oscilloscope is shown in the Fig. Q.5.1.

- As done in all the oscilloscopes, the input signal is applied to the amplifier and attenuator section. The oscilloscope uses same type of amplifier and attenuator circuitry as used in the conventional oscilloscopes.
- The attenuated signal is then applied to the vertical amplifier.
- The vertical input, after passing through the vertical amplifier, is digitised by an analog to digital converter (A/D converter) to create a data set that is stored in the memory.
- The data set is processed by the microprocessor and then sent to the display.

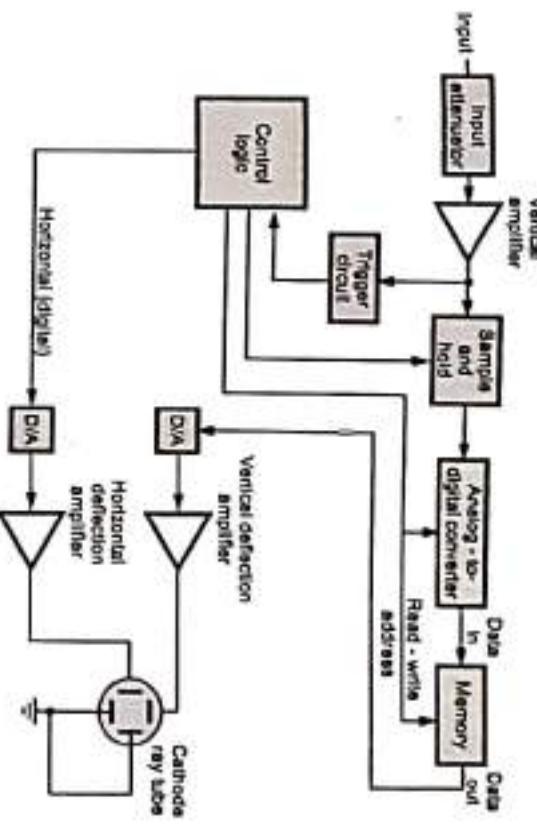


Fig. Q.5.1 Block diagram of digital storage oscilloscope

- The main requirement of A/D converter in the digital storage oscilloscope is its speed.
- The digitising the analog input signal means taking samples at periodic intervals of the input signal.
- The rate of sampling should be at least twice as fast as the highest frequency present in the input signal, according to sampling theorem.
- This ensures no loss of information. The sampling rates as high as 100,000 samples per second is used. This requires very fast conversion rate of A/D converter.

**Key Point :** Hence, generally flash analog to digital converters are used, whose resolution decreases as the sampling rate increases.

- The total digital memory storage capacity is 4096 for a single channel, 2048 for two channels each and 1024 for four channels each.

- The sampling rate and memory size are selected depending upon the duration and the waveform to be recorded.

- Once the input signal is sampled, the A/D converter digitises it. The signal is then captured in the memory.

- Once it is stored in the memory, many manipulations are possible as memory can be read out without being erased.

**Q.6 State the various applications of DSO.** [SPRU : Dec-17, Marks 4]

- Ans. : The various applications of digital storage oscilloscope are,
- Measurement of various a.c. and d.c. parameters such as currents, voltages etc.
  - Measurement of various parameters of alternating signal such as r.m.s., average, crest factor, duty cycle etc.
  - Measurement of frequency, time period, phase, phase difference for periodic and nonperiodic waveforms.
  - The transient parameters of fast changing waveforms such as overshoot, rise time, fall time etc. can be measured.
  - Mathematical operations such as addition, subtraction, integration etc. of various waveforms can be obtained.
  - Used to measure slow moving parameters such as temperature of the day.
  - The operations such as fast Fourier transform, discrete Fourier transform, inverse Fourier transform etc. can be performed.
  - The parameters like inductance, capacitance, impedance etc. also can be measured.
  - For component testing and troubleshooting as the transients can be captured and stored.
  - For transmission line analysis to obtain standing waves, modulation characteristics etc.
  - The visual representation of a target for aeroplane, ship etc. can be obtained.

- The characteristics of various components such as V-I characteristics of diodes, transistors etc. can be obtained.
- To obtain the P-V diagrams, B-H curves, Hysteresis loops etc.

**Q.7 State the advantages of DSO.** [SPRU : Dec-17, Marks 6]

- Ans. i) It is easier to operate and has more capability.

- ii) The storage time is infinite.

- iii) The display flexibility is available. The number of traces that can be stored and recalled depends on the size of the memory.

- iv) The cursor measurement is possible.

- v) The characters can be displayed on screen along with the waveform which can indicate waveform information such as minimum, maximum, frequency, amplitude etc.

- vi) The X-Y plots, B-H curve, P-V diagrams can be displayed.

- vii) The pretrigger viewing feature allows to display the waveform before trigger pulse.

- viii) Keeping the records is possible by transmitting the data to computer system where the further processing is possible.

- ix) Signal processing is possible which includes translating the raw data into finished information e.g. computing parameters of a captured signal like r.m.s. value, energy stored etc.

#### 4.4 : Powerscope

**Q.8 Draw the block diagram of powerscope and explain.** [SPRU : Marks 8]

Ans. : The block diagram of powerscope is shown in the Fig. Q.8.1.

- The input signal is attenuated by a factor of 20 by the input attenuators. Further reduction in sensitivity is provided by the differential compensated attenuators.
- The input stage consists of matched pair of FETs operating as source followers, driving a pair of emitter followers giving a current gain required to drive a main amplifier.

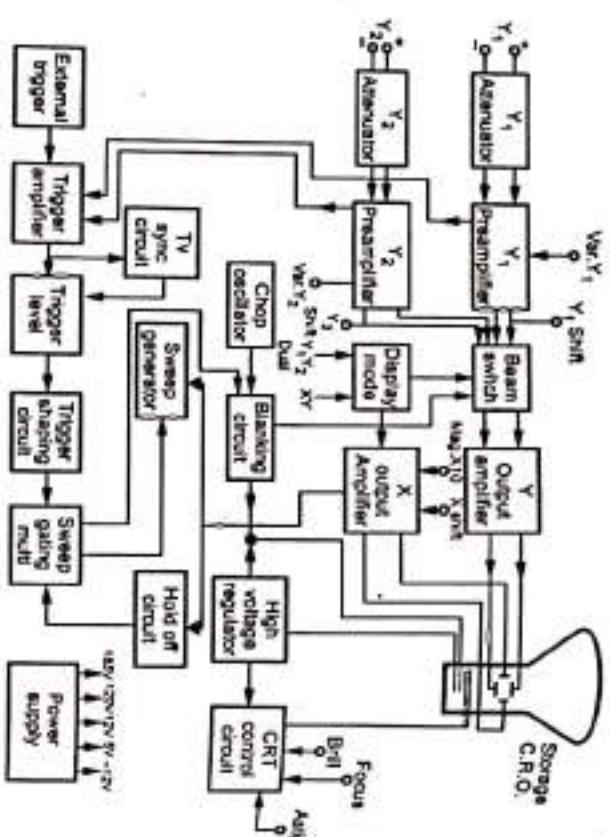


Fig. Q.8.1 Block diagram of power scope

- The vertical deflection system provides calibrated deflection factors from about 50 mV/div to 200 V/div, for both the channels.
- The trace is switched between the two channels at a rate of 100 kHz in CHOP mode and alternating between sweeps in ALT mode. In CHOP mode, additional blanking is provided to eliminate the switching transients. ALT or CHOP mode gets automatically selected by time/div control.
- Triggering circuit provide stable sweep triggering which extends beyond the bandwidth of the vertical deflection system.
- The horizontal deflection system has calibrated sweep rates from 0.5 s/div to 0.2  $\mu$ s/div. X10 magnifier extends fastest rate to 20 ns/div.
- Variable sweep control provides continuous reduction of sweep rate. Triggering is automatic or level, selected from internal/external or line sources.

- T.V. signals can be filtered using T.V. synchronous circuit. The signals are used to lock LINE or FRAME pulses easily and hence it is very useful in T.V. troubleshooting applications.
- XY mode and Z-modulation are added features. The calibrator output provides calibration check and probe compensation facility.
- The output signals from  $Y_1$  and  $Y_2$  are connected to storage C.R.O. To eliminate the effects of variations in line voltage, the regulated d.c. power supplies is used.

#### 4.5 : AC/DC Power Supply

##### Q.9 Draw the block diagram of a.c. to d.c. power supply.

[Marks 5]

Ans. :- A typical d.c. regulated power supply consists of various stages. The Fig. Q.9.1 shows the block diagram of a typical d.c. regulated power supply, consisting of various circuits including the nature of voltages at various points.

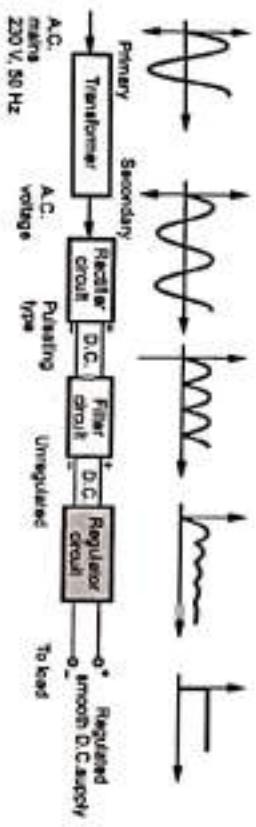


Fig. Q.9.1 A typical regulated power supply

- The a.c. voltage (230 V, 50 Hz) is connected to the primary of the transformer. The transformer steps down the a.c. voltage, to the level required for the desired d.c. output. Thus, with suitable turns ratio we get desired a.c. secondary voltage.
- The rectifier circuit converts this a.c. voltage into a pulsating d.c. voltage.

- The filter circuit is used after a rectifier circuit, which reduces the ripple content in the pulsating d.c. and tries to make it smoother. Still then the filter output contains some ripple. This voltage is called unregulated d.c. voltage.

- A circuit used after the filter is a regulator circuit which not only makes the d.c. voltage smooth and almost ripple free but it also keeps the d.c. output voltage constant though input d.c. voltage varies under certain conditions. It keeps the output voltage constant under variable load conditions, as well.
- The output of a regulator is called d.c. supply, to which the load can be connected.

#### 4.6 : Autotransformer

**Q.10 What is autotransformer ? Explain its working.** [Marks 5]

**Ans. :** • An autotransformer is a special type of transformer such that a part of the winding is common to both primary as well as secondary.

- It has only winding wound on a laminated magnetic core. With the help of autotransformer the voltage can be stepped down or can be stepped up also, to any desired value.

Fig. Q.10.1 (a) shows the step down autotransformer. AB acts as a primary winding while part of the primary winding BC acts as a

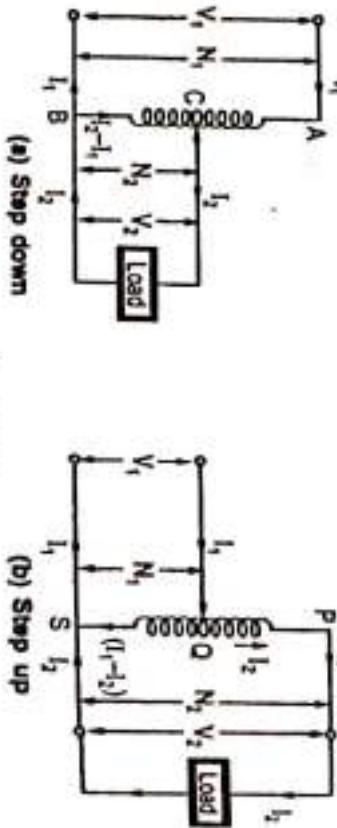


Fig. Q.10.1

\* Neglecting the losses, the leakage reactance and the magnetising current we can write the transformation ratio of the autotransformer as

$$K = \frac{V_2}{V_1} = \frac{I_1}{I_2} = \frac{N_2}{N_1}$$

- Due to the use of single winding compared to normal two winding transformer, for the same capacity and voltage ratio, there is substantial saving in copper, in autotransformer.

**Q.11 Explain the applications of an autotransformer.** [Marks 5]

**Ans. : Applications of Autotransformer**

- 1) For interconnecting systems which are operating roughly at same voltage.
- 2) For starting rotating machines like induction motors, synchronous motors.
- 3) To give a small boost to a distribution cable to correct for the voltage drop.
- 4) As a furnace transformer for getting required supply voltage.
- 5) As a variac, to vary the voltage to the load, smoothly from zero to the rated value. Such variacs are commonly used for dimming the lights in cinema halls. Hence the variacs are also called dimmersstat. The principle of dimmersstat is shown in the Fig. Q.11.1.

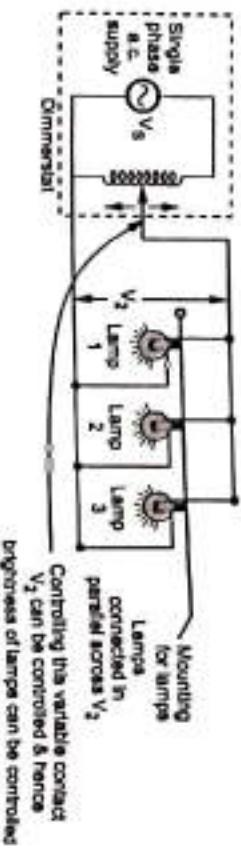


Fig. Q.11.1. Autotransformer as dimmerstat

**4.7 : Analog Ammeter and Voltmeter****Important Points to Remember**

- When a current carrying coil is placed in a magnetic field, it experiences a force. This is motoring action and is called D'Arsonval movement. This principle is used in analog ammeter and voltmeter.
- The basic D'Arsonval movement has two important specifications,

$I_m$  = Full scale deflection current of the movement

$R_m$  = Internal resistance of the coil used in the movement

**Q.12. Draw the basic analog ammeter circuit ? How shunt resistance is calculated ?** [Ans 8]

Ans. : • The coil used in the basic D'Arsonval movement is very small and light due to which it can carry very small currents. Hence it is necessary to modify the basic arrangement to get analog ammeter which can measure large currents.

- For the measurement of large currents, the major part of the current is bypassed using a resistance called shunt, in the basic movement.
- The shunt is connected in parallel with the basic meter as shown in the Fig. Q.12.1.

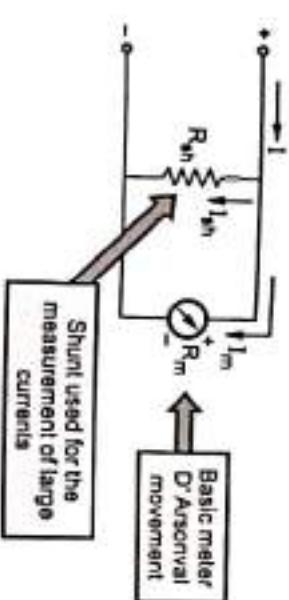


Fig. Q.12.1 Analog ammeter

**Calculation of Shunt Resistance :**

Let

$R_{sh}$  = Shunt resistance

$I_m$  = Full scale deflection current

$I_{sh}$  = Shunt current

$I$  = Total current =  $I_{sh} + I_m$   
drop across them is same.

$$I_{sh} R_{sh} = I_m R_m \quad \text{i.e.} \quad R_{sh} = \frac{I_m R_m}{I_{sh}}$$

$$I_{sh} = I - I_m \quad \text{i.e.} \quad R_{sh} = \frac{I_m R_m}{(I - I_m)}$$

**Q.13. Draw the basic analog voltmeter circuit ? How multiplier resistance is calculated ?** [Ans 8]

Ans. : • The basic d.c. voltmeter is nothing but a PMMC D'Arsonval galvanometer.

- The resistance is required to be connected in series with the basic meter to use it as a voltmeter. This series resistance is called a multiplier.
- The main function of the multiplier is to limit the current through the basic meter so that the meter current does not exceed the full scale deflection value.

- The voltmeter measures the voltage across the two points of a circuit or a voltage across a circuit component.

- The basic d.c. voltmeter is shown in the Fig. Q.13.1.

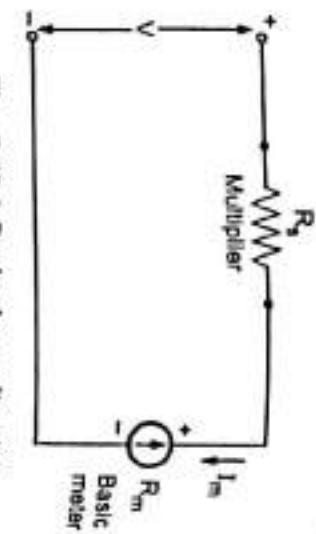


Fig. Q.13.1 Basic d.c. voltmeter

- The voltmeter must be connected across the two points or a component, to measure the potential difference, with the proper polarity.

#### Calculation of Multiplier Resistance :

Let  
 $R_m$  = Internal resistance of coil i.e. meter

$R_s$  = Series multiplier resistance

$I_m$  = Full scale deflection current

$V$  = Full range voltage to be measured

From Fig. Q.13.1,

$$V = I_m (R_m + R_s) = I_m R_m + I_m R_s$$

$$\therefore I_m R_s = V - I_m R_m$$

$$R_s = \frac{V}{I_m} - R_m$$

END... ↗

# 5

## Sensors

### 5.1 Introduction

- Q.1 Draw the block diagram of Instrumentation system and state the function of each block.**

☞ [SPU : May-04,05,07,17, Dec-05,07,08,13,17, Marks 6]

**Ans. :** • Fig Q.1.1 shows the block diagram of a instrumentation system. It indicates the necessary elements and their functions in a general measuring system.

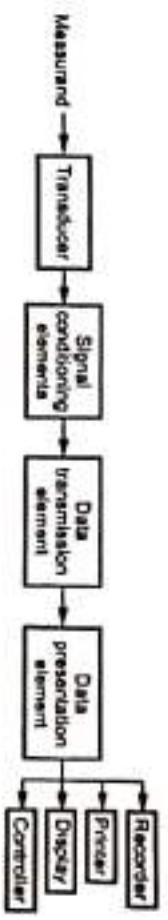


Fig. Q.1.1 Block diagram of an instrumentation system

**Measurand :** Most of the times input to the instrumentation system is the physical quantity such as temperature, pressure, displacement, force, etc. Such non-electrical input quantity is called measurand.

**Transducer :** A transducer converts the non-electrical input measurand into a proportional electrical signal such as voltage or current.

### 5.3 Classification of Sensors

**Q.3 Give the classification of sensors.**

**Ans. :** • It is very difficult to classify sensors under one criterion and hence different criteria may be adopted for the purpose. Some of these include :

#### **Classification based on Physical Quantity to be Sensed**

- The physical quantity that is being sensed is an important factor in this classification. Some of these are :

1. Flow
2. Level
3. Temperature
4. Pressure
5. Proximity and Displacement
6. Acceleration
7. Image
8. Gas
9. Light
10. Humidity
11. Moisture
12. Viscosity

#### **Classification based on Sensors' Conversion Phenomenon**

- The sensors' conversion phenomenon is also an important factor in classification of sensors. Some of the conversion phenomena are :

1. Magneto electric
2. Thermoelectric
3. Photoelectric
4. Piezoelectric
5. Variable resistance
6. Opto electronic
7. Variable reactance

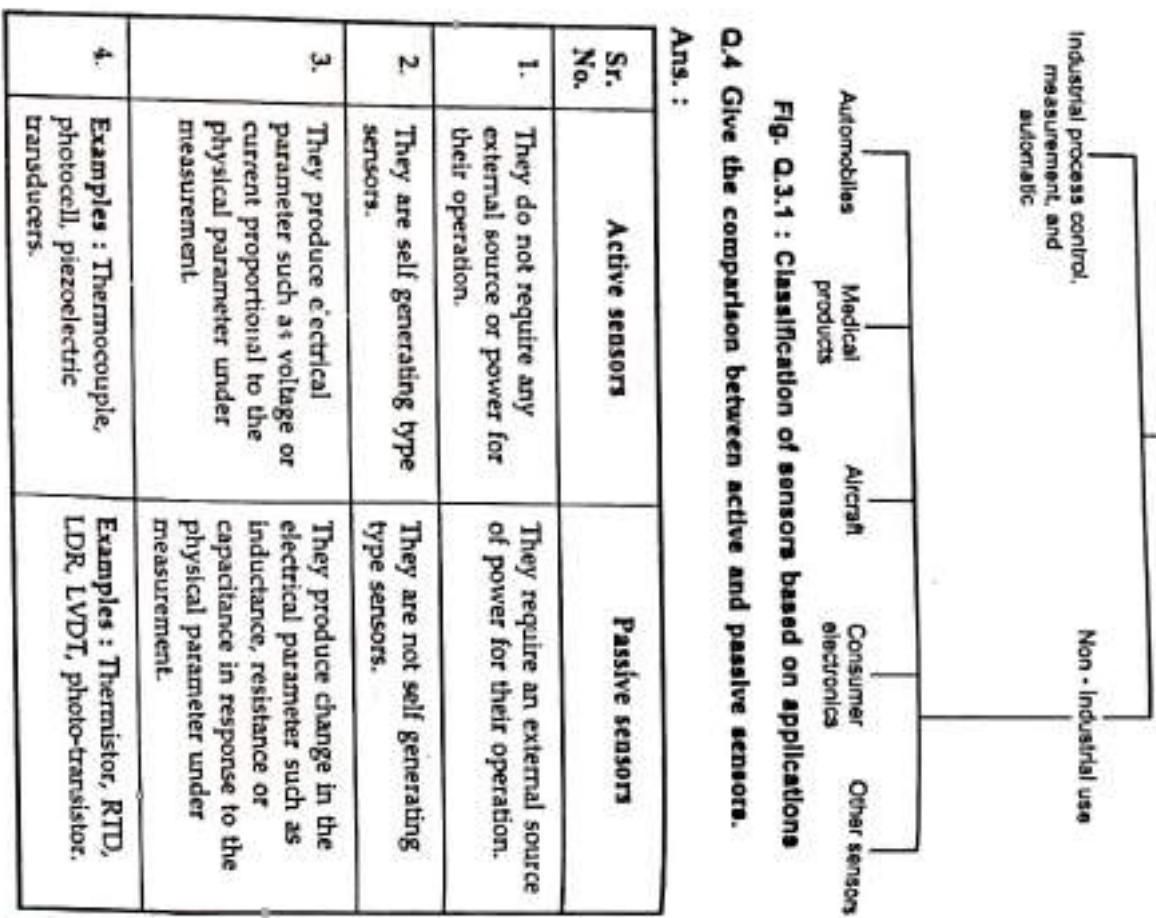
#### **Classification based on Power or Signal Requirement**

- All the sensors can be classified into two types based on the power or signal requirement. They are :

1. Active sensors
2. Passive sensors

#### **Classification based on Applications of Sensor**

- Application based classification of sensors is represented as



- Q.4 Give the comparison between active and passive sensors.**

Ans. :

Sr. No.	Active sensors	Passive sensors
1.	They do not require any external source or power for their operation.	They require an external source of power for their operation.
2.	They are self generating type sensors.	They are not self generating type sensors.
3.	They produce electrical parameter such as voltage or current proportional to the physical parameter under measurement.	They produce change in the electrical parameter such as inductance, resistance or capacitance in response to the physical parameter under measurement.
4.	Examples : Thermocouple, photocell, piezoelectric transducers.	Examples : Thermistor, RTD, LDR, LVDT, photo-transistor.

#### 5.4 Selecting a Sensor

- Q.5 Write short note on selection criteria for sensors.**

**OR Mention the factors to be considered while selecting a sensor for an application.** [SPU : Dec.-06, 10, 14, May-13, 14, Marks 4]

- Ans. : Factors to be considered while selecting a sensors are :
1. **Nature of measurement** : The selection of sensor will naturally depend upon the nature of quantity to be measured.
  2. **Sensing range** : Sensors should be selected according to their sensing range.
  3. **Response speed** : As per the requirements of application sensor must be selected according to response speed.
  4. **Required resolution and sensitivity** : As per the requirement of application, sensor should be selected according to required resolution and accuracy.
  5. **Repetition accuracy** : Repetition accuracy of the sensor should be considered while selecting the sensor.
  6. **Loading effect** : The sensor is selected to have minimum loading effect to keep the errors to minimum. This means that the sensor should not affect or change the value of the parameter under measurement.
  7. **Environmental considerations** : A sensor output may be affected due to adverse environmental conditions such as temperature changes, shock and vibration and electromagnetic interference. Thus sensor, should be selected such that it should work reliably in the given working environment.
  8. **Mechanical considerations** : While selecting the sensor, it is necessary to consider the following mechanical aspects of sensor.
    - Simplicity of mounting and cable installation.
    - Convenient size, shape and weight.
    - Accessibility of the sensor for later repairs.
  9. **Output type** : Depending on the application the sensor should be selected to suit its output type : Discrete or Analog.

**10. Cost and availability :** General factors involved in selection are cost and availability.

**11. Time span :** The time span indicates the time period for which a sensor works reliably. According to application the sensor should be selected so that it will work properly for the desired time span.

**12. Simplicity, reliability and low maintenance :** A sensor should be selected according to its simplicity, reliability and maintenance cost.

### 5.5 Analog and Digital Sensors

**Q.6 Write a note on analog sensors.**

**Ans. :** • An analog sensor produces continuously varying output signals over a range of values. Usually the output signal is voltage and this output signal is proportional to the measurand.

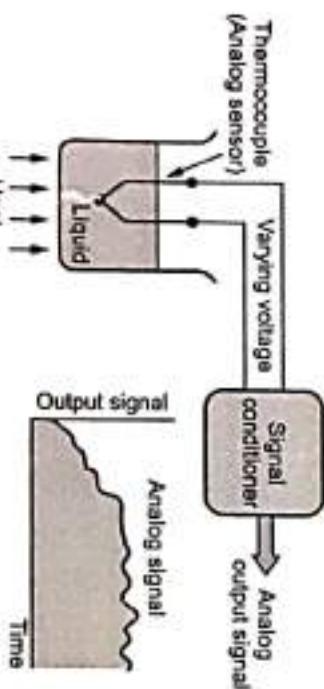


Fig. Q.6.1 Example of analog sensor

- The quantity that is being measured like speed, temperature, pressure, strain, etc. are all continuous in nature and hence they are analog quantities.

- Fig. Q.6.1 shows the example of analog sensor. Here, The thermocouple continuously responds to temperature changes as the liquid is heated up or cooled down.

- The output of an analog sensor tends to change smoothly and continuously over time. Hence the response time and accuracy of circuits employing analog sensors is slow and less.

**Q.7 Explain the operation of digital sensor with the help of example.**

**Ans. :** • A digital sensor produces discrete digital signals. The output of a digital sensor has only two states, namely 'ON' and 'OFF'. ON is logic 1 and OFF is logic 0.

- A push button switch is the best example of a digital sensor. In this case, the switch has only two possible states : Either it is ON when pushed or it is OFF when released or not pushed.
- The following setup uses a light sensor to measure the speed and produces a digital signal.
- In the below setup, the rotating disc is connected to the shaft of a motor and has number of transparent slots. The light sensor captures the presence or absence of the light and sends logic 1 or logic 0 signal accordingly to the counter. The counter displays the count proportion to the speed of the disc.



Fig. Q.7.1 Example of digital sensor

- In general, the accuracy of a digital sensor is high when compared to an analog sensor. The accuracy depends on the number of bits that are used to represent the measurand. Higher the number of bits, the greater is the accuracy.

**Q.8** Give comparison between analog and digital sensor.

**Ans. :** Table Q.8.1 summarize difference between analog sensor and digital sensor.

Specifications	Analog sensor	Digital sensor
Output	Infinite number of values (i.e. continuous)	Finite number of values (i.e. Discrete steps or digital)
Accuracy in reading the output	Low	High
Response time	Low	High
Applications	It is ideal for reading continuous varying parameters such as temperature, humidity etc.	It is ideal for reading discrete values (i.e. binary values 1 (ON) and 0 (OFF)) such as push button switch, line follower robot (reads black or white colors), optical encoder, etc.
Examples	Thermocouple or temperature sensor, Gyroscope	Digital Light Sensor, push button, distance sensor, line follower sensor

Table Q.8.1

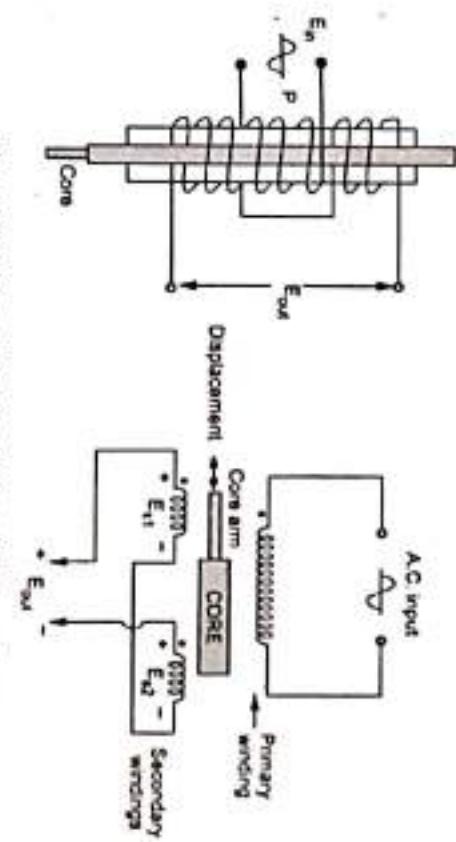


Fig. Q.10.1 Linear variable differential transformer

**Q.9 What is LVDT?**

**Ans. :** • LVDT (Linear Variable Differential Transducer) is a variable inductance displacement transducer in which the inductance is varied according to the displacement.

**O.10 Explain the construction and principle of operation of LVDT.**

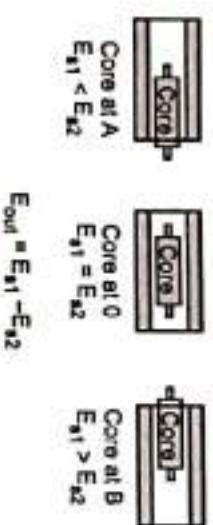
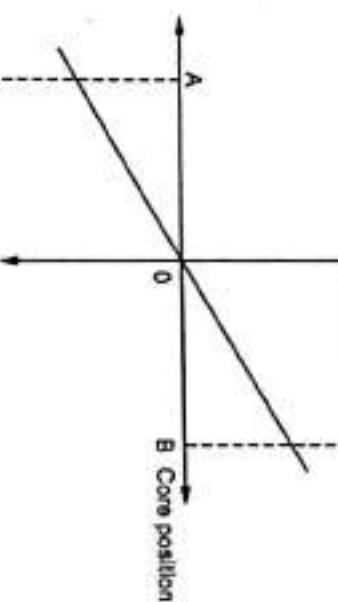
**OR**, Draw and explain Linear Variable Differential Transducer (LVDT) along with its transfer characteristics.  
[SPMU : May-19, Marks 7]

**Ans. : Construction :**

- In LVDT the inductance is varied by varying the mutual inductance between the two coils of linear variable differential transformer.
- The linear variable differential transformer consists of a single primary winding  $P_1$  and two secondary windings  $S_1$  and  $S_2$  wound on a hollow cylindrical former. Refer Fig. Q10.1. The secondaries have an equal number of turns but they are connected in series opposition so that the e.m.f.s induced in the coils oppose each other and the output voltage is given by  $E_{out} = E_{s1} - E_{s2}$

- The core made up of nickel-iron alloy is slotted longitudinally to reduce eddy current losses.
- The displacement to be measured is applied to an arm attached to the core.

Output voltage



**Fig. Q.10.2 Output voltage of LVDT at different core position**

#### Operation

- When a.c. source is applied to primary and with the core in the centre, or reference position, the induced e.m.f.s in the secondaries are equal ( $E_{s1} = E_{s2}$ ), and since they oppose each other, the output voltage will be zero volt.
- When the core is forced to move to the right (Position A), more flux links the right-hand coil than the left-hand coil i.e.  $E_{s1} < E_{s2}$ . Therefore,  $E_{out}$  is negative.
- Similarly, when an externally applied force moves the core to the left-hand position (Position B), more magnetic flux links the

left-hand coil than the right-hand coil i.e.  $E_{s1} > E_{s2}$ . Therefore,  $E_{out}$  is positive.

- The amount of output voltage of an LVDT is a linear function of the core displacement within a limited range of motion.

#### Q.11 State the advantages of LVDT.

[SPRU : May-05,10,12,15, Dec-05,08,11,12, Marks 4]

##### Ans. : A) Mechanical

- Wide range of displacement :  $\pm 0.005$  to  $\pm 25$  inch.
- Frictionless operation : No physical contact exists between the core and coil structure.
- Ruggedness : Good mechanical life.
- Insensitive to temperature changes.
- Highly repeatable response (performance).

##### B) Electrical

- Linearity : Better (Output voltage is a linear function of mechanical displacement).
- High sensitivity.
- Resolution : Infinite.
- Electrical isolation is better.

#### Q.12 State the disadvantages of LVDT.

[SPRU : May-05,10,12,15, Dec-05,08,11,12, Marks 4]

Ans. : 1. Comparatively large displacements are necessary for appreciable differential output.

2. They are sensitive to stray magnetic fields. However, this interference can be reduced by shielding.

3. The dynamic response is limited by the mass of the core.

4. Temperature affects the transducer.

#### Q.13 State the applications of LVDT.

[SPRU : May-13, Marks 2]

**Ans. :** 1. The LVDT can be used in all applications where displacement ranging from fractions of a few mm to a few cm have to be measured.

- Acting as a secondary transducer, LVDT can be used as a device to measure force, weight and pressure etc. The force or pressure to be measured is first converted into a displacement using primary transducers. Then this displacement is applied to an LVDT, that acts as a secondary transducer, and converts the displacement into proportional output voltage. In these applications the high sensitivity of LVDT is a major attraction.

## 5.7 Motion Sensor - Accelerometer

### Q.14 What is an accelerometer?

**Ans. :** An accelerometer is an electromechanical device that will measure acceleration forces. These forces may be static, like the constant force of gravity pulling at your feet, or they could be dynamic - caused by moving or vibrating the accelerometer.

### Q.15 Explain working of piezoelectric accelerometer.

**Ans. :** • The piezoelectric accelerometer consists of a piezoelectric quartz crystal on which an accelerative force, whose value is to be measured, is applied.

- Due to the special self-generating

property, the crystal produces a voltage that is proportional to the accelerative force.

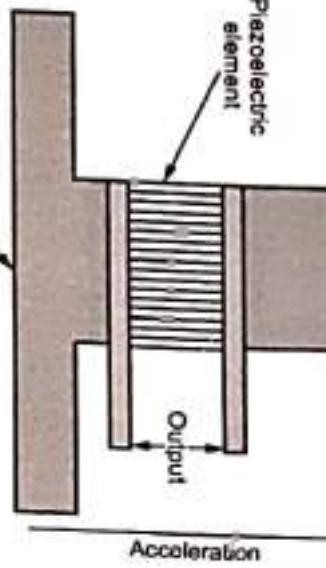


Fig. Q.15.1 Piezoelectric Accelerometer

- Fig. Q.15.1 shows the working and the basic arrangement for piezoelectric accelerometer.

### Q.16 Give important specifications of accelerometer.

**Ans. :** • Frequency response - This parameter can be found out by analyzing the properties of the quartz crystal used and also the resonance frequency of the device.

- Accelerometer grounding - Grounding can be in two modes. One is called the Case Grounded Accelerometer which has the low side of the signal connected to their core. This device is susceptible to ground noise. Ground Isolation Accelerometer refers to the electrical device kept away from the case. Such a device is prone to ground produced noise.

- Resonant frequency - It should be noted that the resonant frequency should be always higher.

- Temperature of operation - An accelerometer has a temperature range between - 50 degree Celsius to 120 degree Celsius.

- Sensitivity - The device must be designed in such a way that it has higher sensitivity.

- Axes - Most of the industrial applications requires only a 2-axis accelerometer. But if you want to go for 3D positioning a 3-axis accelerometer will be needed.

- Analog/Digital output - You must take special care in choosing the type of output for the device. Analog output will be in the form of small changing voltages and digital output will be in PWM mode.

### Q.17 State the applications of accelerometer.

**Ans. :** Some of the common applications of accelerometer are :

- Machine monitoring.
- Used to measure earthquake activity and aftershocks.
- Used in measuring the depth of CPR chest compression.

4. Used in Internal Navigation System (INS). That is, measuring the position, orientation, and velocity of an object in motion without the use of any external reference.
5. Used in airbag shooting in cars and vehicle stability control.
6. Used in video games like PlayStation 3, so as to make the steering more controlled, natural and real.
7. Used in camcorder to make images stable.

### 5.8 Temperature Sensors - Thermocouples, Thermistor and RTD

#### Q.18 What is thermocouple?

Ans. : • Thermoelectric transducer is a temperature transducer which converts thermal energy into an electrical energy. The most commonly used thermoelectric transducer is thermocouple. Thermocouple is generally used as a primary transducer for temperature measurement in which changes in temperature are directly converted into an electrical signal. It is an active temperative sensor which does not require external power supply.

#### Q.19 What is Seebeck effect?

Ans. : • In 1821, the great scientist Prof. Seebeck discovered that if the two wires of different metals are joined together forming closed circuit and if the two junctions formed are at different temperatures, an electric current flows around a closed circuit. This is called Seebeck effect. He also observed that if the two metals used are copper and iron, then the current flows from copper to iron at hot junction and from iron to copper at cold junction as shown in the Fig. Q.19.1 (a).

• If the copper wire is cut, the e.m.f appears across the open circuit as shown in the Fig. Q.19.1 (b). This e.m.f. is commonly known as Seebeck e.m.f. This Seebeck e.m.f. is proportional to the difference in the temperatures of the two junctions.

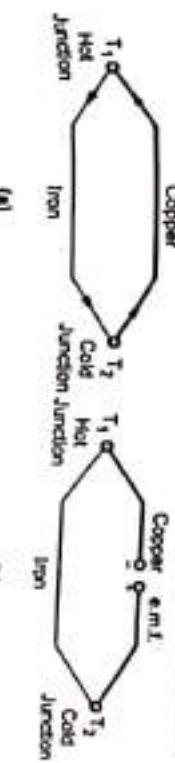


Fig. Q.19.1 Seebeck effect

Q.20 Explain the principle of operation and construction of thermocouple. [ISMU : May-04,05,06,08; Dec-07,18, March-01]

Ans. : • As said earlier the operation of thermocouple is based on the phenomenon called seebeck effect.

• A thermocouple consists of a pair of dissimilar metal wires joined together at one end, forming a hot junction and terminated at the other end known as reference or cold junction.

• When heat is applied to the hot junction, a temperature difference exists between the hot junction and the cold junction, causing generation of e.m.f. This is illustrated in Fig. Q.20.1 (a).

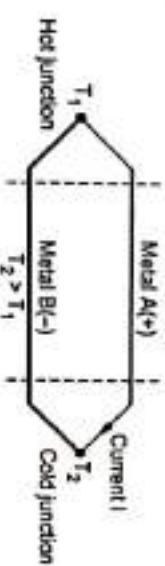


Fig. Q.20.1 (a) Basic circuit of thermocouple

• The magnitude of this e.m.f. depends on the material used for the wires and the temperature difference between the two junctions. The two dissimilar metals form an electric circuit, and a current flows as a result of the generated e.m.f. as shown in Fig. Q.20.1(b).  $e = K(T_1 - T_2)$  where  $K$  is a constant which depends on the material used.

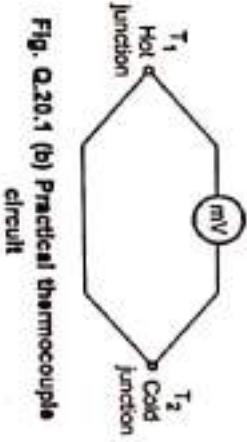


Fig. Q.20.1 (b) Practical thermocouple circuit

**Q.21 Mention the materials used for thermocouples.**

[GATE [SPRU] : May-04,05,06,08, Dec-07, Marks 2]

- Ans. :** • Thermocouples are made from a number of different metals including copper-constantan, iron-constantan, chromel-alumel, platinum-platinum /rhodium. They cover wide range of temperature, going as high as 2700 °C.  
 • The Table Q.21.1 gives the list of important thermocouple materials and the corresponding temperature ranges.

Material used	Types of thermocouple	Temperature range
Copper-constantan	T	- 250 °C to 400 °C
Iron-constantan	J	-200 °C to 850 °C
Chromel-Alumel	K	-200 °C to 110 °C
Chromel-constantan	E	-200 °C to 850 °C
Platinum-platinum-rhodium	S	0 °C to 1400 °C
Tungsten-Molybdenum	-	0 °C to 2700 °C
Tungsten-Rhenium	-	0 °C to 2600 °C

**Table Q.21.1 Thermocouples and temperature ranges****Q.22 State the advantages of thermocouple.**

[GATE [SPRU] : May-04,05,08, Dec-07, Marks 8]

**Ans. :** Advantages of thermocouple are :

1. Rugged in construction.
2. Wide temperature range from - 230 °C to 2700 °C.
3. Small in size.
4. Comparatively cheaper in cost.
5. Easy to calibrate
6. Offers good reproducibility.

7. Speed of response is high.
8. Measurement accuracy is quite satisfactory.
9. External dc supply is not required.

**Q.23 State the limitations of thermocouple.****Ans. :** Limitations of thermocouple are :

1. For accurate temperature measurements, cold junction compensation is necessary.
2. The e.m.f. induced versus temperature characteristics is somewhat nonlinear.
3. Stray voltage pickup is possible.
4. In many applications, amplification of signal is required.

**Q.24 State the applications of thermocouple.**

[GATE [SPRU] : May-04,05,08, Dec-07]

**Ans. :** Applications of thermocouple are :

- Thermocouples are most suitable for temperature measurement of industrial furnaces. They are used in applications where :
- Wide operating temperature range is required.
- Temperatures at remote places are to be measured.
- High response is required.

**Q.25 What is thermistor ?****Ans. :** • Thermistor is a contraction of a term 'thermal-resistors'. Thermistors are semiconductor device which behave as thermal resistors having negative temperature coefficient (NTC); i.e. their resistance decreases as temperature increases.**Q.26 Explain the operating principle of thermistor.**

[GATE [SPRU] : Dec-04, Marks 4]

**Ans. :** • The resistance of thermistor can be expressed as,

$$R_T = R_1 \exp \left[ \beta \left( \frac{1}{T_2} - \frac{1}{T_1} \right) \right]$$

where

$R_t$  : Resistance at  $T^{\circ}\text{K}$   
 $R_1$  : Resistance at known temperature  $T_1^{\circ}\text{K}$   
 $\beta$  : Characteristics temperature.

- The Fig. Q.26.1 shows this characteristic.

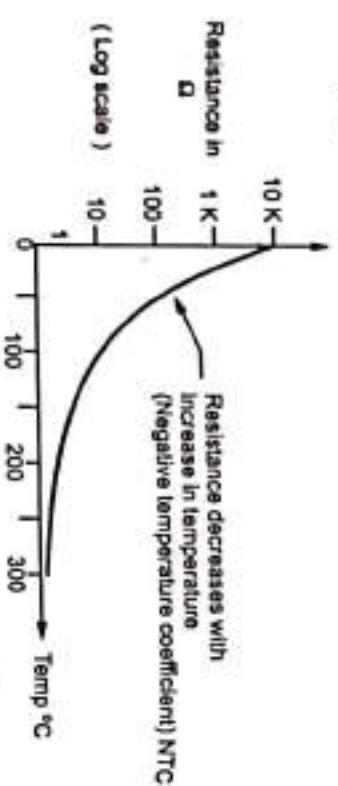


Fig. Q.26.1 Resistance versus temperature characteristics of thermistor

- As seen from the characteristics, thermistors provide a large change in resistance for small change in temperature.

- Measurement of change of resistance of thermistor due to temperature changes is measured by Wheatstone bridge.

**Q.27 State the materials used in a thermistor and explain the construction of it.** [SPRU : May-04, 07, Marks 4]

**Ans. :** Thermistors are composed of a sintered mixture of metallic oxides, such as manganese, nickel, cobalt, copper, iron, and uranium. Their resistances at ambient temperature may range from  $10\ \Omega$  to  $100\ k\Omega$ .

- Thermistors are available in a wide variety of shapes and sizes as shown in the Fig. Q.27.1.

- Smallest in size are the beads with a diameter of 0.15 mm to 1.25 mm. Beads may be sealed in the tips of solid glass rods to form probes. Discs and washers are made by pressing thermistor material under high pressure into flat cylindrical shapes. Washers can be placed in series or in parallel to increase power dissipation rating.

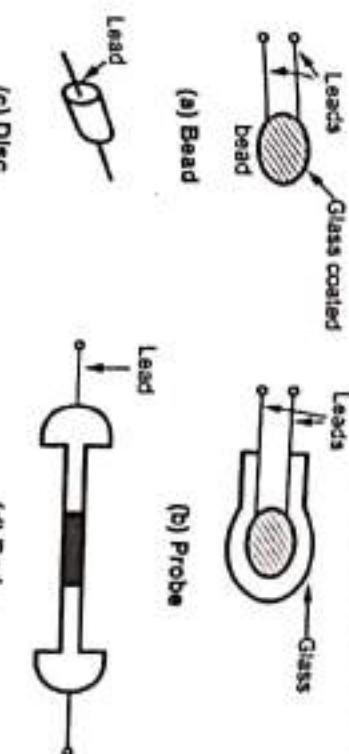


Fig. Q.27.1. Different forms of construction of thermistors

**Q.28 State the advantages of thermistor.** [SPRU : Dec-04, Marks 2]

**Ans. :** 1. Small size.

- Comparatively large change in resistance for a given change in temperature. ( $80\ \Omega/\text{ }^{\circ}\text{C}$ ).

- Fast response over a narrow temperature range.

- Low cost.

**Q.29 State the limitations of thermistor.** [SPRU : Dec-04, Marks 2]

**Ans. :** 1. The resistance versus temperature characteristic is highly nonlinear.

- Not suitable over a wide temperature range.
- Because of high resistance of thermistor, shielded cables have to be used to minimize interference.
- Requires Wheatstone bridge circuit and external power source for measurement.

**Q.30 State the applications of thermistor.** [SPRU : Dec-04, Marks 2]

**Ans. :** 1. The thermistor's relatively large resistance change per degree change in temperature [known as sensitivity] makes it useful as temperature transducer.

2. The high sensitivity, together with the relatively high thermistor resistance that may be selected [e.g. 100 k $\Omega$ ], makes the thermistor ideal for remote measurement or control. Thermistor control systems are inherently sensitive, stable, and fast acting and they require relatively simple circuitry.
3. Because thermistors have a negative temperature coefficient of resistance, thermistors are widely used to compensate for the effects of temperature on circuit performance.
4. Measurement of conductivity.

**Q.31 What is RTD?** [SPRU : May-07, 10, Dec-06, 08, 10, Marks 2]

**Ans.:** • Generally, electrical resistance of any metallic conductor varies according to temperature changes. The primary electrical transducer which measures the temperature using this phenomenon is called Resistance Temperature Detector (RTD), or Resistance Thermometer.

**Q.32 Explain the principle of operation of RTD.**

[SPRU : May-07,10, Dec-06,08,10, Marks 6]

**Ans.:** • The resistance of a conductor changes when its temperature changes. This property is used for the measurement of temperature. The resistance thermometer determines the change in the electrical resistance of the conductor to determine the temperature.

- The relationship between temperature and resistance of conductor is given by equation:

$$R_t = R_{ref} [1 + \alpha \Delta t]$$

where

- $R_t$  : Resistance of the conductor at temperature  $t$  °C,
- $R_{ref}$  : Resistance of the conductor at the reference temperature, usually 0 °C,
- $\alpha$  : Temperature coefficient of the resistance,

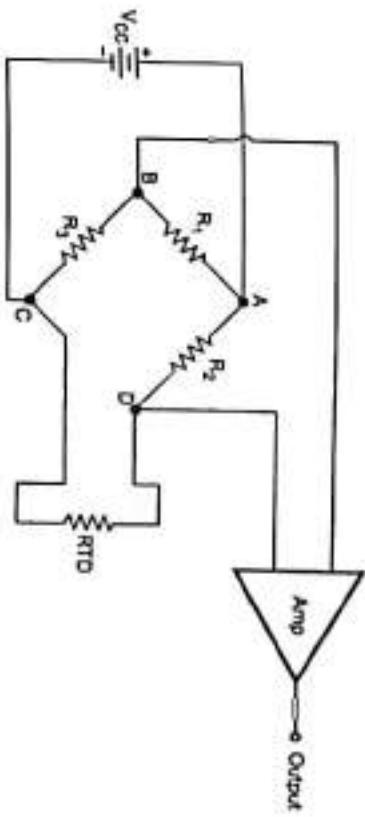


FIG. Q.32.1 RTD resistance measurement

- At 0 °C, the resistance of RTD is usually 100 Ω. By choosing  $R_3 = 100 \Omega$  and  $R_1 = R_2$ , the bridge is balanced at 0 °C. Therefore, at 0 °C voltage across B and D is zero and hence the output voltage is zero.
- Any change in the RTD resistance due to change in temperature unbalances the bridge circuit resulting voltage across B and D terminal. This voltage is proportional to the change in the resistance and hence to the change in the temperature.

**Q.33 Compare three types of temperature transducers or compare RTD with thermistors.**  
 [2R (SPU : Dec.-04, 06, 10, Marks 8)]

**Ans. :**

Parameter	Thermocouple	RTD	Thermistor
Principle of operation	The temperature difference between cold junction and hot junction generates voltage proportional to the temperature difference.	Resistance increases with increase in temperature	Resistance decreases with increase in temperature.
Temperature coefficient	Positive	Positive	Negative
Characteristic	Nonlinear	Linear	Nonlinear
Sensitivity	Medium	Medium	High
Speed of response	High	High	High over narrow temperature range
Operating temperature range	- 270 °C to 2700 °C	- 200 °C to + 650 °C	- 100 °C to + 200 °C
Type of transducer	Active	Passive	Passive
Accuracy	Moderate	High	Moderate
Size	Small	Large	Small
Cost	Low	High	Low
Material used	Copper-Constantan Iron-Constantan Chromel-Alumel etc.	Nickel, Copper, Nickel, Cobalt, Copper, Iron and Uranium	Manganese, Nickel, Cobalt, Copper, Iron and Uranium
Compensation	Cold junction compensation is required.	Not required	Not required

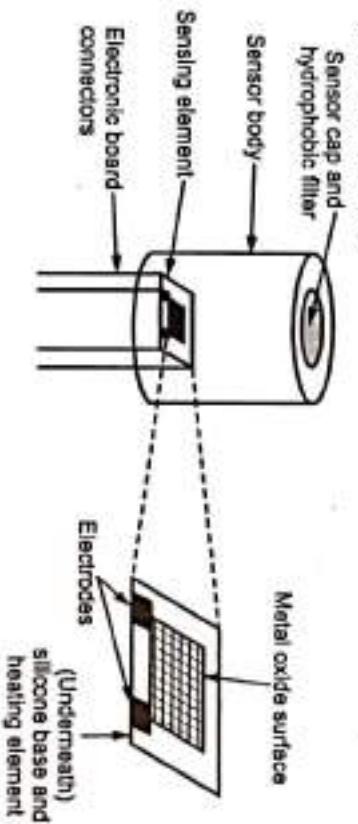
Applications	Suitable for applications which require wide temperature range.	Suitable for applications where speed of response and accuracy are more important.	Suitable for applications where required temperature range is small and sensitivity requirement is high.
<b>5.9 Semiconductor Gas Sensor</b>			

**Q.34 Write a short note on semiconductor gas sensor.**

**Ans. :** • In recent years, semi-conductor gas sensors (or metal oxide sensors, MOX) have become smaller and more powerful. At the same time, they also continue to consume less energy.

• These sensors detect combustible and toxic gases, especially in hazardous atmospheres.

- In these sensors, the metal oxide surface is usually a thin film of a transition or heavy metal that undergoes either oxidation or reduction when a gas comes into contact with it.
- The absorption or desorption of the gas on the metal oxide changes either the conductivity or resistivity from a known baseline value.
- This change in conductivity or resistivity can be measured with electronic circuitry.



**Fig. Q.34.1 Semiconductor gas sensor**

- Semiconductor sensors work best when they have a large surface area. Such a sensor can absorb as much of the target gas as possible particularly at low concentrations.
- Usually the change in conductivity or resistivity is a linear and proportional relationship with gas concentration. Therefore, a simple calibration equation can be established between resistivity/conductivity change and gas concentration.

**Advantages**

- Semiconductor sensors are relatively inexpensive to manufacture due to their simplicity and scalability.

- Specific sensors can be designed for particular applications. For example, a sensor can be designed for low concentration applications whereas an alternative sensor can be designed for high concentration applications.

**Applications**

- Use to detect combustible and toxic gases, especially in hazardous atmospheres.
- Used to detect gas leakages.

**5.10 Optical Sensor - LDR****Q.35 Write a note on LDR.**

- Ans. :** • The light dependent resistor is an electronic component. Light whose resistance decreases with increasing incident light intensity. This allows them to be used in light sensing circuits.
- LDR is also called photo resistor or Fig. Q.35.1 Generation of charge carriers due to light

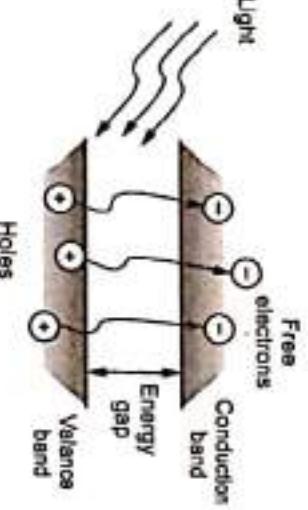


Fig. Q.35.1

- Fig. Q.35.2 shows the symbol of the light dependent resistor.

**Q.36 List the features of LDR.**

**Ans. :** The various features of light dependent resistors are :

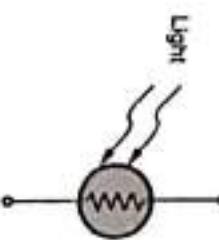
- Wide spectral response
- Low cost
- Wide ambient temperature range

**Q.37 State the applications of LDR.**

**Ans. :** • The light dependent resistors are available in many different types. Their applications are :

- Used in many consumer items such as camera light meters, clock, radios, security alarms and street lights.
- Used for infrared astronomy and infrared spectroscopy.
- Used in sensitive light operated relays.
- Used in light interruption detectors, automatic light circuit, logarithmic law photographic light meter etc.

- Q.38 Discuss any one application of LDR.**
- Ans. :** • Fig. Q.38.3 shows use of light dependent resistor in a sensitive light operated relay.



- The light dependent resistor uses high resistance semiconductor. When light falls on such a semiconductor the bound electrons get the light energy from the incident photons. Due to this additional energy, these electrons become free and jump into the conduction band. The electron-holes pairs are generated. Due to these charge carriers, the conductivity of the device increases, decreasing its resistivity. This is shown in Fig. Q.35.1.

Fig. Q.35.2 Symbol

- Fig. Q.35.2 shows the symbol of the light dependent resistor.

**Q.36 List the features of LDR.**

**Ans. :** The various features of light dependent resistors are :

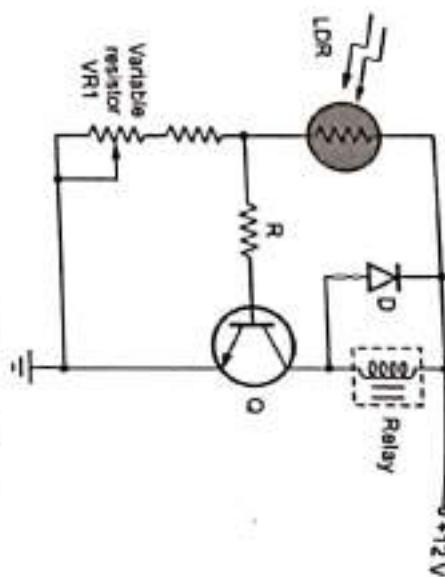
- Wide spectral response
- Low cost
- Wide ambient temperature range

**Q.37 State the applications of LDR.**

**Ans. :** • The light dependent resistors are available in many different types. Their applications are :

- Used in many consumer items such as camera light meters, clock, radios, security alarms and street lights.
- Used for infrared astronomy and infrared spectroscopy.
- Used in sensitive light operated relays.
- Used in light interruption detectors, automatic light circuit, logarithmic law photographic light meter etc.

- Q.38 Discuss any one application of LDR.**
- Ans. :** • Fig. Q.38.3 shows use of light dependent resistor in a sensitive light operated relay.



**Fig. 5.16.3 Sensitive light operated relay**

- The variable resistor VR1 is adjusted in such a way that for the permissible light, the relay is inoperative. When light level increases beyond certain level, the resistance of LDR decreases. This provides proper biasing to the transistor Q and the relay is operated.

### 5.11 Mechanical Sensors - Strain Gauges

**Q.39 What is strain gauge?**

**Ans.:** A strain gauge is a sensor whose resistance varies with applied force; it converts force, pressure, tension, weight, etc., into a change in electrical resistance which can then be measured.

**Q.40 Explain the working principle of strain gauge.**

**Ans.:** When force is applied to any metallic wire its length increases due to the strain. The more is the applied force, more is the strain and more is the increase in length of the wire. If  $L_1$  is the initial length of the wire and  $L_2$  is the final length after application of the force, the strain is given as :

$$\epsilon = (L_2 - L_1)/L_1$$

- Here  $R$  is the resistance of the wire in ohms,  $l$  is the length of the wire in meters, and  $A$  is the cross-sectional area of the wire in  $m^2$ .
- If the length of the wire is stretched uniformly to 2 times its original length, then the cross-sectional area is reduced to  $\frac{1}{2}$  times because the volume ( $V = Al$ ) remains the same.
- Thus the resistance of the wire stretched uniformly to 2 times its original length is given by

$$R = \rho \frac{l \times 2}{A/2} = \rho \frac{l}{A} \times 4$$

which is four times the original resistance of wire.

- This change in resistance of the conductor can be measured easily and calibrated against the applied force. Thus strain gauges can be used to measure force and related parameters like displacement and stress.

**Q.41 Define strain gauge factor.**

**Ans.:** Strain gauge factor of a strain gauge is the ratio of relative change in electrical resistance  $R$ , to the mechanical strain  $\epsilon$ . To get more precise reading this factor should be high.

**Q.42 Give the classification of resistance wire strain gauges.**

**Ans.:** Resistance wire strain gauges are classified as

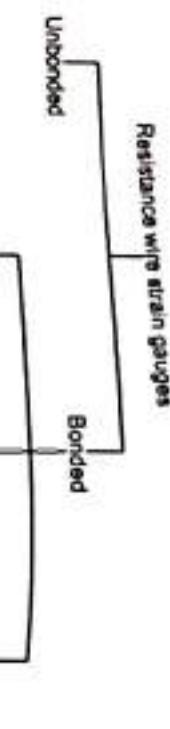


Fig. Q.42.1

**Q.43 Explain the unbonded strain gauge with the help of suitable diagram.**

**Ans. :** • The basic structure of unbonded strain gauge is shown in Fig. Q.43.1.

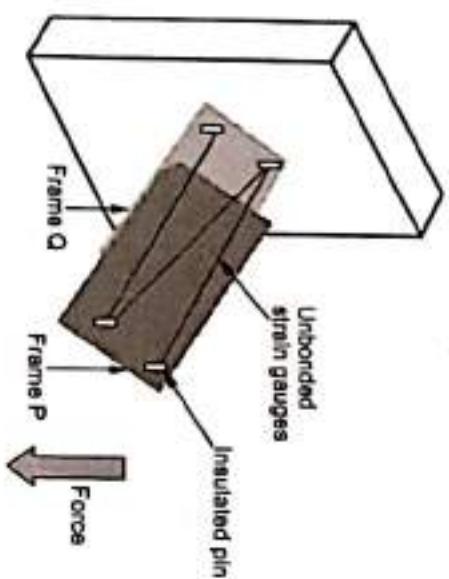


Fig. Q.43.1. Structure of unbonded strain gauge

- It consists of two frames P and Q carrying rigidly fixed insulated pins. These two frames can move relative with respect to each other and they are held together by a spring loaded mechanism.
- A wire is stretched between two points in an insulating medium such as air. A wire is kept under tension so that there is no sag and no free vibration.

**Q.44 What is fine wire strain gauge?**

**Ans. :** • A fine resistance wire diameter 0.025 mm which is looped back and forth on a carrier base as shown in Fig. Q.44.1. This is done to increase the length of the wire so that it permits a uniform distribution of stress. The carrier base protects the gauge from damages. Leads are provided for electrically connecting the strain gauge to a measuring instrument such as Wheatstone bridge.

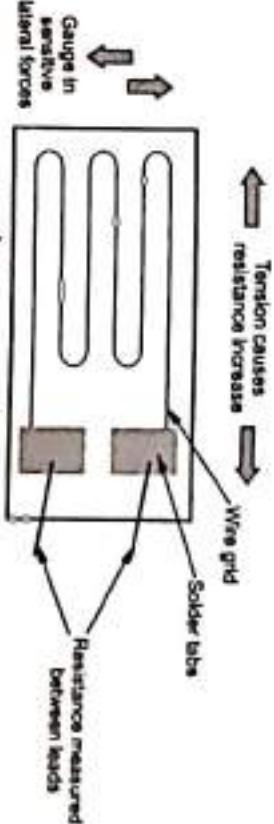


Fig. Q.44.1 Fine wire strain gauge

**Q.45 What is metal foil strain gauge ?**

**Ans. :** • Fig. Q.45.1 shows the structure of metal foil strain gauge. In this strain gauge, the strain is measured using a metal foil. The metals and alloys used for the foil are nichrome, constantan, isoelastic leads (Ni + Cr + Mo), nickel and platinum.

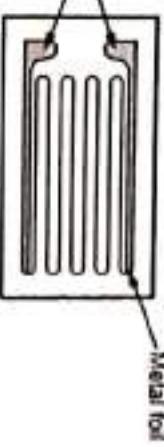


Fig. Q.45.1 Foil strain gauge

- On account of their larger surface area, foil gauges have a much greater dissipation capacity. Therefore, they can be used at a higher operating temperature range. The characteristics of foil type strain gauges and wire type strain gauges are similar, including almost the same gauge factor.

**Q.46 State the advantages of metal foil type strain gauge.**

Ans. : • The advantage of foil type strain gauges are :

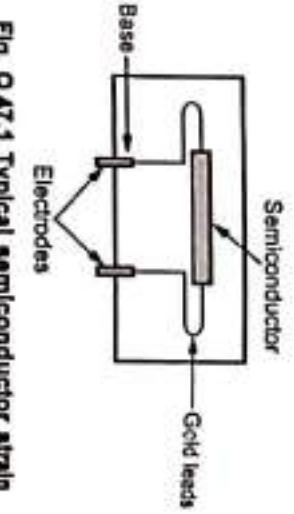
- They can be fabricated on a large scale, and in any shape.
- Perfect bonding of the strain gauge is possible.
- They are more flexible.
- They have a better fatigue life.
- Has good sensitivity and have stability even at high temperatures.

**Q.47 Write a note semiconductor strain gauge.**

Ans. : • A typical semiconductor strain gauge is formed by the semiconductor technology i.e., the semiconducting wafers or filaments of length varying from 2 mm to 10 mm and thickness of 0.05 mm are bonded on suitable insulating substrates (for example Teflon). The gold leads are usually employed for making electrical contacts. The electrodes are formed by vapour deposition.

The assembly is placed in a protective box as shown in the Fig. Q47.1.

- The strain sensitive element used by the semiconductor strain gauge is rectangular filament made as a wafer from silicon or germanium crystals. To these crystals, boron is added to get some desired properties. This process is called doping and the crystals are called doped crystals.



**Fig. Q47.1 Typical semiconductor strain gauge**

- Strain sensitivity of semiconductor material depends on the crystal material, doping levels, type of doping materials, crystal type axis orientation and so on.
- Basic principle of operation of the semiconductor strain gauge is the piezo-resistive effect; i.e. when strain is applied there is a change in the value of resistance due to change in resistivity of the semiconductor.

• This change in resistance of the semiconductor can be measured easily and calibrated against the applied strain with the help of a wheatstone bridge.

**Q.48 State advantages and disadvantages of semiconductor strain gauges.**

Ans. : • Advantages of semiconductor strain gauges are :

- High gauge factor of about 130.
- Hysteresis characteristics of semiconductor strain gauge is excellent
- Life of the semiconductor strain gauge is long more than 10<sup>7</sup> operations.
- Excellent frequency response.
- Semiconductor strain gauge is very small in size.

• Disadvantages of semiconductor strain gauges are :

- Sensitive to changes in temperature.
- Poor linearity.
- More expensive.
- Gauge factor varies with strain.

**Q.49 Give the comparison between semiconductor and metal strain gauges.**

Ans. : • Table Q49.1 gives the comparison between semiconductor and metal strain gauges.

Sr. No	Characteristics	Metal wire / foil gauge	Semiconductor gauge
1.	Size	Large	Very small
2.	Gauge factor	Small	Very high
3.	Linearity	Very good	Poor
4.	Temperature stability	Very good	Poor
5.	Elastic strain range	Low due to plastic flow and hysteresis in the metal	High in silicon gauges
6.	Fatigue life	Low	High
7.	Protection from strong fluctuating light	Not required	Necessary due to photosensitivity of semiconductors
8.	Application requirement	-	Required to reduce non-linearity and temperature instability
9.	Cost	Low	High

Table Q.49.1

**Q.50 Write a note on Rosette strain gauges.**

Ans. : • The wire strain gauge can effectively measure strain in only one direction. However, there is a need to simultaneously measure strain in more than one direction in both stress analysis and transducer applications.

- This need can be accomplished by rosette strain gauges. In rosette strain gauge, the required number of single element gauges are placed at the proper locations for independent measurement of strain.
- Single strain gauges are used to measure only those strains which are parallel to the strain axis.
- But when the direction of the strain is unknown, it is necessary to use a multiple array of gauges which permit the calculation of the direction as well as the magnitude of the two principal strains.

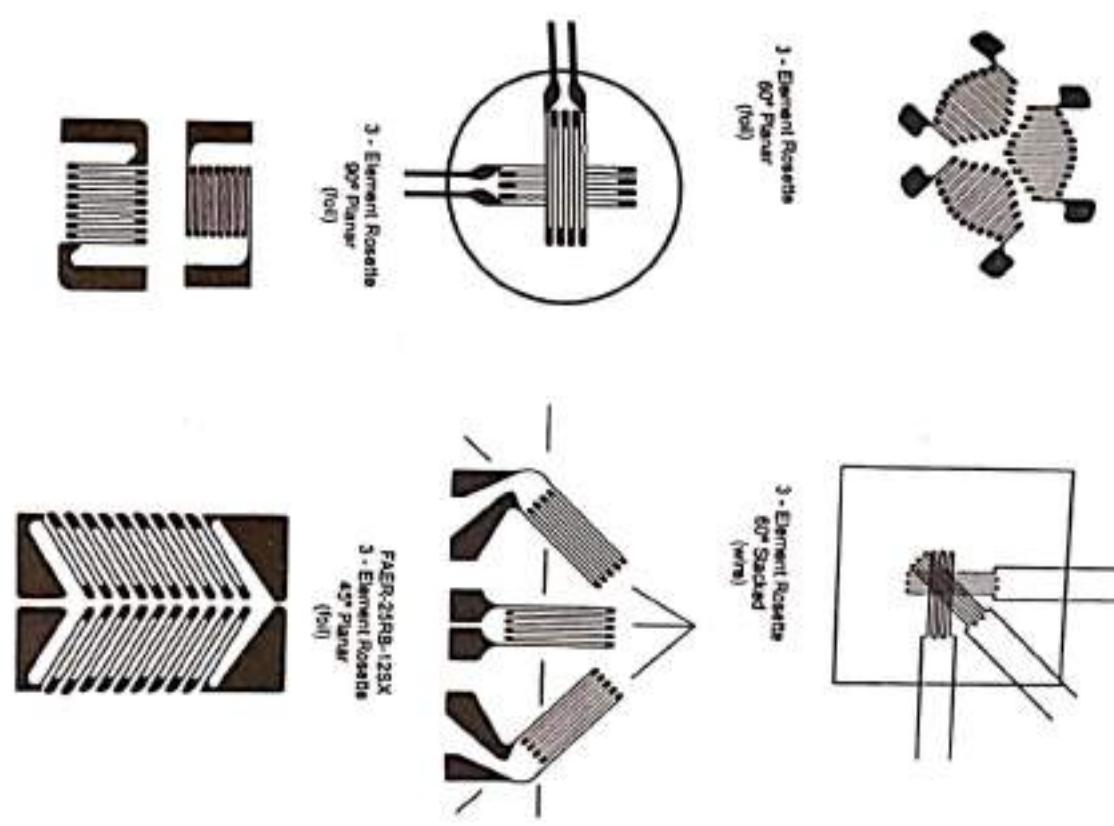


Fig. Q.50.1

- Three or four arm "rosette" gauges are most commonly used. To make the calculations easier, gauges are usually set with either 45 or 60 angles between them. Fig. Q.50.1 shows some forms of rosettes.

### 5.12 Mechanical Sensor - Load Cell

#### Q.51 What is load cell?

**Ans.:** A load cell is an electro-mechanical device used for measurement of weights. It converts weight (or force) into an electrical signal. It is mostly used in industrial applications for static and dynamic force measurements. A load cell consists of a load receiving element i.e. elastic element with high tensile strength as primary transducer and strain gauges arranged in bridge network as secondary network.

#### Q.52 Explain the construction and operating principle of load cell.

**Ans.:** • A load cell is based on a principle that a force applied to an elastic element produces a measurable deflection/deformation. A load cell produces an electrical signal proportional to this deformation.

- The important part of the load cell is the bonded-foil strain gauge which is an extremely sensitive device, whose electrical resistance changes in direct proportion to the applied force.

- A load cell comprises an elastic element. The elastic element is made up of steel alloys which are homogeneous materials.
- The basic design constraints are relative size and shape, density of material, modulus of elasticity, strain sensitivity and dynamic response.
- The elastic elements used are designed and shaped according to specific requirements. The elastic elements of different shapes are as shown in the Fig. Q.52.1.

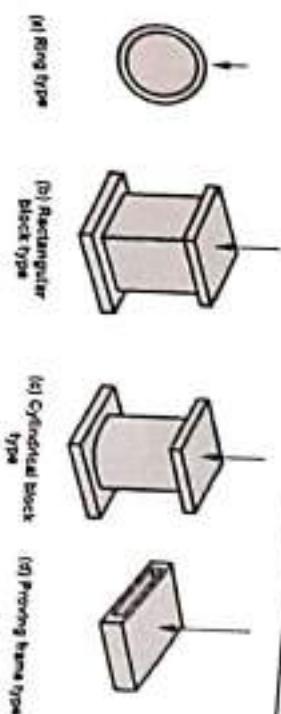


Fig. Q.52.1

#### Q.53 State the main types of load cell.

**Ans.:** The two main types of load cells are :

- Tension - compression (column type) load cell.
- Cantilever beam type load cell.

#### Q.54 State advantages and disadvantages of load cell.

**Ans.:** The advantages of load cell are :

- The great advantage of strain gauge load cell is that the effect of temperature can be compensated using bridge circuitry.
- Rugged and compact construction.
- No moving parts and negligible deflection under load.
- Highly accurate 0.01 to 1.0 %.
- Wide load range.
- The load cell can be employed for static as well as dynamic type of loading.

The disadvantages of load cell are :

- Mounting of strain gauge is critical.
- Calibration is tedious process.

#### Q.55 State the applications of load cell.

**Ans.:** The load cell finds its use in various applications like -

- Measurement of force, pressure, displacement.
- Weigh platforms for domestic and industrial purpose.

3. Process control systems.
4. Freight and baggage weighing

### 5.13 Mechanical Sensor – Pressure Sensors

**Q.56 What is pressure sensor ?**

**Ans. :** A pressure sensor is a device which senses pressure and converts it into an analog electric signal whose magnitude depends upon the pressure applied. Since they convert pressure into an electrical signal, they are also termed as pressure transducers.

**Q.57 What are the types of pressure sensor ?**

**Ans. :** • Most common types of pressure sensors are :

1. Strain gauge pressure sensor
2. Capacitive pressure sensor
3. Piezoelectric pressure sensor

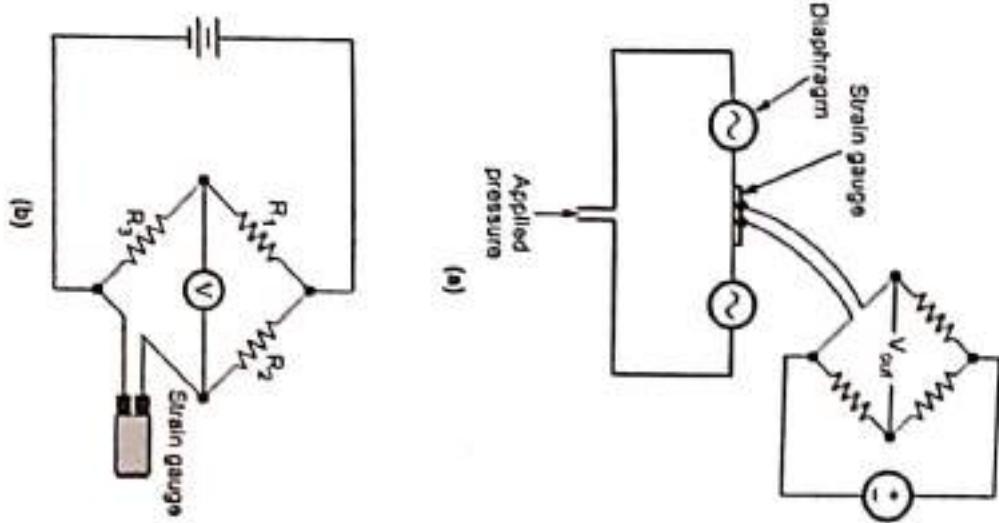
**Q.58 Explain the working of strain gauge pressure sensor.**

**Ans. :** • The strain gauge is a passive transducer used to measure pressure.

• Attaching a strain gauge to a diaphragm results in a device that changes resistance with applied pressure. Pressure forces the diaphragm to deform, which in turn causes the strain gauge to change resistance. Thus arrangement is shown in Fig. Q.58.1 (a).

• The change in resistance of strain gauge is converted into electric voltage using Wheatstone bridge. This arrangement is shown in Fig. Q.58.1 (b).

- In wheat stone bridge, the ratio of resistors of two adjacent arms connected to one end of the battery should be equal to that of other two arms connected to another end of battery. When the two ratios are equal, no output is generated from the wheat stone bridge.



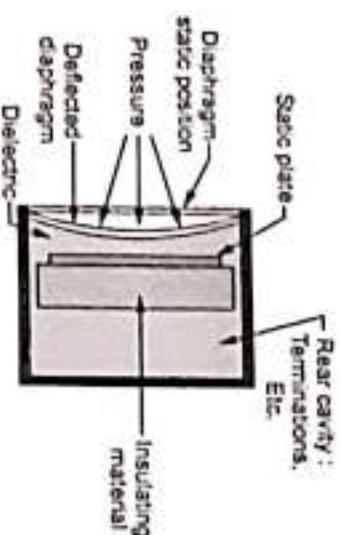
**FIG. Q.58.1 Pressure Sensor**

- The change in the resistance of the strain gauge breaks the balance of the Wheatstone's bridge and change the voltage  $V$ . The voltage  $V$  is proportional to the pressure change in the strain gauge.

**Q.59 Explain the working of capacitive pressure sensor.**

**Ans. :** • Fig. Q.59.1 shows capacitive pressure sensor.

- A capacitor has two metal plates and a dielectric sandwiched between them.



**Fig. Q.59.1 Capacitive pressure sensor**

- In capacitive pressure sensor, one of these metal plates is permitted to move in and out so that the capacitance between them changes due to varying distance between the plates.
- The movable plate is connected to a diaphragm which senses the pressure and then expands or compresses accordingly. The movement of the diaphragm affects the attached metal plate's position and capacitance varies.

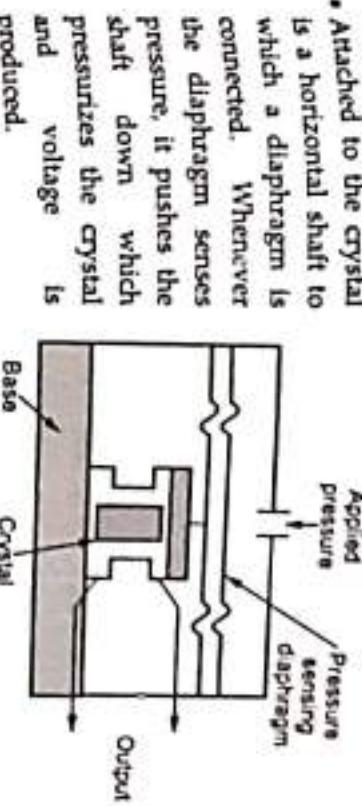
• These pressure sensors, though much ineffective at high temperatures, are widely used at ambient temperature range due to their linear output.

**Q.60 Write a note on piezoelectric pressure sensor.**

**Ans. :** • Piezoelectric crystals develop a potential difference (i.e. voltage is induced across the surfaces) whenever they are subjected to any mechanical pressure.

• Fig. Q.60.1 shows the piezoelectric pressure sensor. As shown in Fig. Q.60.1, these sensors have the crystal mounted on a dielectric base so that there is no current leakage.

• Attached to the crystal is a horizontal shaft to which a diaphragm is connected. Whenever the diaphragm senses pressure, it pushes the shaft down which pressurizes the crystal and voltage is produced.



**Fig. Q.60.1 Piezoelectric pressure sensor**

**Q.61 What is a Biosensor ?**

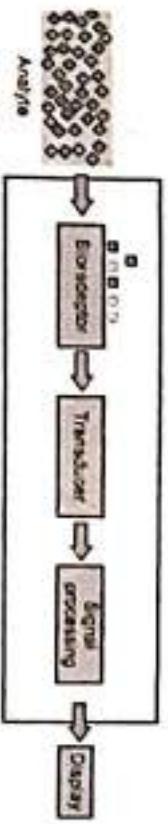
**Ans. :** • A biosensor is a device that measures biological or chemical reactions by generating signals proportional to the concentration of an analyte in the reaction. It includes a combination of biological detecting elements like sensor system and a transducer.

**Q.62 Explain the construction of biosensor.**

**Ans. :** • A typical biosensor is represented in Fig Q.62.1. It consists of the following components :

1. Analyte
2. Bioreceptor
3. Transducer

→ Detected molecule



**Fig. Q.62.1 Biosensor**

- Analyte : A substance of interest that needs detection. For instance, glucose is an 'analyte' in a biosensor designed to detect glucose.

- Bioreceptor :** A molecule that specifically recognizes the analyte is known as a bioreceptor. Enzymes, cells, aptamers, deoxyribonucleic acid (DNA) and antibodies are some examples of bioreceptors. The process of signal generation (in the form of light, heat, pH, charge or mass change, etc.) upon interaction of the bioreceptor with the analyte is termed bio-recognition.
- Transducer :** In a biosensor the role of the transducer is to convert the bio-recognition event into a measurable signal.

**Q.63 Explain the working of biosensor with the help of neat block diagram.**

**Ans. :** • Biosensors are operated based on the principle of signal transduction. These components include a bio-recognition element,

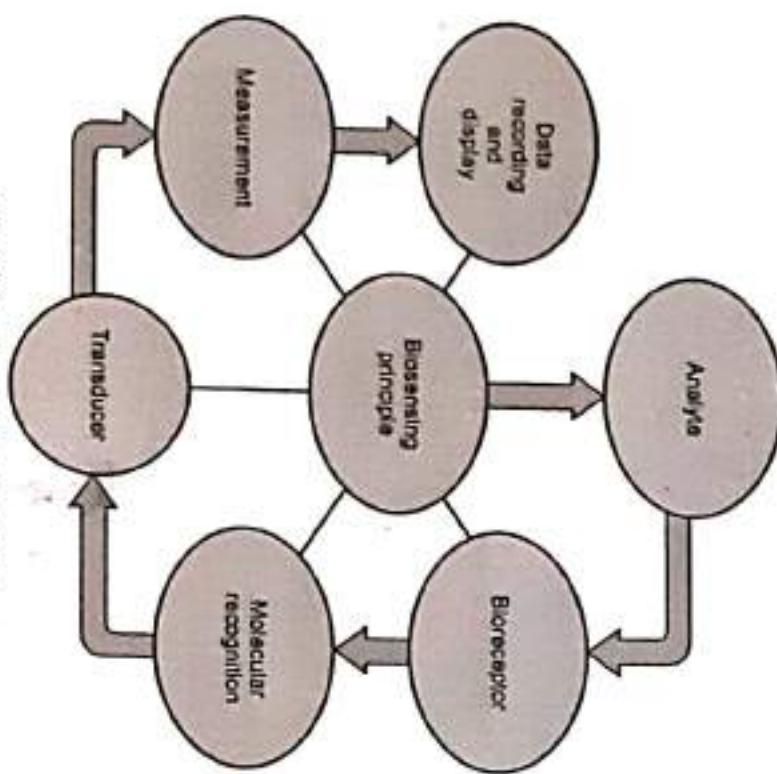


Fig. Q.63.1 Bio-sensing principle

- a biotransducer and an electronic system composed of a display, processor and amplifier.
- The bio-recognition element, essentially a bioreceptor, is allowed to interact with a specific analyte. The transducer measures this interaction and outputs a signal. The intensity of the signal output is proportional to the concentration of the analyte. The signal is then amplified and processed by the electronic system.

**Q.64 List the types of biosensor.**

**Ans. :** • Depending on the mechanism of transduction, biosensors are classified as follows :

1. Resonant biosensors
2. Optical detection biosensors
3. Thermal detection biosensors
4. Ion sensitive biosensors
5. Electrochemical biosensors

**Q.65 List the characteristics of biosensor.**

**Ans. :** The important characteristics of biosensors are :

- Selectivity :** It is the ability of a bioreceptor to detect a specific analyte in a sample containing other admixtures and contaminants.
- Sensitivity :** The minimum amount of analyte that can be detected by a biosensor defines its Limit Of Detection (LOD) or sensitivity.
- Reproducibility :** It is the ability of the biosensor to generate identical responses for a duplicated experimental set-up. The reproducibility is also characterised by the precision and accuracy of the transducer in a biosensor.
- Stability :** It is the degree of susceptibility to ambient disturbances in and around the biosensing system. These disturbances can cause a drift in the output signals of a biosensor under measurement. This can cause an error in the measured concentration and can affect the precision and accuracy of the biosensor.

- **Linearity :** It is the attribute that shows the accuracy of the measured response (for a set of measurements with different concentrations of analyte) to a straight line, mathematically represented as  $y = mc$ , where  $c$  is the concentration of the analyte,  $y$  is the output signal, and  $m$  is the sensitivity of the biosensor.

• **Resolution :** It is defined as the smallest change in the concentration of an analyte that is required to bring a change in the response of the biosensor.

• **Response time :** The necessary time for having 95 % of the response.

#### Q.66 State the applications of biosensors.

**Ans.:** • Some of the major applications of biosensors are listed below :

1. **Medicine and health :** Biosensors are successfully used for the quantitative estimation of several biologically important substances in body fluids e.g. glucose, cholesterol, urea.
2. **Industry :** Biosensors can be used for monitoring of fermentation products and estimation of various ions.
3. **Pollution control :** Biosensors are very helpful to monitor environmental (air, water) pollution.
4. **Military :** Biosensors have been developed to detect the toxic gases and other chemical agents used during war.
5. **Food Industry :** Biosensors for the measurement of carbohydrates, alcohols, and acids are commercially available. They are used for monitoring food authenticity, quality and safety.

#### Q.67 Write a note on blood glucose biosensor.

**Ans.:** • The blood glucose Biosensors are used widely throughout the world for diabetic patients.

• The enzyme glucose oxidase catalyzes the oxidation of D-glucose according to the following reaction.



- Three means are available for measuring glucose concentration with electrochemical transducers : 1) The fall in  $\text{O}_2$  as the reaction proceeds, (2) The production of  $\text{H}_2\text{O}_2$ , and (3) The change in pH with production of D-gluconic acid.

• A typical sensor uses an electrochemical transducer to measure glucose concentration based on the change in  $\text{O}_2$  in the glucose oxidase-catalyzed reaction.

• Fig. Q.67.1 shows differential biosensor to measure glucose using two  $\text{O}_2$  electrodes.

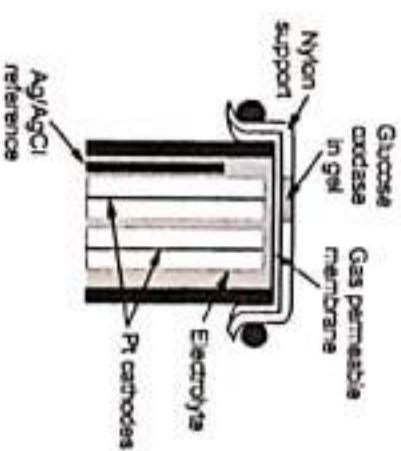


Fig. Q.67.1 Differential biosensor to measure glucose

- One electrode is used to measure ambient  $\text{O}_2$  level to interpret measurement for  $\text{O}_2$  utilized in glucose oxidase-catalyzed reaction in substrate over second  $\text{O}_2$  electrode.

END... ↗

# 6

## Communication Systems

### 6.1 : Importance of Communication System

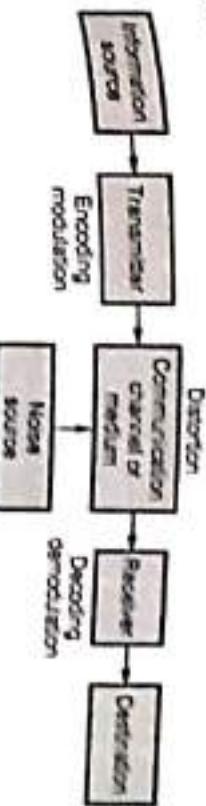
#### Q.1 State the importance of communication system.

**IS [SPNU : May-17, Marks 2]**

- Ans :**
- The best forms of electronic communication, such as radio, television and internet have increased our ability to share information. Today they form the major part of our lives.
  - The electronic communication made it possible for we to communicate almost any time and anywhere.
  - Number of electronic communication channels such as electronic mail (Email), instant messaging, text messaging, post-cast (it is digital media file that is distributed over the internet and downloaded on portable media players and personal computers), blogs enable everyone to exchange information rapidly and efficiently.
  - Social networking sites such as facebook, orkut, twitter have become some of the key online sources and information sharing tools.
  - In today's world every one is so it is hard to imagine living without the knowledge and information that arrive from around the world by electronic communication.

### 6.2 : Block Diagram of Communication System

**Q.2 Explain the elements of communication system with the help of block diagram.** **OR** [Pre : Dec-09, 12, 11, 14, May-11, 17, 18, Marks 5]



**Fig. Q.2.1 Block diagram of communication system**

• The elements of communication system are as follows :

- Information
- Transmitter
- Communication channel or medium
- Noise
- Receiver

**Information :** The communication systems communicate messages. They may contain human voice, picture, code, data, music and their combinations.

**Transmitter :** The transmitter is a collection of electronic circuits designed to convert the information into a signal suitable for transmission over a given communication medium.

**Communication channel :** The communication channel is the medium by which the electronic signal is transmitted from one place to another. The communication medium can be a pair of conducting wires, coaxial cable, optical fibre cable or free space.

**Noise :** Noise is random, undesirable electric energy that enters the communication system via the medium and interferes with the transmitted message. Some noise is also produced in the receiver. Noise is one of the serious problems of electronic communication. It cannot be completely eliminated. However, there are ways to deal with noise, and reduce the possibility of degradation of signal due to noise.

**Basic Electronics Engineering** **6 - 2** **Communication Systems**  
**Ans :** • Any electronic communication system can be represented in its basic form, as shown in the Fig Q.2.1.

Ans. :

**Receiver** : A receiver is a collection of electronic circuits designed to convert the signal back to the original information. It consists of amplifier, detector, mixer, oscillator, transducer and so on.

### 6.3 : Modes of Transmission

#### Q.3 Explain various modes of transmission.

Ans. : • There are four modes of transmission used in telecommunication and computer networking :

1. Simplex
2. Half duplex
3. Full duplex
4. Full/Full duplex

#### 1. Simplex

- In simplex mode, data transmission is unidirectional and thus the information can be sent only in one direction.

- A radio station usually sends signals to the audience but never receives signals from them, thus a radio station is an example of simplex mode of transmission.

#### 2. Half duplex

- In half duplex mode, data can be transmitted in both directions on a signal carrier but not at the same time.

- Walkie-talkie is a typical example of half duplex mode of transmission.

- In full duplex mode, data can be transmitted in both directions simultaneously, but they must be between the same stations.

- A local telephone call is an example of full duplex transmission mode.

- In full/full duplex mode, data can be transmitted in both directions at the same time but not between the same two stations (i.e., one station is transmitting to a second station and receiving from the third station at the same time).

#### Q.4 Give comparison between various modes of transmission.

Basis for Comparison	Simplex	Half Duplex	Full Duplex	Full/Full Duplex
Direction of Communication	Unidirectional	Two - directional, one at a time	Two - directional, simultaneously between same stations	Two - directional, but not simultaneously between same stations
Send / Receive	Sender can only send data.	Sender can send and receive data, but one at a time.	Sender can send and receive data simultaneously.	Sender can send and receive data simultaneously.
Example	Radio station	Walkie - talkie	Local Telephone	U.S. Postal system

### 6.4 : Communication Media : Wired and Wireless

#### Q.5 What is wireless and wireline communication ?

Ans. : According the transmission media the communication can be classified as :

- **Wireless communication** : As the name indicates, there is no wire or any such medium for conduction of electromagnetic waves. Wireless communication takes place through air or vacuum. The frequencies right from 10 kHz up to 100 GHz are transmitted using wireless communication. Such communication is also called radio communication.

- **Wire/wireline communication** : In wire/wireline communication, communication takes place through wire pairs or coaxial cables. The telephone system is an example of wire/wireline communication system. Such communication is also called line communication.

#### Q.6 State the types of wired media of transmission.

- Ans. : The types of wired media of transmission are :
1. Twisted pair cable
  2. Co-axial cable
  3. Optical fiber cable

**Q.7 Write a note on twisted pair cables.** EF [SPU : Dec-09, May-17, March 1]

**Ans. :** • Twisted pair cabling is a form of wiring in which two conductors are wound together for the purposes of cancelling out electromagnetic interference from external sources and crosstalk from neighbouring wires. The Fig. Q.7.1 shows the twisted pair.



Fig. Q.7.1 Twisted pair

- Twisted pair cables are often shielded to prevent electromagnetic interference. Because the shielding is made of metal, it also serves as a ground. This shielding can be applied to individual pairs or to the collection of pairs. When shielding is applied to the collection of pairs, this is referred to as screening. The shielding must be grounded for the shielding to work.
- There are four types of twisted pair cables. These are :
  - Unshielded Twisted Pair (UTP)
  - Shielded Twisted Pair (STP)
  - Screened Shielded Twisted Pair (S/STP)
  - Screened Unshielded Twisted Pair (S/UTP)

**Q.8 State the advantages of twisted pair.**

**Ans. :** Advantages of twisted-pair cables

- High availability
- Low cost of installation
- Low cost for local moves, adds and changes in places.

**Q.9 State the disadvantages of twisted pair.**

**OR Explain problems associated with twisted pair cables.**

EF [SPU : Dec-10 , March 1]

**Ans. 1 Disadvantages of twisted-pair cables are :**

- They provide limited frequency response about 1 MHz.
- Limited data rate - The longer a signal has to travel over twisted-pair, the lower the data rate.
- Short distances are required between repeaters.
- Twisted pairs are highly susceptible to signal interference such as EMI and RFI.
- Power loss due to conduction and radiation.

**Q.10 State the applications of twisted pair cables.**

**Ans. :** Twisted pair cables are used in following applications :

1. Telephone systems
2. Data networks for short and medium length connections
3. Ethernet and ring networks
4. Local area networks
5. Internet Services Digital Network (ISDN).

**Q.11 Write a note on coaxial cable.** EF [SPU : May-13,17,18, March 3 ]

**Ans. :** • The co-axial cable consists of a solid-center conductor surrounded by a plastic insulator such as Teflon. Over the insulator is a second conductor, a tubular braid or shield made of fine wire, as shown in Fig. Q.11.1. An outer sheath protects and insulates the braid.

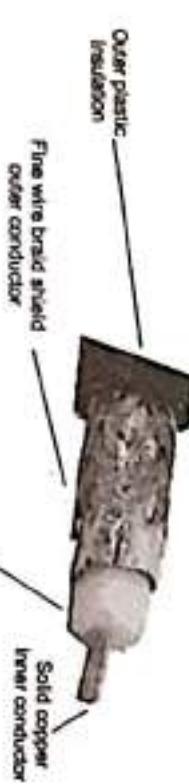


Fig. Q.11.1 Co-axial cable

- Co-axial cables may be rigid or flexible. Rigid types have a solid sheath, while flexible types have a braided sheath, both usually of thin copper wire.

- The inner insulator, also called the dielectric, has a significant effect on the cable's properties, such as its characteristic impedance and its attenuation.
- The fine wire braid shield protects the wire from electromagnetic interference (EMI).

**Q.12 State the advantages of coaxial cable.** **ER** [SPPU : May-14, Maths 7]

**Ans.:** The advantages of coaxial cable are :

- Greater bandwidth.
- Lower losses.
- Much lower crosstalk.
- Excellent noise immunity.
- Lens attenuation of signal as compared to twisted pair cable.
- Less expensive as compare to fiber optic cables.

**Q.13 State the disadvantages of coaxial cable.**

**ER** [SPPU : May-14, Maths 7]

**Ans.:** The disadvantages of coaxial cable are :

- Expensive as compared to twisted pair cable.
- Power loss due to conduction.
- Possibility of short circuit between two conductors.

**Q.14 State applications of coaxial cables.** **ER** [SPPU : May-14, Maths 7]

**Ans.:** They are used as a high-frequency transmission line to carry a high-frequency or broad band signal.

- Cable TV.

- Home Video equipment.

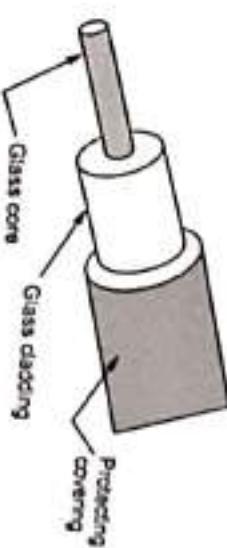
- Fast LAN.
- Conventional LAN.
- Cable modem.

**Q.15 Write a short note on fiber optic cable.**

**ER** [SPPU : May-12, 14, 17, 18, Maths 1]

**OR What are the main sections of an optical fiber? Explain the function of each section.** **ER** [SPPU : May-09, Dec-10, Maths 1]

**Ans.:** • The light in a fiber-optic cable travels through the core by constantly bouncing from the cladding (mirror-lined walls), a principle called total internal reflection.



**Fig. Q.15.1 Fiber optic cable**

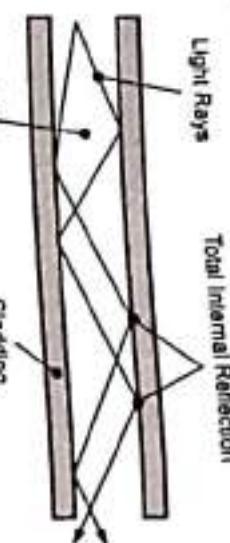
- The core and the cladding (which has a lower-refractive-index) are usually made of high quality silica glass, although they can be made of plastic as well.
- A light source is placed at the end of the fiber and light passes through it and exits at the other end of the cable. The fiber optic cable can carry information such as voice, video and computer data.
- Voice and video signals are converted into binary or digital pulses before being transmitted by a light beam. At the receiving end, the light beam is converted into binary or digital pulses and then into original voice or video signals.

**Q.16 Explain how light travels through a fiber.**

**ER** [SPPU : May-14, Maths 1]

- Ans.:** • The light in a fiber-optic cable travels through the core by constantly bouncing from the cladding (mirror-lined walls), a principle called total internal reflection.

- Fig. Q.16.1 gives an illustration of how light travels down a fiber optic cable.



**Fig. Q.16.1 Illustration of how light travels down a fiber optic cable.**

- Because the cladding does not absorb any light from the core, the light wave can travel great distances. However, some of the light signal degrades within the fiber, mostly due to impurities in the glass.

**Q.17 List the benefits of fiber optic cables.** [UPPU : Dec-17, Marks 2]

Ans. :

Sr. No.	Benefit
1.	Wider bandwidth : Higher information carrying capability.
2.	Lower loss : Less signal attenuation over long distance.

**Q.18 Give the disadvantages of optic fiber cables.**

Ans. : • The disadvantages of optic fiber cables are :

- Expensive.
- Joining the optical fiber cables is not simple.
- Installation is difficult.

**Q.19 State the applications of fiber optic cables.**

Ans. : • For voice, video and computer data transmission.

- Telephone systems.
- Light and infrared transmission.
- Local area networks.

**Q.20 Give the comparison between twisted pair, co-axial cable and fiber optic cable.**

Ans. :

Sr. No.	Twisted pair	Co-axial cable	Fiber optic cable
1.	Uses electrical signal for transmission.	Uses electrical signal for transmission.	Uses optical signal for transmission.
2.	Provides low noise immunity.	Provides higher noise immunity than twisted pair.	Provides highest noise immunity as the light rays are unaffected by the electrical noise.
3.	Affected due to electromagnetic field.	Less affected due to electromagnetic field.	Does not get affected by electromagnetic field.

**Table Q.17.1**

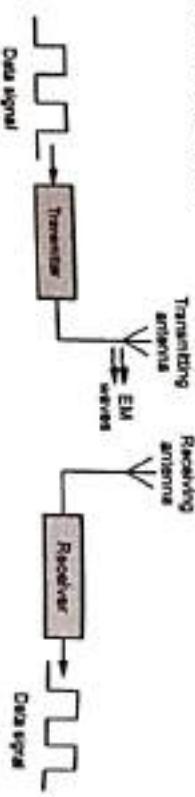
- Microwave and
- Infrared

**Q.22 Compare the advantages and disadvantages of wireless media.**

Ans. :	Channel	Advantages	Disadvantages
Radio	High bandwidth. Signals pass through walls.	Creates electrical interference problems. Susceptible to snooping unless encrypted.	
Microwave	High bandwidth. Relatively inexpensive.	Must have unobstructed line of sight. Susceptible to environmental interference.	
Infrared	Low to medium bandwidth. Used only for short distances.	Must have unobstructed line of sight.	

**Q.21 What is wireless transmission media ?**

**Ans. :** As the name indicates, in wireless transmission, there is no wire or any guided media as a communication channel.



**Fig. Q.21.1 Wireless transmission**

- Wireless communication takes place through air or vacuum.
  - In wireless communication two antennas are used : Transmitting antenna and receiving antenna.
  - The transmitter transmits data signal in the form of electromagnetic waves with the help of transmitting antenna and receiving antenna receives these electromagnetic waves. Receiver converts received electromagnetic waves into data signal.
- The three types of wireless media are
- Radio wave

**Q.23 Compare wired and wireless media.**

**Ans. :**

Sr. No.	(Wired) guided media	(Wireless) unguided media
1.	The signal energy propagates within the guided media.	The signal energy propagates through air.
2.	Guided media is mainly suited for point-to-point communication.	Unguided media is mainly used for broadcasting purpose.
3.	The signal propagates in guided media in the form of voltage. Current or photons.	The signal propagates in unguided media in the form of electromagnetic waves.
4.	Examples of guided media are <ul style="list-style-type: none"> <li>- twisted pair cables</li> <li>- co-axial cable</li> <li>- optical fiber cable.</li> </ul>	Examples of unguided media are <ul style="list-style-type: none"> <li>- microwave or radio links</li> <li>- infrared</li> </ul>

### 6.5 : Electromagnetic Spectrum

**Q.24 Draw and explain electromagnetic spectrum ?**

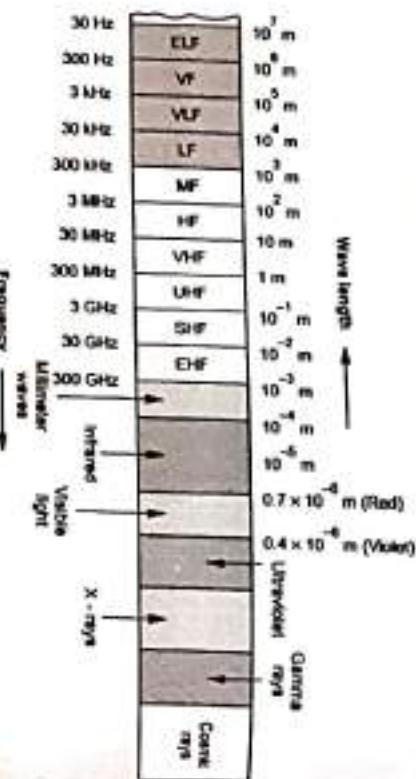
[GATE 2011 : Dec-09,14, May-11,13, Maths]

**Ans. :** • In wireless communication, electromagnetic waves are used as a media of transfer of information. Thus in such a communication, the information signal is converted into the electromagnetic signal before transmission.

• The electromagnetic (EM) waves consist of both electric and magnetic fields and they can travel a long distance through space.

• The range of all possible frequencies of EM waves is called the electromagnetic (EM) spectrum.

• The Fig. Q.24.1 shows the electromagnetic spectrum. The electromagnetic spectrum, shown in the Fig. Q.24.1 extends from just below the frequencies used for modern radio (at the long-wavelength end) to gamma radiation (at the short-wavelength end).



**Fig. Q.24.1 Electromagnetic spectrum**

- In the midrange includes most commonly used radio frequencies for two-way communications, television and other applications.

• The infrared and visible light are at the upper and of the EM spectrum.

**Q.25 Define frequency and wavelength. Also state the relation between them.**

**Ans. :** • The frequency is defined as the number of cycles of a waveform per second. It is expressed in hertz.

• Wavelength is defined as the distance traveled by an electromagnetic wave during the time of one cycle.

$$\text{Wavelength } (\lambda) = \frac{\text{Speed of light}}{\text{Frequency}} = \frac{c}{f}$$

where c is the speed of light = 300,000 km/s

• Electromagnetic energy at a particular wavelength is given by  $E = hf$  where h is Planck's constant = 4.13564 μeV/GHz

• So, high-frequency electromagnetic waves have a short wavelength and high energy; low-frequency waves have a long wavelength and low energy.

**Q.26 What is RF ?**

**Ans. :** Radio frequency or RF refers to that portion of the electromagnetic spectrum in which electromagnetic waves can be generated by alternating current fed to an antenna.

**Q.27 Describes the radio frequency spectrum and its applications according to various frequency bands.**

**OR Lists the applications of electromagnetic spectrum of IEEE frequency spectrum.**

**Ans. :** The Table Q.27.1 shows the radio frequency spectrum and its applications according to various frequency bands.

Frequency band	Frequency	Wavelength	Applications
Extremely low frequency (ELF)	30 - 300 Hz	$10^4$ km - $10^3$ km	Communication with submarines

Voice frequency (VF)	300 - 3000 Hz	$10^3$ km - 100 km	Audio Application
Very low frequency (VLF)	3 - 30 kHz	100 km - 10 km	Submarine communication, avalanche detection, wireless heart rate monitors, geophysics
Low frequency (LF)	30 - 300 kHz	10 km - 1 km	Navigation, time signals, AM longwave broadcasting
Medium frequency (MF)	300 - 3000 kHz	1 km - 100 m	AM (Medium-wave) broadcasts
High frequency (HF)	3 - 30 MHz	100 m - 10 m	Shortwave broadcasts, amateur radio and over-the-horizon aviation communications
Very high frequency (VHF)	30 - 300 MHz	10 m - 1 m	FM television broadcasts and line-of-sight and ground-to-aircraft and aircraft-to-aircraft communications
Ultra high frequency (UHF)	300 - 3000 MHz	1 m - 100 mm	Television broadcasts, mobile phones, wireless LAN, Bluetooth and two-way radios such as FRS and GMRS radios
Super high frequency (SHF)	3 - 30 GHz	100 mm - 10 mm	Microwave devices, wireless LAN, most modern radars

Extremely high frequency (EHF)	30 - 300 GHz	10 mm - 1 mm	Radio astronomy, high-speed microwave radio relay
--------------------------------	--------------	--------------	---

### 6.6 : Introduction to Modulation

**Q.28 What is base band communication ?** [SPRU : Dec-13, Marks 1]

- Ans. : • The original information signals are analog or digital, they are all referred to as "baseband signals".  
• In a communication system, the original information signals (baseband signals) may be transmitted over the medium. Putting the original signal directly into the medium is referred to as "baseband transmission". Or base-band communication.

- The common example is telephony, especially for the local calls. Here the voice signal, converted into electrical form, is placed on the wires and transmitted over some distance to the receiver.

**Q.29 What are the limitations of baseband communication ?** [SPRU : Dec-13, Marks 2]

- Ans. : • There are many instances when the baseband signals are incompatible for direct transmission over the medium.  
• For example, voice signals cannot travel longer distances in air, the signal gets attenuated rapidly.

- Hence for transmission of baseband signals by radio, modulation technique has to be used.

**Q.30 What is modulation ? What is demodulation ?** [SPRU : May-15, Marks 2]

- Ans. : • In electronic communication system, a high frequency signal called the carrier signal is used to transmit baseband signal to the destination.

- The process by which the baseband signal modifies the carrier signal is called **modulation**.

- At the receiving end, the baseband signal and carrier signal are separated from modulated signal by the process of **demodulation**.

**Q.31 Explain the need for modulation.**

**EG [SPPU : May-09,10,11,12, Dec-11,12,13,14, Marks 4]**

**Ans.:** Since baseband signals are incompatible for direct transmission over the medium. We have to use modulation technique for the communication of baseband signal. The advantages of using modulation technique are as given below :

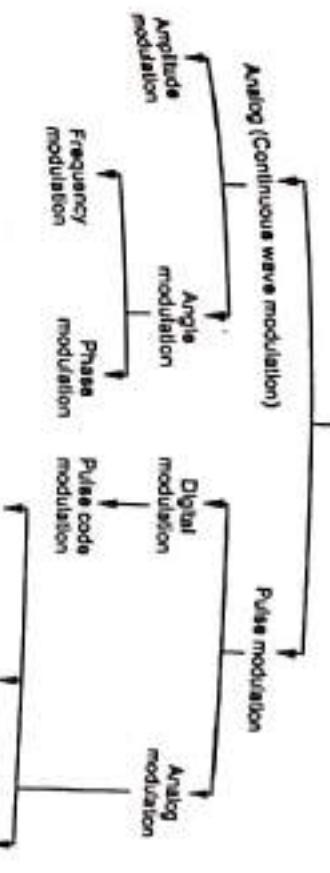
- Reduces the height of antenna
- Avoids mixing of signals
- Increases the range of communication
- Allows multiplexing of signals
- Allows adjustments in the bandwidth
- Improves quality of reception.

**Q.32 List the different types of modulation techniques.**

**EG [SPPU : Dec-12, Marks 3]**

**Ans.:** We may classify the modulation process into analog modulation and pulse modulation. In analog modulation, a sinusoidal wave is used as the carrier. When the amplitude of the carrier is varied in accordance with the baseband signal, we have amplitude modulation (AM), and when the angle of the carrier is varied, we have angle modulation.

• The angle modulation is further subdivided into frequency modulation (FM) and phase modulation (PM), in which the instantaneous frequency and phase of the carrier, respectively, are varied in accordance with the baseband signal.



**Fig. Q.32.1 Modulation techniques**

- In pulse modulation, the carrier consists of a periodic sequence of rectangular pulses. The pulse modulation is further subdivided into analog and digital type.
- In analog pulse modulation, the amplitude, duration or position of a pulse is varied in accordance with sample values of the baseband signal to have pulse amplitude modulation (PAM), pulse duration modulation (PDM) or pulse position modulation (PPM), respectively.

**Q.33 Explain AM technique in detail.**

**EG [SPPU : Dec-12, May-15, Marks 5]**

**Define amplitude modulation and draw waveform of AM wave.**

**EG [SPPU : May-09, Dec-12,13, Marks 2]**

**Ans.:** • Amplitude modulation (AM) is defined as system of modulation in which the instantaneous value of the carrier amplitude changes in accordance with the amplitude of the modulating signal.

- Fig. Q.33.1 shows a single frequency sine wave modulating a higher frequency carrier signal. Looking at Fig. Q.33.1 we can see that the frequency of the carrier signal remains constant during modulation process but its amplitude varies in accordance with the modulating signal.

frequency deviation occurs at the maximum amplitude of the modulating signal. Fig. Q.35.1 shows a single frequency sine wave modulating a higher frequency carrier signal with frequency modulation.

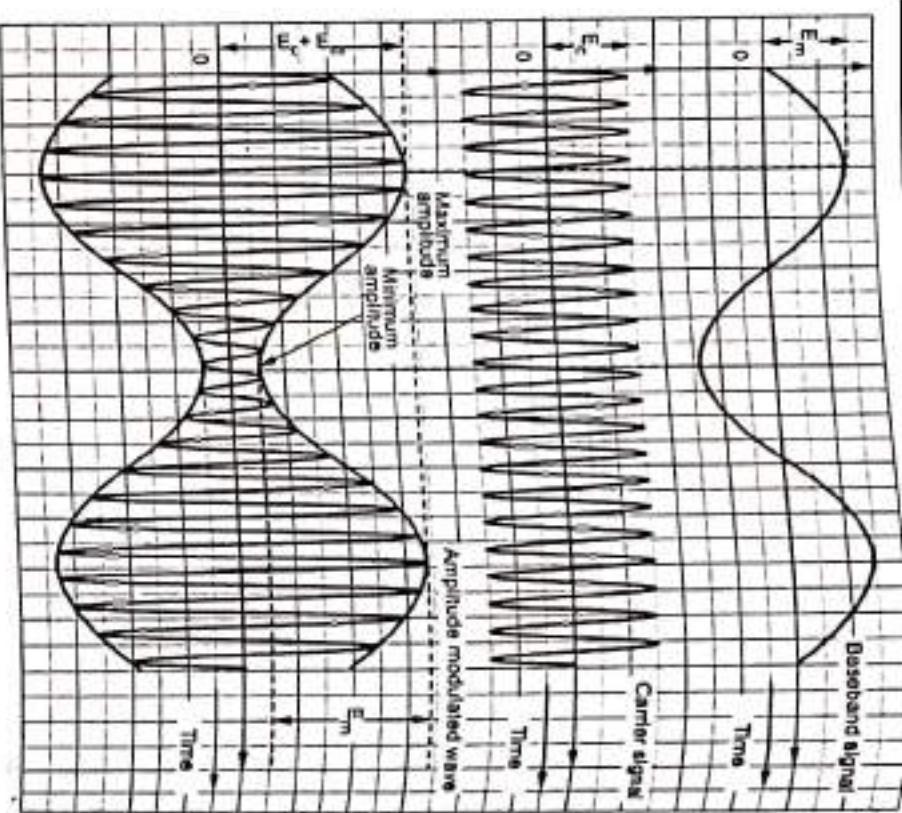


Fig. Q.33.1

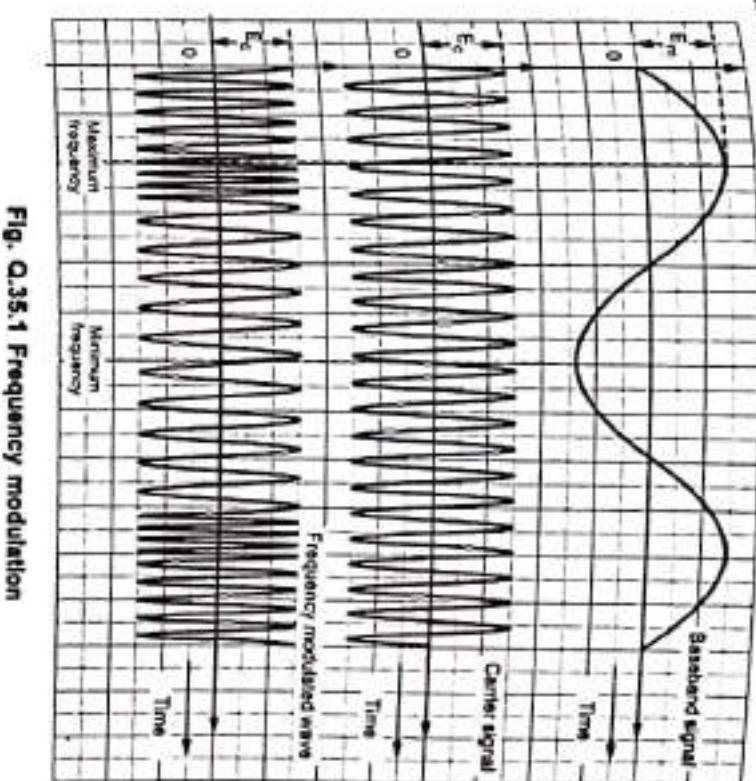


Fig. Q.35.1 Frequency modulation

### 6.7 : Block Diagram of AM Transmitter

**Q.34 Define frequency modulation.**

**Ans.:** When frequency of the carrier varies as per amplitude variations of modulating signal, then it is called Frequency Modulation (FM). Amplitude of the modulated carrier remains constant.

**Q.35 Define frequency deviation and sketch the FM wave.**

**ESE [SPRU : May-13, Dec-17, Marks 4]**

**Ans.:** The amount of change in carrier frequency produced by the modulating signal is known as frequency deviation. Maximum

**Q.36 With help of neat diagram explain high level AM transmitter.  
OR Explain low level AM transmitter.**

**ESE [SPRU : Dec-06, 08, 09, May-07, 08, 12]**

**Ans.:** • Fig. Q.36.1 shows the block diagram of an AM transmitter. Fig. Q.36.1 (a) shows AM transmitter with high level modulation and Fig. Q.36.1 (b) shows AM transmitter with low level modulation.

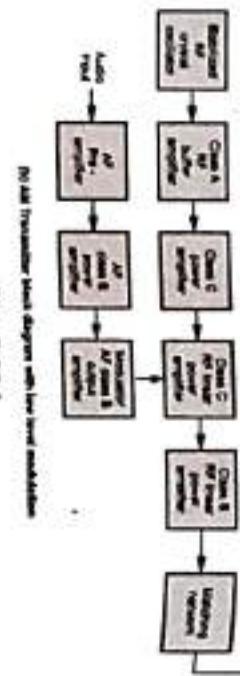
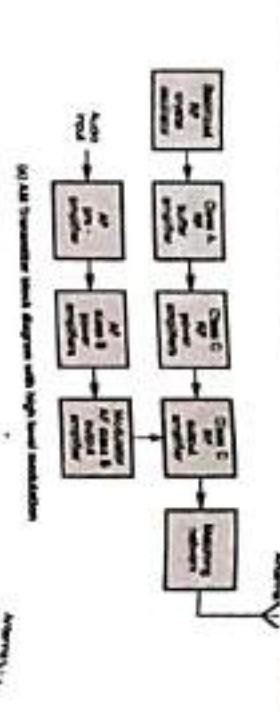


Fig. Q.36.1

- Looking at the Fig. Q.36.1 it can be seen that stable RF source, buffer amplifiers and subsequent RF power amplifiers are common for both, low level modulation transmitter and high level modulation transmitter.

- The stable RF source is provided by crystal oscillator with a carrier frequency or sub-multiple of it.

- The buffer amplifiers are usually class A amplifiers whereas power amplifiers are class C amplifiers. In both, audio and power audio frequency (AF) amplifiers are present.

- In fact, the only difference is the point at which the modulation takes place.

- In case of low level modulation, modulation takes place at low power level, i.e. before the final output amplifier.

- In low level modulation system, amplifier efficiency and bandwidth preservation are important factors since audio signal is having low power. This is especially used for laboratory purpose.

- While for high level modulation other than efficiency of power handling capability, distortion, capability of handling amplitude variations are important parameter.
- The output of final amplifier is passed through an impedance matching network that includes the tank circuit of the final amplifier.
- For tank circuits Q is kept low enough to pass all sideband signals without amplitude and frequency distortion, but at the same time provide sufficient attenuation at the second harmonic of the carrier frequency.

### 6.8 : Block Diagram of AM Receiver

- Q.37 Draw and explain the block diagram of superheterodyne receiver.

IEE [SPNU : Dec-93, 04, 09, 11, May-01, 05, 06]

Ans. : • Fig. Q.37.1 shows the block diagram of AM receiver with a superheterodyne technique. As shown in Fig. Q.37.1 antenna pick up the weak radio signal and feeds it to the RF amplifier. The RF amplifier provides some initial gain and selectivity.

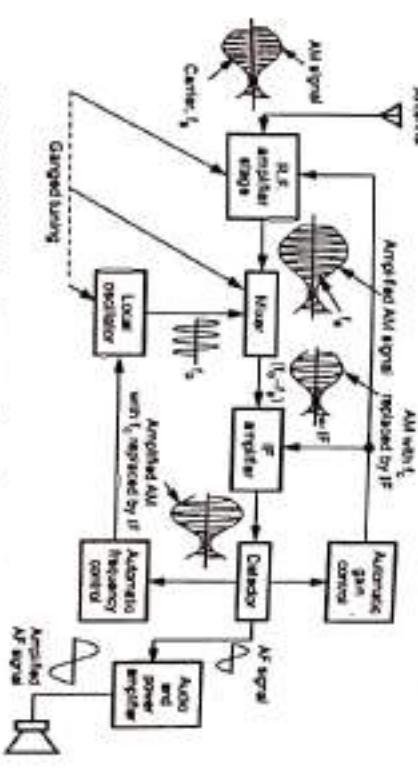


Fig. Q.37.1 Block diagram of superheterodyne receiver

- The output of the RF amplifier is applied to the input of the mixer. The mixer also receives an input from local oscillator.

- The output of the mixer circuit is difference frequency ( $f_o - f_i$ ) commonly known as IF (Intermediate Frequency). The signal at this intermediate frequency contains the same modulation as the original carrier.
- This signal is amplified by one or more IF amplifier stages and most of the receiver gain is obtained in these IF stages.
- The highly amplified IF signal is applied to detector circuits to recover the original modulating information.
- Finally, the output of detector circuit is fed to audio and power amplifier which provides a sufficient gain to operate a speaker.
- Another important circuit in the superheterodyne receiver are AGC and AFC circuit.

- AGC is used to maintain a constant output voltage level over a wide range of RF input signal levels.

- It derives the d.c. bias voltage from the output of detector which is proportional to the amplitude of the received signal. This d.c. bias voltage is feedback to the IF amplifiers and sometimes to the RF amplifier, to control the gain of the receiver. As a result, it provides a constant output voltage level over a wide range of RF input signal levels.
- AFC circuit generates AFC signal which is used to adjust and stabilize the frequency of the local oscillator.

### 6.9 : Block Diagram of FM Transmitter

**Q.38 Explain with block diagram the Armstrong method of FM generation.**

[SPM : Dec-98,99,01,05,06,07,09,10,11, May-2000,04,05, Marks 10]

**Ans. :** • FM generation using Armstrong method is achieved by performing following steps :

1. Generation of PM wave
2. Generation of NBFM from PM wave
3. Generation of WBFM from NBFM

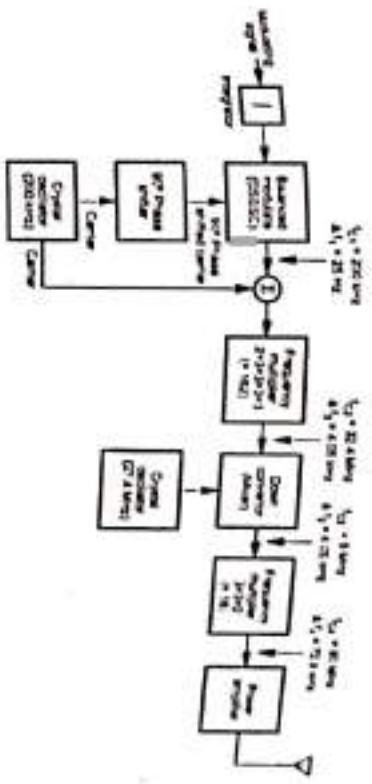


Fig. Q.38.1 shows block diagram of FM generation using Armstrong method.

- As shown in the Fig. Q.38.1 crystal oscillator is used to generate a stable unmodulated carrier which is applied to the 90° phase shifter and the summing circuit.
- The 90° phase shifted carrier is applied to the balanced modulator along with the modulating signal.
- Thus 90° phase shifted carrier is DSBSC modulated in the balanced modulator giving us only two sidebands with their resultant in phase with the 90° shifted carrier.
- The two sidebands and the unshifted carrier are applied to a summing circuit to get the resultant of vector addition of the carrier and two sidebands.

### Generating NBFM from PM

- In PM along with the phase variation, some frequency variation also takes place. Higher modulating voltages produce greater phase shift which results greater frequency deviation. And higher modulating frequencies produce a faster rate of change of modulating voltage hence they also result greater frequency deviation.

- Thus, in PM the carrier frequency deviation is proportional to
  - Modulating voltage and
  - Modulating Frequency

- However, in FM the frequency deviation is only proportional to the modulating voltage regardless of its frequency.

- Thus, to suppress high frequency modulating signals and to make frequency deviation independent of modulating frequency the modulating signal is passed through a low pass RC filter (Integrator) as shown in Fig. Q.38.2.



Fig. Q.38.2

- As a result, the high frequency modulating signals are attenuated but there is no change in the amplitudes of low frequency modulating signals.
- The output of integrator is then applied to the phase modulator.
- With this input the frequency deviation at the output of the phase modulator will be effectively proportional only to the modulating voltage and hence we obtain FM wave at the output of phase modulator.
- The NBFM is converted to WBFM by using frequency multipliers.

### 6.10 : Block Diagram of FM Receiver

**Q.39 Draw and explain superheterodyne FM receiver.**

**SAT (SPRU : May-05,12,13, Dec-10,11, Maha 6)**

**Ans. :** • The block diagram of typical F.M. receiver is shown in the Fig. Q.39.1.

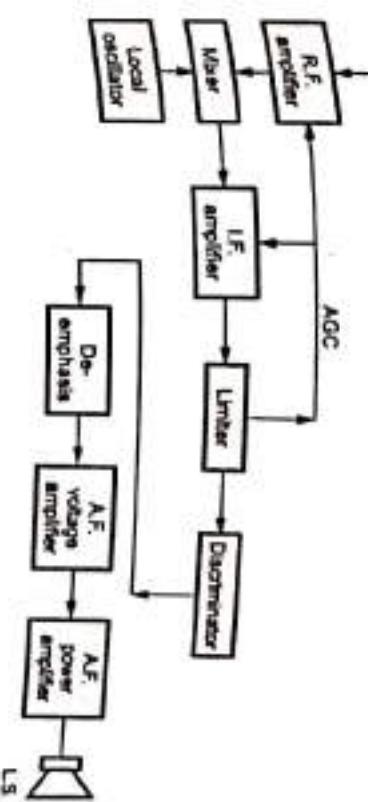


Fig. Q.39.1 Block diagram of F.M. receiver

- **R.F. Amplifier Stage :** Since F.M. signal has a larger bandwidth it is likely to encounter more noise. Hence to reduce the noise figure of the receiver, an RF amplifier stage is used. The RF amplifier stage matches the antenna to the receiver.
- **Mixer Stage :** With the help of local oscillator, this stage down converts the incoming carrier frequency to L.F., which is 10.7 MHz for F.M. receiver.
- **L.F. Amplifier Stage :** In the L.F. amplifier stages, the most of the gain of receiver is developed.
- **Limiter Stage :** To remove the amplitude variations of the signal is the main function of the limiter. At the output of the limiter stage, we get a constant amplitude signal, even though the amplitude of input signal may be varying.
- **FM Demodulators :** FM demodulators, change the frequency deviation of the incoming carrier into an AF amplitude variation (identical to the one that originally caused the frequency variation).

### 6.11 : Mobile Communication System

#### Q.40 What is mobile communication ?

Ans. : • Mobile communication refers to the conversation established between two users at two different places with their hand held equipment.

- Initially the focus of mobile communication was towards voice but later it also dealt with data. Today cellular phones provide many services. That include electronic mail, internet access, short message service, electronic address book, games, calculator. Further research is in progress to attract people towards commercial product.

#### Q.41 Explain the concept of cellular system.

ES [SPU : Dec-11, May-12, 19, Marks 4]

Ans. : • The basic concept behind the cellular/mobile system is that rather than serving a given geographical area within a single transmitter and receiver, the system divides the service area into many small areas known as **cells**.

- A cellular mobile communications system uses a large number of low-power wireless transmitters to create cells.
- Each cell is served by at least one fixed-location transceiver, known as a **cell site** or **base station**.
- Each mobile uses a separate, temporary radio channel to talk to the base station. The base station talks to many mobiles at once, using one channel per mobile. Channels use a pair of frequencies for communication—one frequency, the **forward link**, for transmitting from the base station, and one frequency, the **reverse link**, for the base station to receive calls from the users.
- Variable power levels allow cells to be sized according to the subscriber density and demand within a particular region.
- The typical cell covers only several square kilometers and contains its own receiver and low-power transmitter. As shown in the Fig. Q.41.1, the cells are hexagons with the repeater and base station at the center.

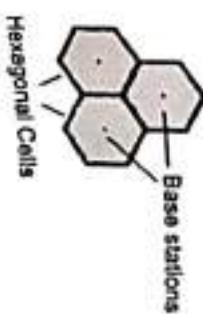


Fig. Q.41.1 Cells

- Clusters** : Cells are arranged in clusters. A cluster is a group of cells. No channels are reused within the cluster.

- Cluster Size** : Only certain cluster sizes are possible, principally due to geometry of a hexagon and the allowable cluster sizes of 3, 4, 7 and 12. Fig. Q.41.2 shows the cluster of size 7.

- Frequency Reuse** : In a cellular network, each cell uses a different set of frequencies from neighboring cells, to avoid interference and provide guaranteed bandwidth within each cell. The coverage area of cells are called the **footprint**. This footprint is limited by a boundary so that the same group of channels can be used in different cells that are far enough away from each other so that their frequencies do not interfere.
- When joined together these cells provide radio coverage over a wide geographic area. This enables a large number of portable transceivers (e.g., mobile phones, pagers, etc.) to communicate with each other and with fixed transceivers and telephones anywhere in the network, via base stations, even if some of the transceivers are moving through more than one cell during transmission.

#### Q.42 Explain the basic structure of mobile phone system.

ES [SPU : May-15, 18, Marks 4]

- Ans. : • Fig. Q.42.1 shows the basic structure of mobile/cellular phone system. The cellular communications system consists of the following major components that work together to provide mobile service to subscribers :

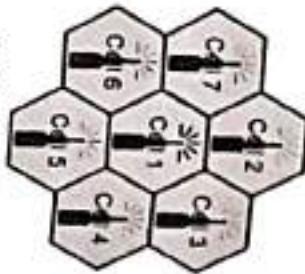
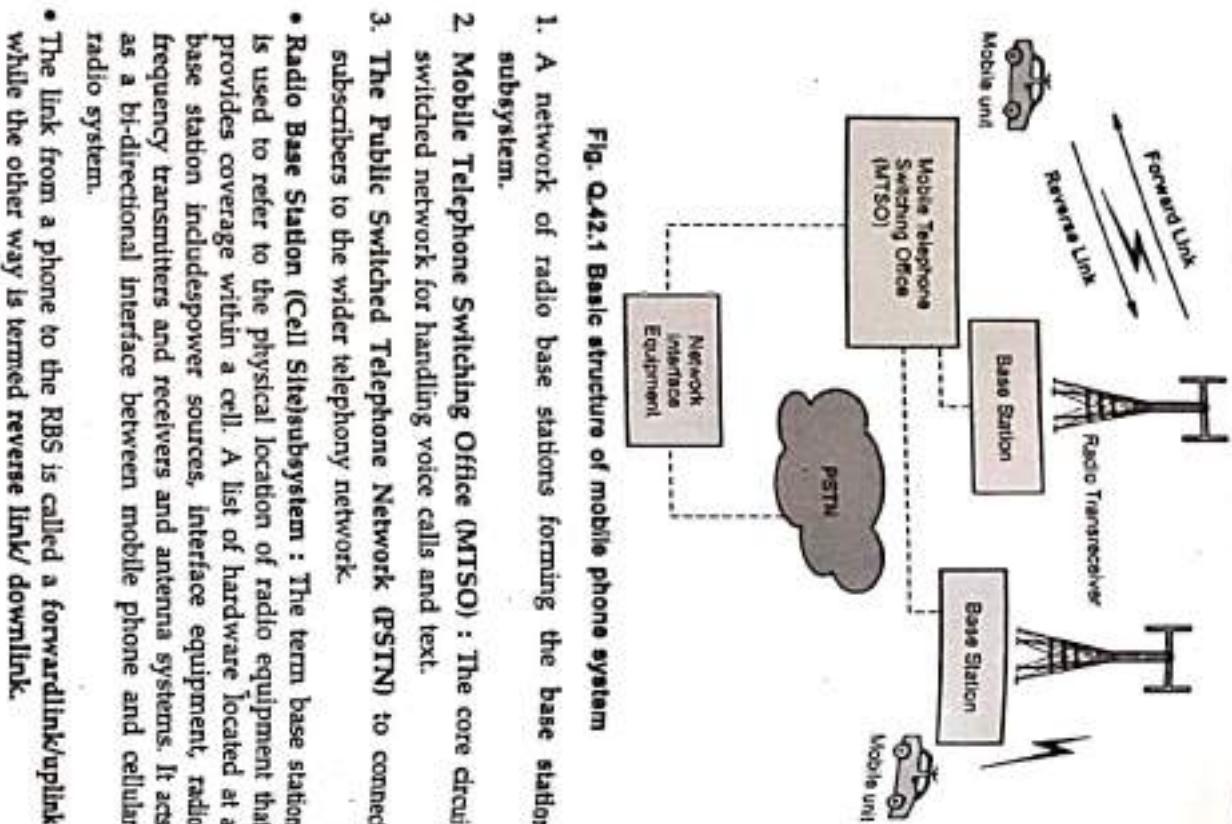


Fig. Q.41.2 Cluster



**Fig. Q.42.1 Basic structure of mobile phone system**

1. A network of radio base stations forming the base station subsystem.
2. Mobile Telephone Switching Office (MTSO) : The core circuit switched network for handling voice calls and text.
3. The Public Telephone Network (PSTN) to connect subscribers to the wider telephony network.
4. Radio Base Station (Cell Site) subsystem : The term 'base station' is used to refer to the physical location of radio equipment that provides coverage within a cell. A list of hardware located at a base station includes power sources, interface equipment, radio frequency transmitters and receivers and antenna systems. It acts as a bi-directional interface between mobile phone and cellular radio system.
- The link from a phone to the RBS is called a **forward link/uplink** while the other way is termed **reverse link/downlink**.

\* In analog cellular networks, the MSC controls the system operations such as calls, tracks billing information, and locates cellular subscribers.

#### Q.43 What is GSM system?

Ans. : • GSM (Group of Special Mobile) system is a second generation (2 G) cellular system developed in Europe. It uses digital modulation and network level architectures and services. Commercial services of GSM was started in mid-1991.

- GSM can handle both voice and data traffic, the voice waveform being digitally encoded before transmission. GSM transmission is done within frequency bands of 900 MHz, 1800 MHz and 1900 MHz.

- GSM provides subscribers with high-quality digital wireless phone service and clarity, as well as enhanced call security and privacy.

#### Q.44 Draw and explain the block diagram of GSM.

Ans. : The Fig. Q.44.1 shows the block diagram of GSM system. It is divided into four parts :

1. Mobile station - Carried by subscriber
2. Base station system - Controls the radio link with mobile station
3. Network system - Performs switching of calls between mobile users.
4. Operation and support subsystem. (OSS)

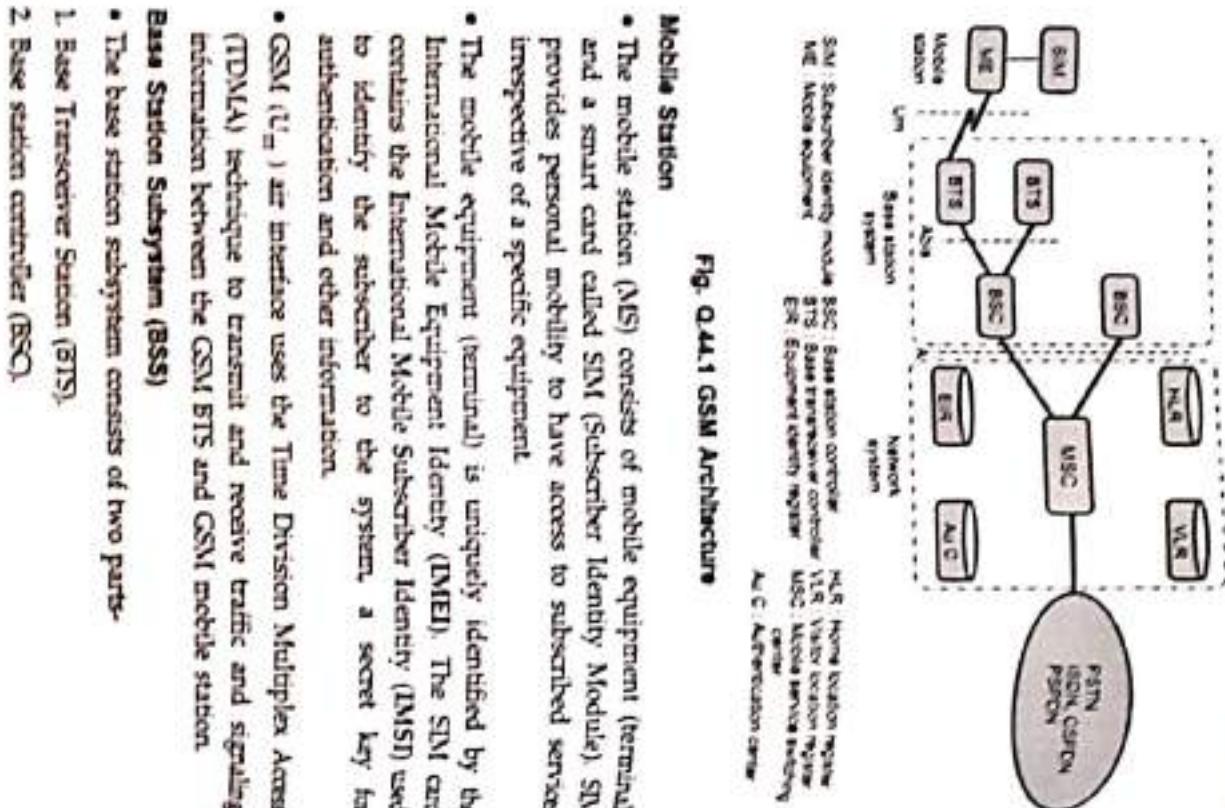


Fig. Q4.1 GSM Architecture

**Mobile Station**

- The mobile station (MS) consists of mobile equipment (terminal) and a smart card called SIM (Subscriber Identity Module). SIM provides personal mobility to have access to subscribed services irrespective of a specific equipment.
- The mobile equipment (terminal) is uniquely identified by the International Mobile Equipment Identity (IMEI). The SIM card contains the International Mobile Subscriber Identity (IMSI) used to identify the subscriber to the system, a secret key for authentication and other information.
- GSM ( $\text{U}_{\text{m}}$ ) air interface uses the Time Division Multiplex Access (TDMA) technique to transmit and receive traffic and signaling information between the GSM BTS and GSM mobile station.

- The base station subsystem consists of two parts-
  1. Base Transceiver Station (BTS).
  2. Base station controller (BSC).

**Network Substation**

- The central component of network subsystem is the Mobile Services Switching Center (MSC). It acts as switching node of PSTN and provides the function needed to handle a mobile subscriber such as - registration, authentication, locating updating handovers and call routing to roaming subscriber.
- Network subsystem includes data bases required for subscribers and mobility management. The Network subsystem also includes four different data bases -
  1. Home Location Register (HLR)
  2. Visitor Location Register (VLR)
  3. Equipment Identity Register (EIR)
  4. Authentication Center (AuC)
- The Home Location Register (HLR) and Visitor Location Register (VLR), together with MSC provide the call routing and roaming capabilities of GSM.
- The Equipment Identity Register (EIR) is a database that contains a list of all valid mobile equipment on the network, where each mobile station is identified by its International Mobile Equipment Identity (IMEI).

- The Authentication Center (AuC) is a protected database that stores a copy of the secret key stored in each subscriber's SIM card, which is used for authentication and encryption over the radio channel.
- The AuC contains security modules for authentication keys ( $K_A$ ), authentication algorithms ( $A_A$ ) and cipher key generation algorithms ( $A_g$ ).
- The operations and support subsystem (OSS) is the command center used to monitor and control the GSM system.

END...  
E

## QUESTION BANK FOR END SEM EXAM

### Unit - III

- Explain various number systems. (Refer section 3.1)
- Name the number system used in computers. (Refer section 3.1)
- What are 1's complement and 2's complement numbers ? (Refer Q.17 and Q.18 of Chapter 3)
- State the procedure to perform binary subtraction using 1's complement method. (Refer Q.24 of Chapter 3)
- State the different ways for representing the signed binary numbers. (Refer Q.16 of Chapter 3)
- What is BCD code ? State its advantages and disadvantages. (Refer Q.31 of Chapter 3)
- State and prove DeMorgan's theorem. (Refer Q.32 of Chapter 3)
- Write the logic symbol, expression and truth table for the following logic gates :
  - i) NOT      ii) AND
  - iii) OR      iv) EX-NOR
  - v) NAND      vi) NOR      vii) EX-OR (Refer section 3.7)
- Draw the symbol for OR gate and write its truth table. (Refer section 3.7)

- Q.10** Draw and explain the circuit diagram of AND, OR and NOT gates with suitable truth tables. (Refer section 3.7)
- Q.11** Write the truth table of an exclusive-OR gate. (Refer section 3.7)
- Q.12** What is meant by universal gates ? (Refer Q.42 of Chapter 3)
- Q.13** Why NAND and NOR gates are called universal gates ? (Refer Q.42 of Chapter 3)
- Q.14** Derive basic gates from NAND gates. (Refer Q.42 of Chapter 3)
- Q.15** Derive basic gates from NOR gates. (Refer Q.42 of Chapter 3)
- Q.16** What is the difference between half adder and full adder. (Refer Q.47 of Chapter 3)
- Q.17** Implement half adder using gates, truth table and give equations for sum and carry. (Refer Q.48 of Chapter 3)
- Q.18** Implement full adder using basic gates along with its truth table and write the equations for sum and carry. (Refer Q.50 of Chapter 3)
- Q.19** What is flip-flop ? (Refer Q.54 of Chapter 3)
- Q.20** Draw and explain the working of SR flip-flop. (Refer Q.56 of Chapter 3)

- Q.21** Draw and explain the operation of D-flip-flop. (Refer Q.57 of Chapter 3)
- Q.22** Explain the operation of JK flip-flop. (Refer Q.58 of Chapter 3)
- Q.23** What is race around condition ? Explain in brief. (Refer Q.59 of Chapter 3)
- Q.24** Draw and explain the operation of T flip-flop. (Refer Q.60 of Chapter 3)
- Q.25** State various applications of flip-flops. (Refer Q.61 of Chapter 3)
- Q.26** Draw and explain the block diagram of microprocessor. (Refer Q.62 of Chapter 3)
- Q.27** Draw and explain the block diagram of a microcontroller. (Refer Q.63 of Chapter 3)
- Q.28** Give the comparison between microprocessor and microcontroller. (Refer Q.64 of Chapter 3)
- Q.29** State the advantages of microprocessor and microcontroller. (Refer Q.65 of Chapter 3)
- Q.30** Give the applications of microprocessor and microcontroller. (Refer Q.66 of Chapter 3)

**Unit - IV**

- Q.1** With the help of block diagram explain how digital multimeter is used to measure the various quantities. (Refer Q.1 of Chapter 4)

- Q.2** Write the important specifications of digital multimeter. (Refer Q.2 of Chapter 4)
- Q.3** Draw the block diagram of function generator and explain the function of each block. (Refer Q.3 of Chapter 4)
- Q.4** State the applications of function generator. (Refer Q.4 of Chapter 4)
- Q.5** Draw the block diagram of digital storage oscilloscope and explain function of each block. (Refer Q.5 of Chapter 4)
- Q.6** State the various applications of DSO. (Refer Q.6 of Chapter 4)
- Q.7** State the advantages of DSO. (Refer Q.7 of Chapter 4)
- Q.8** Draw the block diagram of powerscope and explain. (Refer Q.8 of Chapter 4)
- Q.9** Draw the block diagram of a.c. to d.c. power supply. (Refer Q.9 of Chapter 4)
- Q.10** What is autotransformer ? Explain its working. (Refer Q.10 of Chapter 4)
- Q.11** Explain the applications of an autotransformer. (Refer Q.11 of Chapter 4)
- Q.12** Draw the basic analog ammeter circuit ? How shunt resistance is calculated ? (Refer Q.12 of Chapter 4)
- Q.13** Draw the basic analog voltmeter circuit ? How multiplier resistance is calculated ? (Refer Q.13 of Chapter 4)

**Unit - V**

- Q.1** Draw the block diagram of instrumentation system and state the function of each block. (Refer Q.1 of Chapter 5)
- Q.2** Define sensor, transducer and actuator. (Refer Q.2 of Chapter 5)
- Q.3** Give the classification of sensors. (Refer Q.3 of Chapter 5)
- Q.4** Give the comparison between active and passive sensors. (Refer Q.4 of Chapter 5)
- Q.5** Write short note on selection criteria for sensors. (Refer Q.5 of Chapter 5)
- Q.6** Write a note on analog sensors. (Refer Q.6 of Chapter 5)
- Q.7** Explain the operation of digital sensor with the help of example. (Refer Q.7 of Chapter 5)
- Q.8** Give comparison between analog and digital sensor. (Refer Q.8 of Chapter 5)
- Q.9** What is LVDT ? (Refer Q.9 of Chapter 5)
- Q.10** Explain the construction and principle of operation of LVDT. (Refer Q.10 of Chapter 5)
- Q.11** State the advantages of LVDT. (Refer Q.11 of Chapter 5)
- Q.12** State the disadvantages of LVDT. (Refer Q.12 of Chapter 5)
- Q.13** State the applications of LVDT. (Refer Q.13 of Chapter 5)
- Q.14** What is an accelerometer ? (Refer Q.14 of Chapter 5)

- Q.15** Explain working of piezoelectric accelerometer.  
(Refer Q.15 of Chapter 5)
- Q.16** Give important specifications of accelerometer.  
(Refer Q.16 of Chapter 5)
- Q.17** State the applications of accelerometer.  
(Refer Q.17 of Chapter 5)
- Q.18** What is thermocouple ? (Refer Q.18 of Chapter 5)
- Q.19** What is Seebeck effect ? (Refer Q.19 of Chapter 5)
- Q.20** Explain the principle of operation and construction of thermocouple. (Refer Q.20 of Chapter 5)
- Q.21** Mention the materials used for thermocouples.  
(Refer Q.21 of Chapter 5)
- Q.22** State the advantages of thermocouple.  
(Refer Q.22 of Chapter 5)
- Q.23** State the limitations of thermocouple.  
(Refer Q.23 of Chapter 5)
- Q.24** State the applications of thermocouple.  
(Refer Q.24 of Chapter 5)
- Q.25** What is thermistor ? (Refer Q.25 of Chapter 5)
- Q.26** Explain the operating principle of thermistor.  
(Refer Q.26 of Chapter 5)
- Q.27** State the materials used in a thermistor and explain the construction of it. (Refer Q.27 of Chapter 5)

- Q.28** State the advantages of thermistor.  
(Refer Q.28 of Chapter 5)
- Q.29** State the limitations of thermistors.  
(Refer Q.29 of Chapter 5)
- Q.30** State the applications of thermistor.  
(Refer Q.30 of Chapter 5)
- Q.31** What is RTD ? (Refer Q.31 of Chapter 5)
- Q.32** Explain the principle of operation of RTD.  
(Refer Q.32 of Chapter 5)
- Q.33** Compare three types of temperature transducers or compare RTD with thermistors. (Refer Q.33 of Chapter 5)
- Q.34** Write a short note on semiconductor gas sensor.  
(Refer Q.34 of Chapter 5)
- Q.35** Write a note on LDR. (Refer Q.35 of Chapter 5)
- Q.36** List the features of LDR. (Refer Q.36 of Chapter 5)
- Q.37** State the applications of LDR. (Refer Q.37 of Chapter 5)
- Q.38** Discuss any one application of LDR.  
(Refer Q.38 of Chapter 5)
- Q.39** What is strain gauge ? (Refer Q.39 of Chapter 5)
- Q.40** Explain the working principle of strain gauge.  
(Refer Q.40 of Chapter 5)
- Q.41** Define strain gauge of factor. (Refer Q.41 of Chapter 5)

- Q.42** Give the classification of resistance wire strain gauges. (Refer Q.42 of Chapter 5)
- Q.43** Explain the unbonded strain gauge with the help of suitable diagram. (Refer Q.43 of Chapter 5)
- Q.44** What is fine wire strain gauge? (Refer Q.44 of Chapter 5)
- Q.45** What is metal foil strain gauge? (Refer Q.45 of Chapter 5)
- Q.46** State the advantages of metal foil type strain gauge. (Refer Q.46 of Chapter 5)
- Q.47** Write a note on semiconductor strain gauge. (Refer Q.47 of Chapter 5)
- Q.48** State advantages and disadvantages of semiconductor strain gauges. (Refer Q.48 of Chapter 5)
- Q.49** Give the comparison between semiconductor and metal strain gauges. (Refer Q.49 of Chapter 5)
- Q.50** Write a note on Rosette strain gauges. (Refer Q.50 of Chapter 5)
- Q.51** What is load cell? (Refer Q.51 of Chapter 5)
- Q.52** Explain the construction and operating principle of load cell. (Refer Q.52 of Chapter 5)
- Q.53** State the main types of load cell. (Refer Q.53 of Chapter 5)
- Q.54** State advantages and disadvantages of load cell. (Refer Q.54 of Chapter 5)
- Q.55** State the applications of load cell. (Refer Q.55 of Chapter 5)

- Q.61** What is pressure sensor? (Refer Q.56 of Chapter 5)
- Q.62** What are the types of pressure sensor? (Refer Q.57 of Chapter 5)
- Q.63** Explain the working of strain gauge pressure sensor. (Refer Q.58 of Chapter 5)
- Q.64** Explain the working of capacitive pressure sensor. (Refer Q.59 of Chapter 5)
- Q.65** Write a note on piezoelectric pressure sensor. (Refer Q.60 of Chapter 5)
- Q.66** What is a Biosensor? (Refer Q.61 of Chapter 5)
- Q.67** Explain the construction of biosensor. (Refer Q.62 of Chapter 5)
- Q.68** Explain the working of biosensor with the help of neat block diagram. (Refer Q.63 of Chapter 5)
- Q.69** List the types of biosensor. (Refer Q.64 of Chapter 5)
- Q.70** List the characteristics of biosensor. (Refer Q.65 of Chapter 5)
- Q.71** State the applications of biosensors. (Refer Q.66 of Chapter 5)
- Q.72** Write a note on blood glucose biosensor. (Refer Q.67 of Chapter 5)

### Unit - VI

- Q.1** State the importance of communication system. (Refer Q.1 of Chapter 6)

- Q.2** Explain the elements of communication system with the help of block diagram. (Refer Q.2 of Chapter 6)
- Q.3** Explain various modes of transmission. (Refer Q.3 of Chapter 6)
- Q.4** Give comparison between various modes of transmission. (Refer Q.4 of Chapter 6)
- Q.5** What is wireless and wireline communication ? (Refer Q.5 of Chapter 6)
- Q.6** State the types of wired media of transmission. (Refer Q.6 of Chapter 6)
- Q.7** Write a note on twisted pair cables. (Refer Q.7 of Chapter 6)
- Q.8** State the advantages of twisted pair. (Refer Q.8 of Chapter 6)
- Q.9** State the disadvantages of twisted pair. (Refer Q.9 of Chapter 6)
- Q.10** State the applications of twisted pair cables. (Refer Q.10 of Chapter 6)
- Q.11** Write a note on coaxial cable. (Refer Q.11 of Chapter 6)
- Q.12** State the advantages of coaxial cable. (Refer Q.12 of Chapter 6)
- Q.13** State the disadvantages of coaxial cable. (Refer Q.13 of Chapter 6)
- Q.14** State applications of coaxial cables. (Refer Q.14 of Chapter 6)

- Q.15** Write a short note on fiber optic cable. (Refer Q.15 of Chapter 6)
- Q.16** Explain how light travels through a fiber. (Refer Q.16 of Chapter 6)
- Q.17** List the benefits of fiber optic cables. (Refer Q.17 of Chapter 6)
- Q.18** State the disadvantages of optic fiber cables. (Refer Q.18 of Chapter 6)
- Q.19** State the applications of fiber optic cables. (Refer Q.19 of Chapter 6)
- Q.20** Give the comparison between twisted pair, co-axial cable and fiber optic cable. (Refer Q.20 of Chapter 6)
- Q.21** What is wireless transmission media ? (Refer Q.21 of Chapter 6)
- Q.22** Compare the advantages and disadvantages of wireless media. (Refer Q.22 of Chapter 6)
- Q.23** Compare wired and wireless media. (Refer Q.23 of Chapter 6)
- Q.24** Draw and explain electromagnetic spectrum ? (Refer Q.24 of Chapter 6)
- Q.25** Define frequency and wavelength. Also state the relation between them. (Refer Q.25 of Chapter 6)
- Q.26** What is RF ? (Refer Q.26 of Chapter 6)

- Q.27** Describes the radio frequency spectrum and its applications according to various frequency bands. (Refer Q.27 of Chapter 6)
- Q.28** What is base band communication ? (Refer Q.28 of Chapter 6)
- Q.29** What are the limitations of baseband communication ? (Refer Q.29 of Chapter 6)
- Q.30** What is modulation ? What is demodulation ? (Refer Q.30 of Chapter 6)
- Q.31** Explain the need for modulation. (Refer Q.31 of Chapter 6)
- Q.32** List the different types of modulation techniques. (Refer Q.32 of Chapter 6)
- Q.33** Explain AM technique in detail. (Refer Q.33 of Chapter 6)
- Q.34** Define frequency modulation. (Refer Q.34 of Chapter 6)
- Q.35** Define frequency deviation and sketch the FM wave. (Refer Q.35 of Chapter 6)
- Q.36** With help of neat diagram explain high level AM transmitter. (Refer Q.36 of Chapter 6)
- Q.37** Draw and explain the block diagram of superheterodyne receiver. (Refer Q.37 of Chapter 6)
- Q.38** Explain with block diagram the Armstrong method of FM generation. (Refer Q.38 of Chapter 6)
- Q.39** Draw and explain superheterodyne FM receiver. (Refer Q.39 of Chapter 6)

- Q.40** What is mobile communication ? (Refer Q.40 of Chapter 6)
- Q.41** Explain the concept of cellular system. (Refer Q.41 of Chapter 6)
- Q.42** Explain the basic structure of mobile phone system. (Refer Q.42 of Chapter 6)
- Q.43** What is GSM system ? (Refer Q.43 of Chapter 6)
- Q.44** Draw and explain the block diagram of GSM. (Refer Q.44 of Chapter 6)

**END... ↗**

