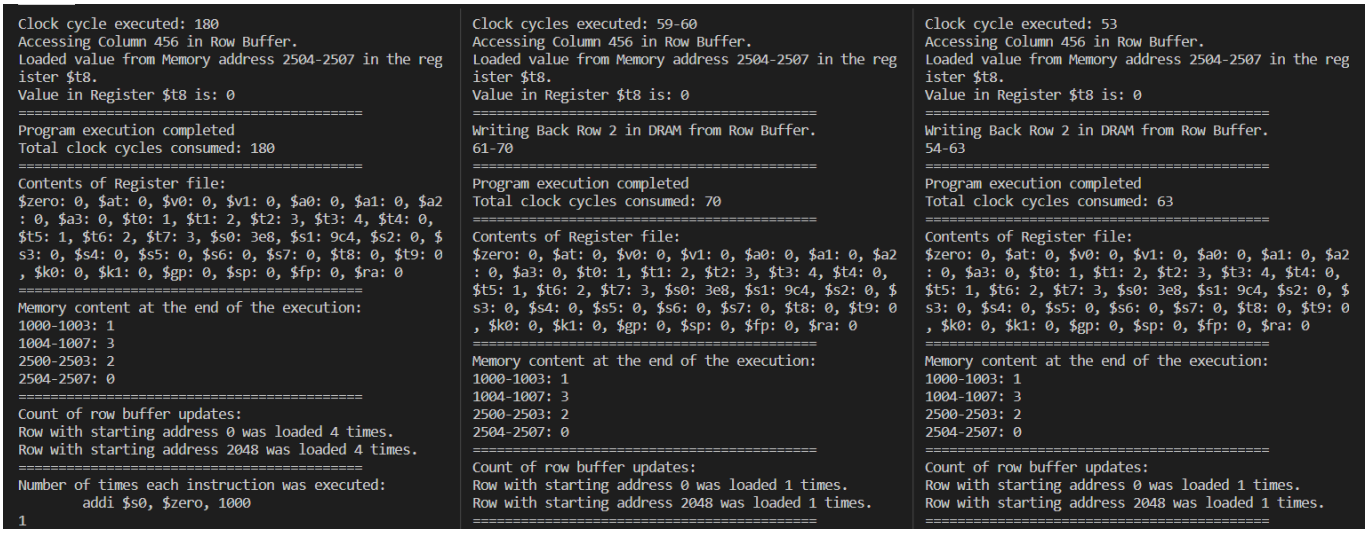
Testing:

Strategy:

1. Drastic reduction in cycles. Contrasting with without optimization (lefyt) (180+10), DRAM reordering (middle) (70), DRAM reordering with Non blocking access (right) (63)

```
main:
    addi $s0, $zero, 1000
    addi $s1, $zero, 2500
    addi $t0, $zero, 1
    addi $t1, $zero, 2
    addi $t2, $zero, 3
    addi $t3, $zero, 4
    sw $t0, 0($s0)
    sw $t1, 0($s1)
    sw $t2, 4($s0)
    sw $t4, 4($s1)
    lw $t5, 0($s0)
    lw $t6, 0($s1)
    lw $t7, 4($s0)
    lw $t8, 4($s1)
```



2. Reordering with NBA impact 63+10, 73, 71

```
addi $t0, $t0, 5000
addi $t1, $t1, 10000
addi $t2, $t2, 1000
lw $s0, 0 ($t2)
lw $s1, 0 ($t0)
lw $s2, 7500 ($s1)
add $s2, $s2, $s5
```

```
=========
Clock cycle executed: 62
Accessing Column 828 in Row Buffer.
Loaded value from Memory address 29500-29503 in the r
egister $s2.
Value in Register $s2 is: 22000
================================================
=========
Clock cycle executed: 63
Current Instructiion being executed: add $s2, $s2, $s
5
Updated value of $s2 to 22000.
========================================
Program execution completed
Total clock cycles consumed: 63
========================================
Contents of Register file:
$zero: 0, $at: 0, $v0: 0, $v1: 0, $a0: 0, $a1: 0, $a2
: 0, $a3: 0, $t0: 1388, $t1: 2710, $t2: 3e8, $t3: 0,
$t4: 0, $t5: 0, $t6: 0, $t7: 0, $s0: 55f0, $s1: 55f0,
 $s2: 55f0, $s3: 0, $s4: 0, $s5: 0, $s6: 0, $s7: 0, $
t8: 0, $t9: 0, $k0: 0, $k1: 0, $gp: 0, $sp: 0, $fp: 0
, $ra: 0
========================================
Memory content at the end of the execution:
========================================
Count of row buffer updates:
Row with starting address 0 was loaded 1 times.
Row with starting address 4096 was loaded 1 times.
Row with starting address 28672 was loaded 1 times.
========================================
```

```
Accessing Column 332 in Row Buffer.
Loaded value from Memory address 7500-7503 in the reg
ister $s2.
Value in Register $s2 is: 0
================================================
=========
Clock cycle executed: 63
Current Instructiion being executed: add $s2, $s2, $s
5
Updated value of $s2 to 0.
========================================
Writing Back Row 7 in DRAM from Row Buffer.
64-73
========================================
Program execution completed
Total clock cycles consumed: 73
========================================
Contents of Register file:
$zero: 0, $at: 0, $v0: 0, $v1: 0, $a0: 0, $a1: 0, $a2
: 0, $a3: 0, $t0: 1388, $t1: 2710, $t2: 3e8, $t3: 0,
$t4: 0, $t5: 0, $t6: 0, $t7: 0, $s0: 0, $s1: 0, $s2:
0, $s3: 0, $s4: 0, $s5: 0, $s6: 0, $s7: 0, $t8: 0, $t
9: 0, $k0: 0, $k1: 0, $gp: 0, $sp: 0, $fp: 0, $ra: 0
========================================
Memory content at the end of the execution:
========================================
Count of row buffer updates:
Row with starting address 0 was loaded 1 times.
Row with starting address 4096 was loaded 1 times.
Row with starting address 7168 was loaded 1 times.
========================================
```

```
Clock cycle executed: 60
Accessing Column 332 in Row Buffer.
Loaded value from Memory address 7500-7503 in the reg
ister $s2.
Value in Register $s2 is: 0
================================================
=========
Clock cycle executed: 60
Current Instructiion being executed: add $s2, $s2, $s
5
========================================
Writing Back Row 7 in DRAM from Row Buffer.
62-71
========================================
Program execution completed
Total clock cycles consumed: 71
========================================
Contents of Register file:
$zero: 0, $at: 0, $v0: 0, $v1: 0, $a0: 0, $a1: 0, $a2
: 0, $a3: 0, $t0: 1388, $t1: 2710, $t2: 3e8, $t3: 0,
$t4: 0, $t5: 0, $t6: 0, $t7: 0, $s0: 0, $s1: 0, $s2:
0, $s3: 0, $s4: 0, $s5: 0, $s6: 0, $s7: 0, $t8: 0, $t
9: 0, $k0: 0, $k1: 0, $gp: 0, $sp: 0, $fp: 0, $ra: 0
========================================
Memory content at the end of the execution:
========================================
Count of row buffer updates:
Row with starting address 0 was loaded 1 times.
Row with starting address 4096 was loaded 1 times.
Row with starting address 7168 was loaded 1 times.
========================================
```

3. Accessing non existential values from DRAM memory. Returns garbage values vs 0. 181+10, 91, 84 cylces

```
main:
    addi $s0, $zero, 1000
    addi $s1, $zero, 2500
    addi $s5, $zero, 4000
    addi $t0, $zero, 1
    addi $t1, $zero, 2
    addi $t2, $zero, 3
    addi $t3, $zero, 4
    sw $t0, 0($s0)
    sw $t1, 0($s1)
    sw $t2, 4($s0)
    sw $t4, 4($s1)
    lw $t5, 0($s0)
    lw $t6, 0($s5)
    lw $t7, 4($s0)
    lw $t8, 4($s1)
exit:
```

```
Clock cycle executed: 181
Accessing Column 456 in Row Buffer.
Loaded value from Memory address 2504-2507 in the reg
ister $t8.
Value in Register $t8 is: 0
========================================
Program execution completed
Total clock cycles consumed: 181
========================================
Contents of Register file:
$zero: 0, $at: 0, $v0: 0, $v1: 0, $a0: 0, $a1: 0, $a2
: 0, $a3: 0, $t0: 1, $t1: 2, $t2: 3, $t3: 4, $t4: 0,
$t5: 1, $t6: 5630, $t7: 3, $s0: 3e8, $s1: 9c4, $s2: 0
, $s3: 0, $s4: 0, $s5: fa0, $s6: 0, $s7: 0, $t8: 0, $
t9: 0, $k0: 0, $k1: 0, $gp: 0, $sp: 0, $fp: 0, $ra: 0
========================================
Memory content at the end of the execution:
1000-1003: 1
1004-1007: 3
2500-2503: 2
2504-2507: 0
========================================
Count of row buffer updates:
Row with starting address 0 was loaded 4 times.
Row with starting address 2048 was loaded 3 times.
Row with starting address 3072 was loaded 1 times.
========================================
Number of times each instruction was executed:
        addi $s0, $zero, 1000
1
```

```
Clock cycles executed: 80-81
Accessing Column 928 in Row Buffer.
Loaded value from Memory address 4000-4003 in the reg
ister $t6.
Value in Register $t6 is: 0
========================================
Writing Back Row 3 in DRAM from Row Buffer.
82-91
========================================
Program execution completed
Total clock cycles consumed: 91
========================================
Contents of Register file:
$zero: 0, $at: 0, $v0: 0, $v1: 0, $a0: 0, $a1: 0, $a2
: 0, $a3: 0, $t0: 1, $t1: 2, $t2: 3, $t3: 4, $t4: 0,
$t5: 1, $t6: 0, $t7: 3, $s0: 3e8, $s1: 9c4, $s2: 0, $
s3: 0, $s4: 0, $s5: fa0, $s6: 0, $s7: 0, $t8: 0, $t9:
 0, $k0: 0, $k1: 0, $gp: 0, $sp: 0, $fp: 0, $ra: 0
========================================
Memory content at the end of the execution:
1000-1003: 1
1004-1007: 3
2500-2503: 2
2504-2507: 0
========================================
Count of row buffer updates:
Row with starting address 0 was loaded 1 times.
Row with starting address 2048 was loaded 1 times.
Row with starting address 3072 was loaded 1 times.
========================================
```

```
Clock cycle executed: 74
Accessing Column 928 in Row Buffer.
Loaded value from Memory address 4000-4003 in the reg
ister $t6.
Value in Register $t6 is: 32764
========================================
Writing Back Row 3 in DRAM from Row Buffer.
75-84
========================================
Program execution completed
Total clock cycles consumed: 84
========================================
Contents of Register file:
$zero: 0, $at: 0, $v0: 0, $v1: 0, $a0: 0, $a1: 0, $a2
: 0, $a3: 0, $t0: 1, $t1: 2, $t2: 3, $t3: 4, $t4: 0,
$t5: 1, $t6: 7ffc, $t7: 3, $s0: 3e8, $s1: 9c4, $s2: 0
, $s3: 0, $s4: 0, $s5: fa0, $s6: 0, $s7: 0, $t8: 0, $
t9: 0, $k0: 0, $k1: 0, $gp: 0, $sp: 0, $fp: 0, $ra: 0
========================================
Memory content at the end of the execution:
1000-1003: 1
1004-1007: 3
2500-2503: 2
2504-2507: 0
========================================
Count of row buffer updates:
Row with starting address 0 was loaded 1 times.
Row with starting address 2048 was loaded 1 times.
Row with starting address 3072 was loaded 1 times.
========================================
```

4. Intermediate optimizations

```
addi $t0, $t0, 1000
addi $t1, $t1, 2500
addi $t2, $t2, 5000
addi $t3, $t3, 7500
addi $t4, $t4, 10000
sw $t4, 0 ($t1)
lw $s0, 0 ($t4)
sw $s0, 0 ($t1)
add $s0, $s1, $t4
```

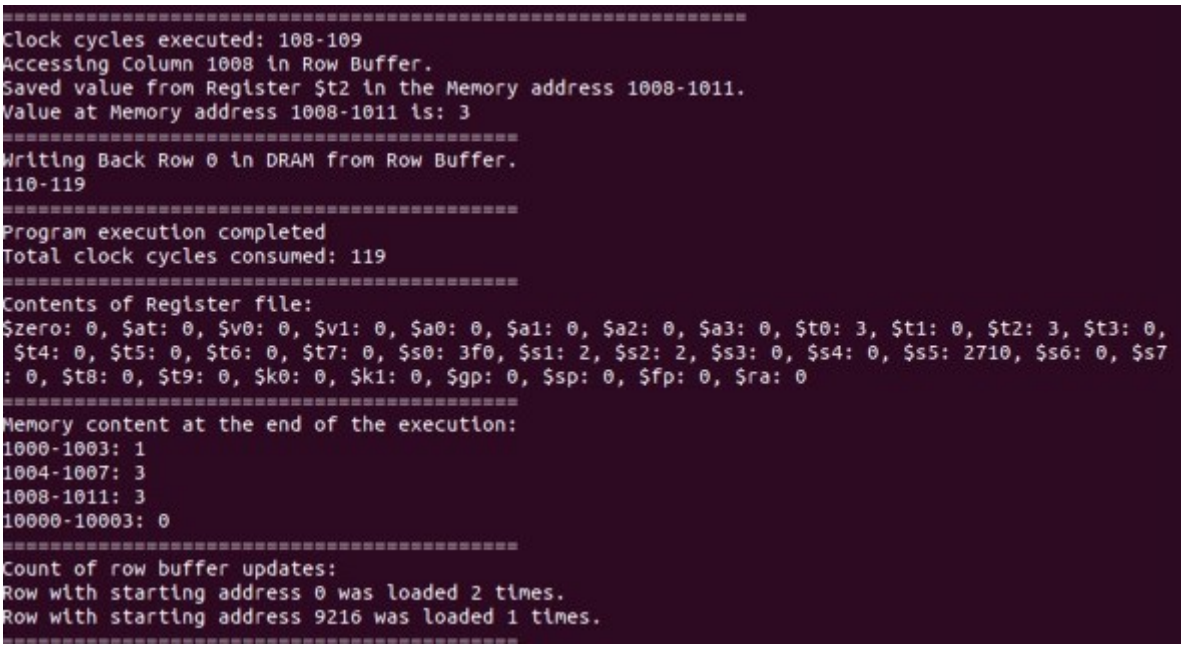
```
=========
Clock cycle executed: 65
Current Instructiion being executed: add $s0, $s1, $t
4
Updated value of $s0 to 10000.
========================================
Writing Back Row 2 in DRAM from Row Buffer.
66-75
========================================
Program execution completed
Total clock cycles consumed: 75
========================================
Contents of Register file:
$zero: 0, $at: 0, $v0: 0, $v1: 0, $a0: 0, $a1: 0, $a2
: 0, $a3: 0, $t0: 3e8, $t1: 9c4, $t2: 1388, $t3: 1d4c
, $t4: 2710, $t5: 0, $t6: 0, $t7: 0, $s0: 2710, $s1:
0, $s2: 0, $s3: 0, $s4: 0, $s5: 0, $s6: 0, $s7: 0, $t
8: 0, $t9: 0, $k0: 0, $k1: 0, $gp: 0, $sp: 0, $fp: 0,
 $ra: 0
========================================
Memory content at the end of the execution:
2500-2503: 0
========================================
Count of row buffer updates:
Row with starting address 2048 was loaded 2 times.
Row with starting address 9216 was loaded 1 times.
```

```
Clock cycle executed: 62
Accessing Column 452 in Row Buffer.
Saved value from Register $s0 in the Memory address 2
500-2503.
Value at Memory address 2500-2503 is: 0
========================================
Writing Back Row 2 in DRAM from Row Buffer.
63-72
========================================
Program execution completed
Total clock cycles consumed: 72
========================================
Contents of Register file:
$zero: 0, $at: 0, $v0: 0, $v1: 0, $a0: 0, $a1: 0, $a2
: 0, $a3: 0, $t0: 3e8, $t1: 9c4, $t2: 1388, $t3: 1d4c
, $t4: 2710, $t5: 0, $t6: 0, $t7: 0, $s0: 0, $s1: 0,
$s2: 0, $s3: 0, $s4: 0, $s5: 0, $s6: 0, $s7: 0, $t8:
0, $t9: 0, $k0: 0, $k1: 0, $gp: 0, $sp: 0, $fp: 0, $r
a: 0
========================================
Memory content at the end of the execution:
2500-2503: 0
========================================
Count of row buffer updates:
Row with starting address 2048 was loaded 2 times.
Row with starting address 9216 was loaded 1 times.
```

5. slt instruction optimization

```
main:
    addi $s0, $zero, 1000
    addi $s5, $s5, 10000
    addi $s1, $zero, 0
    addi $s2, $zero, 2
    addi $t1, $zero, 0
initloop:
    addi $t1, $t1, 1
    sw $t1, 0($s0)
    addi $s0, $s0, 4
    addi $s1, $s1, 1
    sw $t7, 0 ($s5)
    slt $s3, $s1, $s2
    bne $s3, $zero, initloop
    addi $s0, $zero, 1000
    addi $s1, $zero, 0
    addi $s3, $zero, 0
```

```
    addi $s2, $zero, 2
sumloop:
    lw $t0, 0($s0)
    addi $s0, $s0, 4
    lw $t1, 0($s0)
    add $t2, $t0, $t1
    sw $t2, 0($s0)
    addi $s1, $s1, 1
    slt $s3, $s1, $s2
    bne $s3, $zero, sumloop
```



6. Jump instruction optimization

```
addi $t1, $t1, 5
sw $t1, 2500 ($t0)
main:
    addi $t1, $t1, -1
    lw $t2, 5000 ($t0)
    beq $t1, $t0, label
    j main
label:
    add $t0, $t2, $t1
```

Exceptions:

1. Out of bound access:

```
main:
   sw $s0, 100000000000($s0)
```

```
================================================================
Clock cycle executed: 1
Current Instructiion being executed:    sw $s0, 10000000000000000($s0)
DRAM Request Issued
Segmentation fault
make: *** [makefile:37: run2] Error 139
```

2. Non existent register:

```
main:
   addi $s9, $s12, 12
```

```
Running the executable ...
cd ./build; ./nba ../input.txt

INVALID REGISTER DETECTED!! : $s12
Length: 4
```

3. Invalid instruction:

```
main:
   sw5 $s0, 1024
```

```
Running the executable ...
cd ./build; ./nba ../input.txt

INVALID INSTRUCTION DETECTED!! sw5
terminate called after throwing an instance of 'std::exception'
```

4. Invalid Branch:

```
main:
  j abc
```

```
Running the executable ...
cd ./build; ./nba ../input.txt
================================================================
Clock cycle executed: 1
Current Instructiion being executed:    j abc

INVALID Branch Detected!! : abc
terminate called after throwing an instance of 'std::exception'
  what():  std::exception
Aborted
```

5. Invalid syntax of instruction:

```
main:
   addi $s0, $s1, $s2
```

```
Running the executable ...
cd ./build; ./nba ../input.txt
================================================================
Clock cycle executed: 1
Current Instructiion being executed:    addi $s0, $s1, $s2
terminate called after throwing an instance of 'std::invalid_argument'
  what():  stoi
```