COL216 Minor Examination

Testing Report

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a) Non Blocking Memory Address

Row_access_delay = 4
Col_access_delay = 2

```
lw $t0, 0($s0)
addi $t1, $t1, 1
addi $t0, $t0, 1
```

```
============================================================
Clock cycle executed: 1
DRAM Request Issued
============================================================
Clock cycle executed: 2
Loading Row 0 in Row Buffer.
Updated value of $t1 to 1.
============================================================
Clock cycle executed: 3
Loading Row 0 in Row Buffer.
============================================================
Clock cycle executed: 4
Loading Row 0 in Row Buffer.
============================================================
Clock cycle executed: 5
Loading Row 0 in Row Buffer.
============================================================
Clock cycle executed: 6
Accessing Column 0 in Row Buffer.
============================================================
Clock cycle executed: 7
Accessing Column 0 in Row Buffer.
Loaded value from Memory address 0-3 in the register $t0.
Value in Register $t0 is: 0
============================================================
Clock cycle executed: 8
Updated value of $t0 to 1.
==========================================
Program execution completed
Total clock cycles consumed: 8
==========================================
```

b) Writing back RowBuffer to the DRAM and Nonblocking Memory

```
addi $t1, $zero, 1000
addi $t2, $zero, 1024
addi $s0, $s0, 2
sw $s0, 0($t1)
addi $s0, $s0, 1
sw $s0, 0($t2)
```

```
============================================================
Clock cycle executed: 1
Updated value of $t1 to 1000.
============================================================
Clock cycle executed: 2
Updated value of $t2 to 1024.
============================================================
Clock cycle executed: 3
Updated value of $s0 to 2.
============================================================
Clock cycle executed: 4
DRAM Request Issued
============================================================
Clock cycle executed: 5
Loading Row 0 in Row Buffer.
Updated value of $s0 to 3.
============================================================
Clock cycle executed: 6
Loading Row 0 in Row Buffer.
============================================================
Clock cycle executed: 7
Loading Row 0 in Row Buffer.
============================================================
Clock cycle executed: 8
Loading Row 0 in Row Buffer.
============================================================
Clock cycle executed: 9
Accessing Column 1000 in Row Buffer.
============================================================
Clock cycle executed: 10
Accessing Column 1000 in Row Buffer.
Saved value from Register $s0 in the Memory address 1000-1003.
Value at Memory address 1000-1003 is: 2
============================================================
```

```
============================================================
Clock cycle executed: 11
DRAM Request Issued
============================================================
Clock cycle executed: 12
Writing Back Row 0 in DRAM from Row Buffer.
============================================================
Clock cycle executed: 13
Writing Back Row 0 in DRAM from Row Buffer.
============================================================
Clock cycle executed: 14
Writing Back Row 0 in DRAM from Row Buffer.
============================================================
Clock cycle executed: 15
Writing Back Row 0 in DRAM from Row Buffer.
============================================================
Clock cycle executed: 16
Loading Row 1 in Row Buffer.
============================================================
Clock cycle executed: 17
Loading Row 1 in Row Buffer.
============================================================
Clock cycle executed: 18
Loading Row 1 in Row Buffer.
============================================================
Clock cycle executed: 19
Loading Row 1 in Row Buffer.
============================================================
Clock cycle executed: 20
Accessing Column 0 in Row Buffer.
============================================================
Clock cycle executed: 21
Accessing Column 0 in Row Buffer.
Saved value from Register $s0 in the Memory address 1024-1027.
Value at Memory address 1024-1027 is: 3
```

```
==========================================
Program execution completed
Total clock cycles consumed: 21
==========================================
Contents of Register file:
$zero: 0, $at: 0, $v0: 0, $v1: 0, $a0: 0, $a1: 0, $a2: 0, $
0, $s3: 0, $s4: 0, $s5: 0, $s6: 0, $s7: 0, $t8: 0, $t9: 0,
==========================================
Memory content at the end of the execution:
1000-1003: 2
1024-1027: 3
==========================================
Number of times each instruction was executed:
addi $t1, $zero, 1000
1
addi $t2, $zero, 1024
1
addi $s0, $s0, 2
1
sw $s0, 0($t1)
1
addi $s0, $s0, 1
1
sw $s0, 0($t2)
2
```

c) Exceptions

```
addi $t1, $zero, 1000
adde $t1, $t2, $t1
```

```
================================================================
Clock cycle executed: 1
Updated value of $t1 to 1000.
================================================================
Clock cycle executed: 2

INVALID INSTRUCTION DETECTED!! adde
```

d) Syntax error

```
addi $t1, $zero, 1000
addi $t1, $t2, $t1
```

```
================================================================
Clock cycle executed: 1
Updated value of $t1 to 1000.
================================================================
Clock cycle executed: 2
terminate called after throwing an instance of 'std::invalid_argument'
```