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entry:
%branch.addr = alloca i32, align 4
%i.addr = alloca i32, align 4
%A = alloca [10 x i32], align 16
%k = alloca i32, align 4
%result = alloca i32, align 4
store i32 0, %branch.addr, i32* %branch.addr, align 4
call void @llvm.dbg.declare(metadata i32* %branch.addr, metadata !289,
.. metadata !DIExpression()), !dbg !290
%branch.addr1 = bitcast i32* %branch.addr to i8*
call void @llvm.var.annotation(i8* %branch.addr1, i8* getelementptr inbounds
... ([7 x i8], [7 x i8]* @.str, i32 0, i32 0), i8* getelementptr inbounds ([21 x
... i8], [21 x i8]* @.str.1, i32 0, i32 0), i32 8, i8* null)
store i32 %i, i32* %i.addr, align 4
call void @llvm.dbg.declare(metadata i32* %i.addr, metadata !291, metadata
... !DIExpression()), !dbg !292
call void @llvm.dbg.declare(metadata [10 x i32]* %A, metadata !293, metadata
... !DIExpression()), !dbg !297
%0 = bitcast [10 x i32]* %A to i8*, !dbg !297
call void @llvm.memcpy.p0i8.p0i8.i64(i8* align 16 %0, i8* align 16 bitcast
... ([10 x i32]* @_const._Z12targetBranchii.A to i8*), i64 40, i1 false), !dbg
... !297
call void @llvm.dbg.declare(metadata i32* %k, metadata !298, metadata
... !DIExpression()), !dbg !299
%1 = load i32, i32* %branch.addr, align 4, !dbg !300
%idxprom = sext i32 %1 to i64, !dbg !301
%arrayidx = getelementptr inbounds [10 x i32], [10 x i32]* %A, i64 0, i64
... %idxprom, !dbg !301
%2 = load i32, i32* %arrayidx, align 4, !dbg !301
store i32 %2, i32* %k, align 4, !dbg !299
call void @llvm.dbg.declare(metadata i32* %result, metadata !302, metadata
... !DIExpression()), !dbg !303
store i32 0, i32* %result, align 4, !dbg !303
%3 = load i32, i32* %k, align 4, !dbg !304
switch i32 %3, label %sw.default [
i32 0, label %sw.bb
i32 1, label %sw.bb5
i32 2, label %sw.bb21
], !dbg !305, !prof !306
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sw.bb:
%4 = alloca i32, align 4, !dbg !307
%5 = load i32, i32* %4, align 4, !dbg !307
%6 = alloca i32, align 4, !dbg !307
%7 = load i32, i32* %6, align 4, !dbg !307
%8 = alloca i32, align 4, !dbg !307
%9 = load i32, i32* %8, align 4, !dbg !307
%10 = alloca i32, align 4, !dbg !307
%11 = load i32, i32* %10, align 4, !dbg !307
%12 = alloca i32, align 4, !dbg !307
%13 = load i32, i32* %12, align 4, !dbg !307
%14 = alloca i32, align 4, !dbg !307
%15 = load i32, i32* %14, align 4, !dbg !307
%16 = alloca i32, align 4, !dbg !307
%17 = load i32, i32* %16, align 4, !dbg !307
%18 = alloca i32, align 4, !dbg !307
%19 = load i32, i32* %18, align 4, !dbg !307
%20 = alloca i32, align 4, !dbg !307
%21 = load i32, i32* %20, align 4, !dbg !307
%22 = alloca i32, align 4, !dbg !307
%23 = load i32, i32* %22, align 4, !dbg !307
%24 = mul i32 %23, %2, !dbg !307
%pgocount = load i64, i64* @getelementptr inbounds ([4 x i64], [4 x i64]*
... @ _prof_c_Z12targetBranchii, i64 0, i64 2), align 8, !dbg !307
%25 = add i64 %pgocount, 1, !dbg !307
store i64 %25, i64* @getelementptr inbounds ([4 x i64], [4 x i64]*
... @ _prof_c_Z12targetBranchii, i64 0, i64 2), align 8, !dbg !307
%26 = load i32, i32* %result, align 4, !dbg !307
%div = sdiv i32 %26, 3, !dbg !307
store i32 %div, i32* %result, align 4, !dbg !307
%27 = load i32, i32* %i.addr, align 4, !dbg !309
%rem = srem i32 %27, 14, !dbg !310
%mul = mul nsw i32 %rem, 243, !dbg !311
%28 = load i32, i32* %result, align 4, !dbg !312
%xor = xor i32 %28, %mul, !dbg !312
store i32 %xor, i32* %result, align 4, !dbg !312
%29 = load i32, i32* %i.addr, align 4, !dbg !313
%rem2 = srem i32 %29, 10, !dbg !314
%idxprom3 = sext i32 %rem2 to i64, !dbg !315
%arrayidx4 = @getelementptr inbounds [10 x i32], [10 x i32]* %A, i64 0, i64
... %idxprom3, !dbg !315
%30 = load i32, i32* %arrayidx4, align 4, !dbg !315
%31 = load i32, i32* %result, align 4, !dbg !316
%add = add nsw i32 %31, %30, !dbg !316
store i32 %add, i32* %result, align 4, !dbg !316
br label %sw.epilog, !dbg !317

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sw.bb5:
%32 = alloca i32, align 4, !dbg !318
store volatile i32 42, i32* %32, align 4, !dbg !318
%33 = alloca i32, align 4, !dbg !318
store volatile i32 42, i32* %33, align 4, !dbg !318
%pgpcount1 = load i64, i64* getelementptr inbounds ([4 x i64], [4 x i64]*
... @ _prof_ Z12targetBranchii, i64 0, i64 0), align 8, !dbg !318
%34 = add i64 %pgpcount1, 1, !dbg !318
store i64 %34, i64* getelementptr inbounds ([4 x i64], [4 x i64]*
... @ _prof_ Z12targetBranchii, i64 0, i64 0), align 8, !dbg !318
%35 = load i32, i32* %i.addr, align 4, !dbg !318
%rem6 = srem i32 %35, 5, !dbg !319
%mul7 = mul nsw i32 %rem6, 9, !dbg !320
%36 = load i32, i32* %result, align 4, !dbg !321
%add8 = add nsw i32 %36, %mul7, !dbg !321
store i32 %add8, i32* %result, align 4, !dbg !321
%37 = load i32, i32* %i.addr, align 4, !dbg !322
%shr = ashr i32 %37, 3, !dbg !323
%38 = load i32, i32* %result, align 4, !dbg !324
%xor9 = xor i32 %38, %shr, !dbg !324
store i32 %xor9, i32* %result, align 4, !dbg !324
%39 = load i32, i32* %result, align 4, !dbg !325
%mul10 = mul nsw i32 %39, 2, !dbg !325
store i32 %mul10, i32* %result, align 4, !dbg !325
%40 = load i32, i32* %i.addr, align 4, !dbg !326
%mul11 = mul nsw i32 %40, 2, !dbg !326
store i32 %mul11, i32* %i.addr, align 4, !dbg !326
%41 = load i32, i32* %i.addr, align 4, !dbg !327
%rem12 = srem i32 %41, 14, !dbg !328
%mul13 = mul nsw i32 %rem12, 243, !dbg !329
%42 = load i32, i32* %result, align 4, !dbg !330
%xor14 = xor i32 %42, %mul13, !dbg !330
store i32 %xor14, i32* %result, align 4, !dbg !330
%43 = load i32, i32* %result, align 4, !dbg !331
%div15 = sdiv i32 %43, 3, !dbg !332
store i32 %div15, i32* %i.addr, align 4, !dbg !333
%44 = load i32, i32* %i.addr, align 4, !dbg !334
%rem16 = srem i32 %44, 5, !dbg !335
%mul17 = mul nsw i32 %rem16, 9, !dbg !336
%45 = load i32, i32* %result, align 4, !dbg !337
%add18 = add nsw i32 %45, %mul17, !dbg !337
store i32 %add18, i32* %result, align 4, !dbg !337
%46 = load i32, i32* %i.addr, align 4, !dbg !338
%shr19 = ashr i32 %46, 1, !dbg !339
%47 = load i32, i32* %result, align 4, !dbg !340
%xor20 = xor i32 %47, %shr19, !dbg !340
store i32 %xor20, i32* %result, align 4, !dbg !340
br label %sw.epilog, !dbg !341

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sw.bb21:
%48 = alloca i32, align 4, !dbg !342
store volatile i32 42, i32* %48, align 4, !dbg !342
%49 = alloca i32, align 4, !dbg !342
store volatile i32 42, i32* %49, align 4, !dbg !342
%50 = alloca i32, align 4, !dbg !342
store volatile i32 42, i32* %50, align 4, !dbg !342
%51 = alloca i32, align 4, !dbg !342
store volatile i32 42, i32* %51, align 4, !dbg !342
%52 = alloca i32, align 4, !dbg !342
store volatile i32 42, i32* %52, align 4, !dbg !342
%53 = alloca i32, align 4, !dbg !342
store volatile i32 42, i32* %53, align 4, !dbg !342
%54 = alloca i32, align 4, !dbg !342
store volatile i32 42, i32* %54, align 4, !dbg !342
%pgcount2 = load i64, i64* getelementptr inbounds ([4 x i64], [4 x i64]*
... @ _profic_Z12targetBranchii, i64 0, i64 1), align 8, !dbg !342
%55 = add i64 %pgcount2, 1, !dbg !342
store i64 %55, i64* getelementptr inbounds ([4 x i64], [4 x i64]*
... @ _profic_Z12targetBranchii, i64 0, i64 1), align 8, !dbg !342
%56 = load i32, i32* %i.addr, align 4, !dbg !342
%rem22 = srem i32 %56, 7, !dbg !343
%mul23 = mul nsw i32 %rem22, 91, !dbg !344
%57 = load i32, i32* %result, align 4, !dbg !345
%add24 = add nsw i32 %57, %mul23, !dbg !345
store i32 %add24, i32* %result, align 4, !dbg !345
%58 = load i32, i32* %i.addr, align 4, !dbg !346
%shr25 = ashr i32 %58, 2, !dbg !347
%59 = load i32, i32* %result, align 4, !dbg !348
%xor26 = xor i32 %59, %shr25, !dbg !348
store i32 %xor26, i32* %result, align 4, !dbg !348
%60 = load i32, i32* %i.addr, align 4, !dbg !349
%rem27 = srem i32 %60, 5, !dbg !350
%idxprom28 = sext i32 %rem27 to i64, !dbg !351
%arrayidx29 = getelementptr inbounds [10 x i32], [10 x i32]* %A, i64 0, i64
... %idxprom28, !dbg !351
%61 = load i32, i32* %arrayidx29, align 4, !dbg !351
%62 = load i32, i32* %result, align 4, !dbg !352
%sub = sub nsw i32 %62, %61, !dbg !352
store i32 %sub, i32* %result, align 4, !dbg !352
%63 = load i32, i32* %result, align 4, !dbg !353
%div30 = sdiv i32 %63, 3, !dbg !353
store i32 %div30, i32* %result, align 4, !dbg !353
br label %sw.epilog, !dbg !354

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sw.default:
%64 = alloca i32, align 4, !dbg !355
%65 = load i32, i32* %64, align 4, !dbg !355
%66 = alloca i32, align 4, !dbg !355
%67 = load i32, i32* %66, align 4, !dbg !355
%68 = alloca i32, align 4, !dbg !355
%69 = load i32, i32* %68, align 4, !dbg !355
%70 = alloca i32, align 4, !dbg !355
%71 = load i32, i32* %70, align 4, !dbg !355
%pgocount3 = load i64, i64* @getelementptr_inbounds ([4 x i64], [4 x i64]*
... @_profc_Z12targetBranchii, i64 0, i64 3), align 8, !dbg !355
%72 = add i64 %pgocount3, 1, !dbg !355
store i64 %72, i64* @getelementptr_inbounds ([4 x i64], [4 x i64]*
... @_profc_Z12targetBranchii, i64 0, i64 3), align 8, !dbg !355
store i32 -1, i32* %result, align 4, !dbg !355
br label %sw.epilog, !dbg !356
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sw.epilog:
%73 = load i32, i32* %result, align 4, !dbg !357
ret i32 %73, !dbg !358
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CFG for ' Z12targetBranchii' function