Lakshmi Anirudh Ghantasala

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OBJECTIVE

To obtain an Internship in or related to Machine Learning, Artificial Intelligence, Quantum Computing.

EDUCATION

PhD in Electrical and Computer Eng., Purdue University **Current**
Masters in ECE, Purdue University (FPGA, Machine Learning) (GPA: 3.34) **Dec 2019**
B.S EE with Minors in Biology and English, Purdue University (Honors College | GPA: 3.2) **May 2017**

SKILLS/LANGUAGES

Python (Tensorflow/Keras/Pytorch), Matlab, C++, C, Verilog, HTML, Javascript, Java, CUDA
Extensively used AWS, Google Collaboratory, Github

RESEARCH

Probabilistic Neural Networks for Optimization/Sampling Problems **June 2016 – Current**

I've published 3 papers in probabilistic computing using p-bits and have developed the headline website for p-bit research at Purdue, www.purdue.edu/p-bit. I am currently also leading FPGA development related to expedited p-circuit execution on the cloud. Through this work, I've become familiarized with various types of neural networks as well as implementing them in a broad range of settings, including MATLAB, python, C++, and in an FPGA. I've extensively worked with AWS and Google Collaboratory to expedite our processes.

- Leading FPGA development in team of 2 on AWS cloud servers
- Building and maintaining headline website for p-bit research at Purdue at www.purdue.edu/p-bit
- Developed a comprehensive python p-bit package with GPU/FPGA integration to be published on Github
- Carried out implementation and extensive benchmarking of various ML algorithms in MATLAB and Python not limited to SVMs, CNNs, RNNs, and LSTMS

Tungsten Diselenide Research for Spintronics Devices **Sep 2015-May 2016**

Fabricated WSe_2 transistors which could separate charge current into polarized spin current in the cleanrooms of the Birck Nanotechnology Center.

- Researched spin-device materials, and optimization of copper contacts in nanodevices
- Exfoliated WSe_2 monolayers, used software to lay contacts for WSe_2 transistors
- Measured IV curves for transistors, used cleanroom optical microscope to determine flake thickness and quality

Graphene Transistor Fabrication for Next-Gen Transistors **June 2015-Aug 2015**

Fabricated back-gated graphene transistors at the Indian Institute of Science. A thorough report of this experience can be found at https://www.linkedin.com/in/lakshmi-ghantasala/.

- Optimized fabrication process for back-gated graphene transistors
- Carried out cleanroom procedures including ultra-sonication, graphene exfoliation, N_2 blow drying, resist spin coating application.
- Observed a host of procedures used today for transistor fabrication including Lithography, Application of Masks, EBM, SEM, TEM, AFM, Raman Spectroscopy, PVD, and CVD

PROFESSIONAL EXPERIENCE

Software Intern - IT Seers Software Pvt Ltd **June-August 2015**

Became proficient with C++ development in a purely UNIX (bash) environment. IT Seers is a consulting firm in Bangalore India, which serves the IT needs of clients. I developed C++ code to enhance the accuracy of Optical Character Recognition software by training the default OpenCV recognition software with handwritten images.

- Improved upon standard OCR (optical character recognition) ML OpenCV code
- Trained default OpenCV recognition network to better recognize cursive handwriting with cursive image training sets
- Achieved 44% word accuracy up from 35% on a purely cursive handwritten document

Test Lab Technician - Stryker Corporation **May-August 2014**

The official duty of a Test Lab Technician is to run quality tests on various equipment engineered by Stryker. One of these tests required users to scan a list of results to separate those results that fell in a certain range. This was a mundane task which could easily be automated. I learned visual basic and automated the process within a few days. The results were noted by the manager, who put me in touch with the only programmer for the test lab. My automation was then put into effect in the test lab officially.

- Learned Visual Basic on the job, and implemented it in a company setting
- Upgraded Stryker testing flow with data-acquisition macros, enabling automatic testing of certain instruments

AWARDS

- 1st place Research Poster Presenter for Asynchronous FPGA modelling of p-bits (18 posters) **Oct. 9th, 2018**
- 1st place Research Poster Presenter for Purdue-P, a Platform for p-bit research (9 posters) **Oct. 9th, 2019**

PUBLICATIONS

- B. Sutton, R. Faria, L. A. Ghantasala, R. Jaiswal, K. Y. Camsari and S. Datta, "*Autonomous Probabilistic Coprocessing with Petaflips per Second*," **IEEE Access**, 10.1109/ACCESS.2020.3018682. 2020
- Ahmed Zeeshan Pervaiz, Brian M. Sutton, Lakshmi Anirudh Ghantasala, Kerem Y. Camsari, "*Weighted p-bits for FPGA Implementation of Probabilistic Circuits*" **IEEE-TNNLS***,* 10.1109/TNNLS.2018.2874565, p.1-7, 2018
- Ahmed Zeeshan Pervaiz, Lakshmi Anirudh Ghantasala, et al., "*Hardware Emulation of Stochastic p-Bits for Invertible Logic."* **Nature - Scientific Reports**, vol. 7, no. 1, 2017
- Lakshmi A. Ghantasala, "*Multiple CNNs for Dermatological Workflow Triaging*", TBD , 2020