Anirudh Srikant Iyengar

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Summary:

Fourth year Ph.D. student with experience in circuit and micro-architecture design in the field of energy-efficient spintronic memory and security, looking to obtain an internship position to pursue a career in research and development in memory and security.

Education:

- **Ph.D. in EECS,** Pennsylvania State University, (current).
- **Ph.D. in CSEE,** University of South Florida, (2013 – 2016), GPA of 3.70/4.0. (transfer)
- **M.S.E.E**, University of South Florida. (May 2013), GPA of 3.70/4.0.
- **B.E in Instrumentation and Control,** Manipal Institute of Technology, India, (June 2010). GPA 7.76/10.

Employment:

- Research Assistant, School of Electrical Engineering and Computer Science, PSU (fall 2016).
- Student Inten at Security Center of Excellence (SeCoE) Intel Corp. (summer 2016).
- Teaching Assistant, Department of Computer Science and Engineering, USF (spring 2015 – spring 2016).
- Research Assistant, Department of Computer Science and Engineering, USF (fall 2013 – spring 2016).
- Tutor at the athletics department for, USF (spring 2012).
- Assistant Software Engineer, Accenture, India (August 2010).

Research Interests:

My research is focused towards emerging spintronic devices for low-power and enhanced security. In particular, I am interested in the following topics:

- **Security using spintronics:** In this project, I investigate the prospects and challenges of spintronic devices towards hardware security.
  - → Investigating the emerging threat models, detection and protection mechanisms associated with spintronic memories. [J4, J5, C4, C7, C9].
  - → Exploit the randomness in Domain Wall dynamics for security primitives such as Physically Unclonable Functions. (**An inter/intra die Hamming distance of ~50%/5% was achieved**) [J1, J4, C2].
  - → Aside from this, I am also investigating the use of multi-threshold based CMOS logic, aimed at camouflaging ICs against cloning. [C5, C6].
  - → Additionally, I have explored the side channel vulnerabilities of STTRAM memory and have provided some low-overhead countermeasures [C8].
- **Application of spintronics:** In this project, I investigate the state retentive sequentials and non-volatile cache. [J3]
  - → Modeling, circuit design and micro-architectures for robust, low-power and energy efficient Domain wall memories (DWM). (**3-33% performance and 1.2X-14.4X power improvement achieved**) [J1, J2, C1, C3].
- **Reliability and retention analysis of spin transfer torque RAM (STTRAM) memory:** In this project I am modeling the STTRAM lifetime and retention and developing algorithms for test time improvement. [J5, C9]
- **Camouflaging of circuit design using threshold defined switches:** In this project, I investigate the potential security application of threshold voltage defined switches in circuit camouflaging.
  - → Investigate the tradeoff between area and performance overhead against reverse engineering effort [C5, C6].
  - → Look at the best-case implementation of camouflage gates, quantified over circuit node's observability and controllability metrics [P6].

- **Integrity and authentication of Printed Circuit Boards [PCB]:** In this project, I investigate some countermeasures to mitigate PCB cloning, and put forth benchmarks to test PCB security [P5].

  → I have also worked on PCB based PUFs for board authentication. [P9]

Publications:

Journals:

J1. **A. Iyengar**, S. Ghosh, K. Ramclam, "Domain Wall Magnets for Embedded Memory and Hardware Security"**, JETCAS**, 2014.

J2. S. Motaman, **Anirudh Iyengar**, and S. Ghosh, "Domain Wall Memory—layout, circuits and synergistic systems", **TNANO**, 2014. **Impact Factor: 1.62.**

J3. **A. Iyengar**, S. Ghosh, and J. Jang. "MTJ-Based State Retentive Flip-Flop with Enhanced-Scan Capability to Sustain Sudden Power Failure." **TCAS-I** (2015).

J4. **A. Iyengar**, S. Ghosh, K. Ramclam, J. Jang and C. Lin, "Spintronic PUFs for Security, Trust and Authentication" **JETC** (Special Issue on Secure and Trustworthy Computing), 2015.

J5. **A. Iyengar**, S. Srinivasan and S. Ghosh, "Retention Testing Methodology for STTRAM" **IEEE Design & Test**, 2016.

J6. S. Ghosh, **A. Iyengar** et. al, "Circuits, Systems and Applications of Spintronics" **JETCAS**, 2017.

J7. S Ghosh, RV Joshi, D Somasekhar, X Li, **A. Iyengar** et. al, "EMERGING MEMORIES—TECHNOLOGY, ARCHITECTURE, AND APPLICATIONS—SECOND ISSUE" **JETCAS, 2017.**

Conferences:

C1. **A. Iyengar** and S. Ghosh, "Modeling and analysis of domain wall dynamics for robust and low-power embedded memory", IEEE Design Automation Conference (***DAC***), 2014.

C2. **A. Iyengar,** K. Ramclam, S. Ghosh, "DWM-PUF: A Low-overhead, Memory-based Security Primitive". Symposium on Hardware-Oriented Security and Trust (**HOST**), 2014.

C3. S. Motaman, **A. Iyengar**, and S. Ghosh. "Synergistic circuit and system design for energy-efficient and robust domain wall caches." ***ISLPED***, 2014.

C4. N. Rathi, S. Ghosh, **A. Iyengar** and H. Naeimi, "Data Privacy in Non-Volatile Cache: Challenges, Attack Models and Solutions", **ASPDAC**, 2016.

C5. **A. Iyengar** and S. Ghosh, "Threshold Voltage-Defined Switches for Programmable Gates", **GOMACTech**, 2015.

C6. I. Nirmala, D. Vontela, S. Ghosh, **A. Iyengar** "A novel threshold voltage defined switch for circuit camouflaging", **ETS 2016**.

C7. **A. Iyengar,** "Retention Testing Methodology for STTRAM" **TECHCON 2016**.

C8. **A. Iyengar,** S. Ghosh, Nitin Rathi & Helia Naeimi Side Channel Attacks on STTRAM and Low-Overhead Countermeasures **DFT 2016.**

C9. N.I.Khan, **A. Iyengar** & S. Ghosh "Novel Magnetic Burn-In for Retention Testing of STTRAM" **DATE 2017** (accepted)

Poster Presentations:

P1. **Anirudh Iyengar**, Kenneth Ramclam, Jae-Won Jang & Cheng Wei Lin, "Spintronic PUFs for Security, Trust and Authentication", Cyber Security Awareness Week Conference (**CSAW**), 2014.

P2. **Anirudh Iyengar**, Nitin Rathi, Swaroop Ghosh, "Static and Dynamic Current Throttling for Improved Oxide Lifetime of STTRAM Arrays", IEEE Design Automation Conference (***DAC***), 2015.

P3. **Anirudh Iyengar**, Swaroop Ghosh, Deepakreddy Vontela & Ithihasa Reddy Nirmala "Threshold Defined Logic Engines and Applications", Florida Institute for Cybersecurity Research (**FICS**), 2016.

P4. **Anirudh Iyengar** & Swaroop Ghosh, "Threshold Voltage-Defined Switches for Programmable Gates", Government Microcircuit Applications & Critical Technology Conference (**GOMACTech**), 2016.

P5. **Anirudh Iyengar**, Fengchao Zhang, Swaroop Ghosh & Swarup Bhunia, "Split-Manufacturing of Printed Circuit Boards", IEEE Design Automation Conference (**DAC**), 2016.

P6. **Anirudh Iyengar**, Deepakreddy Vontela, Ithihasa Reddy Nirmala & Swaroop Ghosh, "A Novel Threshold Voltage Defined Switch for Circuit Camouflaging", IEEE European Test Symposium (**ETS**), 2016.

P7. **Anirudh Iyengar,** "Spintronic memory towards Secure and Energy-Efficient Computing" **PhD Forum at DAC** 2016.

P8. **Anirudh Iyengar**, "Retention Testing Methodology for STTRAM" abstract accepted for a full paper & poster presentation in **TECHCON 2016**.

P9. **Anirudh Iyengar** & Swaroop Ghosh, "Authentication of Printed Circuit Boards", International Symposium for Testing and Failure Analysis (**ISTFA**), 2016.

P10. **A. Iyengar,** S. Ghosh "Side Channel Attacks on STTRAM and Low-Overhead Countermeasures" **GOMACTech 2017.**

Invention Disclosures:

D1. Methods and Apparatus to Build Physically Unclonable Functions Using Spintronic Domain Wall Memory**,** Swaroop Ghosh, **Anirudh Iyengar**, and Kenneth Ramclam (filed May 2014).

D2. Non-Volatile Flip-Flop with Enhanced-Scan Capability to Sustain Sudden Power Failure**,** Swaroop Ghosh and **Anirudh Iyengar** (filed March 2015).

D3. Threshold Voltage Defined Switches for Programmable Camouflage Gates, **Anirudh Iyengar**, Swaroop Ghosh, Deepakreddy Vontela & Ithihasa Reddy Nirmala (filed June 2016)

D4. Novel Magnetic Burn-In for Retention Testing of STTRAM, Nasim Imtiaz Khan, **Anirudh Iyengar** & Swaroop Ghosh (under filing Nov 2016).

Class Projects:

- **SPA-Based attack on DES Encryption:** Crack the encryption key through a Trojan based side channel attack.
- **Design of low-power ALU with wide operating range**: Optimizing circuit design to sustain high performance at low power
- **Safety System for a Semi-Automatic Robot (**January-May 2010)**:** Create a safety device for a human controlled robot that is capable of working in an obstacle-filled terrain.
- **Huffman Encoder:** Characters were assigned a bit size depending on their frequency of occurrence, using Verilog HDL.
- **Micro- UART**: Design of the Universal Asynchronous Receiver and Transmitter in Verilog HDL.
- **AMBA APB Protocol:** Data management, control, transmission & reception using Sys Verilog.

Leadership and Awards:

- **Won** the **Best Poster Presentation award** at the 2016 PhD Forum at DAC.
- **Third place** in **Embedded Security Challenge** at Cyber Security Awareness Week Conference (**CSAW**), 2014.
- An article in ***IEEE XPLORE Innovation Spotlight***, titled "Domain Wall Memory: The Next Big Thing in Hardware Security?" July 2015.
- Organized and moderated events in the Fifth National Control Instrumentation Conference (CISCON) held at MIT, Manipal during November 2008.The conference is a National Annual event with participation from all over India.

Technical Skills:

- Languages: Verilog HDL, VerilogA HDL, PERL, VHDL, C.
- Design: Cadence Virtuoso, L-edit, Xilinx ISE, Circuit-maker.
- Simulation: Matlab, Hspice, Spectre, LT-Spice, Simple scalar, Model SIM, Questa SIM, PSpice.

Certifications:

- Plasma Etch Seminar (January 2012), hosted by Plasma Therm LLC.
- VLSI and Advanced System Design and Verification from January-June 2011, Sandeepani School organized by Core EL technologies, an authorized training partner of XILINX corp.
- Industrial Distributed control systems using Centum CS3000 under the guidance of the organization head, Broadfield Solutions from August-November 2010 as a project intern.