Anirudh Srikant Iyengar

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Objective:

To pursue a career in the field of Research and Development aimed at solving the problems of security, energy-efficiency and robustness which are the key challenges in the field of Electronic Design Automation.

Education:

- **Ph.D.,** University of South Florida, (2013 – current), GPA of 3.70.
- **M.S.E.E**, University of South Florida. (2011 – 2013), GPA of 3.70.
- **B.E in Instrumentation and Control,** Manipal Institute of Technology, India, 2010. GPA 7.76/10.

Employment:

- Assistant Software Engineer (August 2010), Accenture, India.
- Tutor at the athletics department for spring 2012.
- Research Assistant at the Department of Computer Science and Engineering (since fall 2013)
- Teaching Assistant at the Department of Computer Science and Engineering (since spring 2015)

Research Interests:

My research is focused towards emerging spintronic devices for low-power and enhanced security. In particular, I am interested in the following topics:

- **Security using spintronics:** In this project I am investigating the prospects and challenges of spintronic devices towards hardware security.
  - → Investigating the emerging threat models, detection and protection mechanisms associated with spintronic memories. [J4, C4].
  - → Exploit the randomness in Domain Wall dynamics for security primitives such as Physically Unclonable Functions. [J1, J4, C2].
  - → Aside from this, I have am also investigating the use of multi-threshold based CMOS logic, aimed at camouflaging ICs against cloning. [C6].
- **Application of spintronics:** In this project I am investigating the state retentive sequentials and non-volatile cache. [J3]
  - → Modeling, circuit design and micro-architectures for robust, low-power and energy efficient Domain wall memories (DWM). [J1, J2, C1, C3].
  - → Explore the application of DWM for implementing hardware accelerators. [C5].
- **Reliability and retention analysis of spin transfer torque RAM (STTRAM) memory:** In this project I am modeling STTRAM lifetime and retention and developing algorithms for test time improvement.

Publications:

Journal:

J1. **A. Iyengar**, S. Ghosh, K. Ramclam, "Domain Wall Magnets for Embedded Memory and Hardware Security"**,** **JETCAS**, 2014.

J2. S. Motaman, **Anirudh Iyengar**, and S. Ghosh, "Domain Wall Memory—layout, circuits and synergistic systems", **TNANO**, 2014. **Impact Factor: 1.62.**

J3. **A. Iyengar**, S. Ghosh, and J. Jang. "MTJ-Based State Retentive Flip-Flop with Enhanced-Scan Capability to Sustain Sudden Power Failure." **TCAS-I** (2015).

J4. **A. Iyengar**, S. Ghosh, K. Ramclam, J. Jang and C. Lin, "Spintronic PUFs for Security, Trust and Authentication" **JETC** (Special Issue on Secure and Trustworthy Computing), (accepted), 2015.

Conference:

C1. **A. Iyengar** and S. Ghosh, "Modeling and analysis of domain wall dynamics for robust and low-power embedded memory", IEEE Design Automation Conference (***DAC***), 2014.

C2. **A. Iyengar,** K. Ramclam, S. Ghosh, "DWM-PUF: A Low-overhead, Memory-based Security Primitive". Symposium on Hardware-Oriented Security and Trust (**HOST**), 2014.

C3. S. Motaman, **A. Iyengar**, and S. Ghosh. "Synergistic circuit and system design for energy-efficient and robust domain wall caches." ***ISLPED***, 2014.

C4. N. Rathi, S. Ghosh, **A. Iyengar** and H. Naeimi, "Data Privacy in Non-Volatile Cache: Challenges, Attack Models and Solutions", **ASPDAC**, 2016.

C5. **A. Iyengar** and S. Ghosh, "DWM-Based Spintronic Accelerators for Compute Intensive Operations", **DATE**, 2016 (under review).

C6. **A. Iyengar** and S. Ghosh, "Threshold Voltage-Defined Switches for Programmable Gates", **GOMACTech**, 2015 (under review).

Poster Presentations:

1. **Anirudh Iyengar**, Kenneth Ramclam, Jae-Won Jang & Cheng Wei Lin, "Spintronic PUFs for Security, Trust and Authentication", Cyber Security Awareness Week Conference (**CSAW**), 2014.
2. **Anirudh Iyengar**, Nitin Rathi, Swaroop Ghosh, "Static and Dynamic Current Throttling for Improved Oxide Lifetime of STTRAM Arrays", IEEE Design Automation Conference (***DAC***), 2015.

Invention Disclosures:

1. Methods and Apparatus to Build Physically Unclonable Functions Using Spintronic Domain Wall Memory**,** Swaroop Ghosh, **Anirudh Iyengar**, and Kenneth Ramclam (filed May 2014).
2. Non-Volatile Flip-Flop with Enhanced-Scan Capability to Sustain Sudden Power Failure**,** Swaroop Ghosh and **Anirudh Iyengar** (filed March 2015).

Class Projects:

- **SPA-Based attack on DES Encryption:** Crack the encryption key through a Trojan based side channel attack.
- **Design of low-power ALU with wide operating range**: Optimizing circuit design to sustain high performance at low power
- **Safety System for a Semi-Automatic Robot (**January-May 2010**):** Create a safety device for a human controlled robot that is capable of working in an obstacle-filled terrain.
- **Huffman Encoder:** Characters were assigned a bit size depending on their frequency of occurrence, using Verilog HDL.
- **Micro- UART**: Design of the Universal Asynchronous Receiver and Transmitter in Verilog HDL.
- **AMBA APB Protocol:** Data management, control, transmission & reception using Sys Verilog.

Leadership and Awards:

- **Third place** in **Embedded Security Challenge** at Cyber Security Awareness Week Conference (**CSAW**), 2014.
- An article in ***IEEE XPLORE Innovation Spotlight***, titled "Domain Wall Memory: The Next Big Thing in Hardware Security?" July 2015.
- Organized and moderated events in the Fifth National Control Instrumentation Conference (CISCON) held at MIT, Manipal during November 2008.The conference is a National Annual event with participation from all over India.

Skills:

- Languages: Verilog HDL, VerilogA HDL, PERL, VHDL, C.
- Design: Cadence Virtuoso, L-edit, Xilinx ISE, Circuit-maker.
- Simulation: Matlab, Hspice, Spectre, LT-Spice, Simple scalar, Model SIM, Questa SIM, PSpice.

Certification:

- VLSI and Advanced System Design and Verification from January-June 2011, Sandeepani School organized by Core EL technologies, an authorized training partner of XILINX corp.
- Plasma Etch Seminar (January 2012), hosted by Plasma Therm LLC.
- Industrial Distributed control systems using Centum CS3000 under the guidance of the organization head, Broadfield Solutions from August-November 2010 as a project intern.